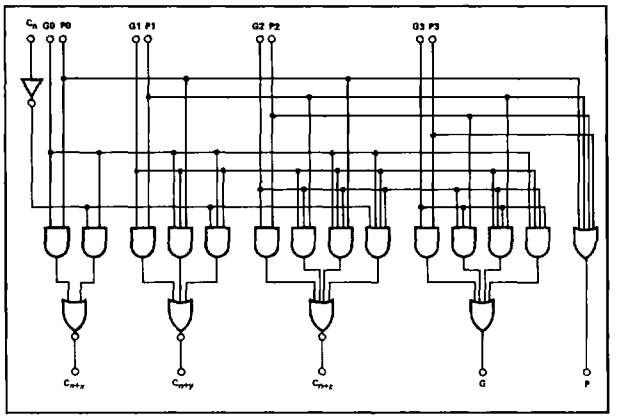
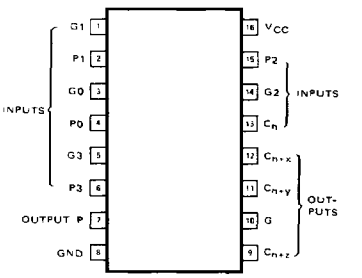
LOGIC DIAGRAM



PIN CONFIGURATION

B,F,W PACKAGE

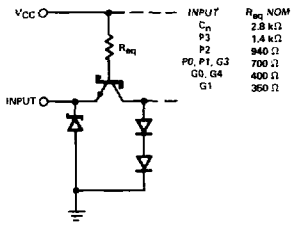


PIN DESIGNATIONS

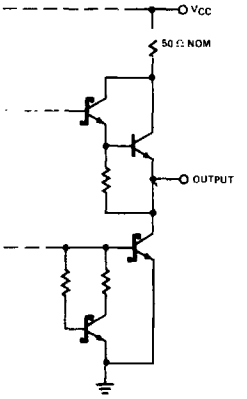
DESIGNATION	PIN NOS.	FUNCTION
G0, G1, G2, G3	3, 1, 14, 5	Active-Low Carry Generate Inputs
P0, P1, P2, P3	4, 2, 15, 6	Active-Low Carry Propagate Inputs
C_n	13	Carry Input
C_{n+x}, C_{n+y}, C_{n+z}	12, 11, 9	Carry Outputs
G	10	Active-Low Carry Generate Output
P	7	Active-Low Carry Propagate Output
V_{CC}	16	Supply Voltage
GND	8	Ground

INPUT/OUTPUT SCHEMATICS

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74 C_L=15pF R_L=400Ω			54/74S C_L=15pF R_L=280Ω			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Propagation delay time									
t_{PLH} Low-to-high				11	17				ns
t_{PHL} High-to-low				15	22				
t_{PLH} Low-to-high	G0,G1,G2, G3,P0,P1,	C_{n+x}, C_{n+y},					4.5	7	
t_{PHL} High-to-low	P2, P3	C_{n+z}					4.5	7	
t_{PLH} Low-to-high	G0,G1,G2, G3,P1,P2,	G					5	7.5	
t_{PHL} High-to-low	P3						7	10.5	
t_{PLH} Low-to-high	P0,P1,P2 P3	P					4.5	6.5	
t_{PHL} High-to-low							6.5	10	
t_{PLH} Low-to-high	C_n	C_{n+x}, C_{n+y},					6.5	10	
t_{PHL} High-to-low		C_{n+z}					7	10.5	

Load circuit and typical waveforms are shown at the front of section.

SPEED/PACKAGE RELIABILITY

54	F,W	74	B
54S	F,W	74S	B

LOGIC