

82502 ETHERNET TRANSCEIVER CHIP

- **Conforms to Following Standards:**
 - IEEE 802.3, 10BASE5 (Ethernet)
 - IEEE 802.3, 10BASE2 (Cheapernet)
 - Ethernet Version 2.0
- **Jabber Function**
- **Receive Based Collision Detection**
- **Defeatable Signal Quality Error (Heartbeat) Test**
- **Requires Minimum Board Space**
 - On-Chip Voltage Reference
 - 16 Pin DIP
- **No External Adjustments Required**
- **Reliable CHMOS Technology**

The 82502 Ethernet Transceiver Chip is a CHMOS VLSI device that provides the complete set of transmit, receive and collision detection functions specified by the IEEE 802.3, 10BASE5 (Ethernet) and 10BASE2 (Cheapernet) 10 Mbps baseband standards for the Media Attachment Unit (MAU). The 82502 teams up with Intel's 82586 LAN Coprocessor and the 82C501 Ethernet Serial Interface enabling the designer to implement highly integrated IEEE 802.3 systems.

Three basic functional blocks make up the 82502: transmit, receive and collision detection. The transmit and receive sections transfer data from the transceiver drop (Attachment Unit Interface or AUI) cable to the coaxial cable of the network and vice-versa. The collision detection section senses simultaneous transmissions by two or more network stations (collisions) on the coaxial cable and reacts by sending a 10 MHz signal across the transceiver drop cable to the station that it front ends.

When used in an Ethernet application, the 82502 can drive a transceiver cable up to 50 meters in length (for Cheapernet, there is no transceiver cable). The 82502 provides all active communications circuitry for the transceiver function in the Ethernet/Cheapernet environment. It is an ideal companion to the Intel 82C501.

The 82502 is fabricated in Intel's reliable 10V CHMOS II process.

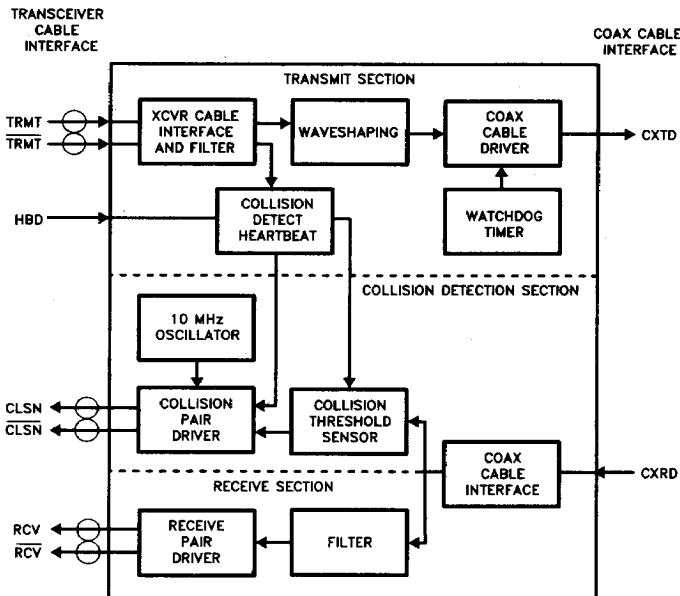


Figure 1. 82502 Functional Block Diagram

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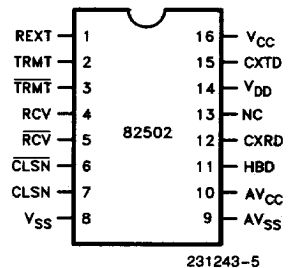


Figure 2. 82502 Pin Diagram

Table 1. Pin Description

Symbol	Pin No.	Type	Name and Function
TRMT, TRMT	2 3	I I	TRANSMIT DATA PAIR: A differentially driven input tied to the transmit pair of the transceiver cable. The transmit pair of the transceiver cable is driven with 10 Mbps Manchester encoded data from the serial interface of the data link (82C501). TRMT/TRMT must be isolated from the transceiver cable by a pulse transformer. The last transition is expected to be positive indicating end of packet.
RCV, RCV	4 5	O O	RECEIVE DATA PAIR: An output driver pair that generates an ECL AC signal level to drive the transceiver cable receive pair with the 10 Mbps Manchester encoded data received from the coaxial cable of the network. RCV/RCV must be isolated from the transceiver cable by a pulse transformer. The last transition is always positive indicating the end of the packet. The current from the RCV pin is incrementally decreased after the last transition.
CLSN, CLSN	7 6	O O	COLLISION PRESENCE PAIR: An output driver pair that generates a 10 MHz ECL AC signal level square wave on the collision presence pair of the transceiver cable when: a collision is detected on the coaxial cable of the network, during self-test as the collision circuit heartbeat indication, or after the watchdog timer has expired to indicate that the coaxial cable transmitter is disabled.
CXTD	15	O	COAXIAL CABLE TRANSMIT DATA: An output pin that transmits data onto the coaxial cable of the network by sinking current from the center conductor of the coaxial cable. The last data transition at the end of a packet is always low to high.
CXRD	12	I	COAXIAL CABLE RECEIVE DATA: An input pin that receives data from the coaxial cable of the network. Typical signal levels (referenced to V_{DD}) received on CXRD are -200 mV for high, -1.8 V for a low and 0 V during idle. The last data transition received is expected to be positive indicating the end of packet.
HBD	11	I	HEARTBEAT DISABLE: A strapping option that when tied low (V_{SS}), allows the transceiver to generate a collision detect heartbeat signal after each packet. A high (V_{CC}) on this pin disables the heartbeat circuitry as well as the 6.4μ s transmit inhibit timer but keeps the collision circuit enabled for use in repeater applications.
REXT	1		EXTERNAL RESISTOR: A 243Ω 0.5% resistor is attached between REXT and ground (V_{SS}) to provide precision internal current levels.
NC	13	NC	
V_{CC}^*	16		POWER: $5 \pm 10\%$ volts.
V_{SS}^*	8		GROUND
V_{DD}^*	14		POWER/COAX SHIELD: $10 \pm 10\%$ volts.
AV_{CC}^*	10		ANALOG POWER: $5 \pm 10\%$ volts. Included to reduce the effects of the current fluctuations in the V_{CC} pin.
AV_{SS}^*	9		ANALOG GROUND: Included to reduce the effects of current fluctuations in the V_{SS} pin.

***NOTE:**

These voltages are referenced to V_{SS} . The shield of the coaxial cable of the Ethernet channel (V_{DD}) is connected to earth ground.

FUNCTIONAL DESCRIPTION

Transmit Section

Transmit Pair Receiver

The 82502 receives transmit data from an Ethernet Serial Interface (ESI) on the TRMT pins and transmits it onto a 50 Ω coax cable (the Ethernet channel). The TRMT pins are connected to the transmit pair of a transceiver cable through a pulse transformer (see Figure 3). The transformer provides the isolation required between the transceiver cable and the coax cable. The DC bias for the TRMT pins is provided internally. The 78 \pm 5% Ω resistor for the TRMT input termination is external to the device.

A noise filter (squelch) is provided at the TRMT input pair to prevent spurious noise signals received on the pins from being transmitted onto the coaxial cable. The squelch is on during idle and rejects signals not more negative than -160 mV and/or less than 16 ns wide. The squelch is removed if the signal on the TRMT pins becomes more negative than -225 mV for 42 ns or more.

Once the squelch is removed, the transmit signal received on the device's TRMT pins measured differentially may be between \pm 0.25V minimum and \pm 1.32V maximum. The squelch will remain off if the received signal is not more positive than -225 mV or if it is more positive for less than 111 ns. The squelch will turn back on if the received signal is more positive than -160 mV for more than 215 ns. When the squelch turns back on a non-retriggerable 6.4 μ s transmit inhibit timer is started which disables the transmitter within 250 ns after the last transition for a minimum of 5.5 μ s and a maximum of 8 μ s.

The transmit data path through the device consists of a receiver, rise and fall time control circuitry, and coaxial cable current driver. The maximum timing distortion introduced by the device's transmit path is \pm 2 ns per data transition edge (t3) including timing

distortion caused by output rise and fall time difference. The maximum steady-state propagation delay of the transmit path is 50 ns.

Coaxial Cable Driver

The CXTD pin transmits data onto the coaxial cable by sinking current from the center conductor of the coaxial cable. The DC component of the output current level is between 37 mA and 45 mA. The AC component is from \pm 28 mA up to the DC component value. The idle current level is less than 5 μ A. Positive current is defined as current into the device. The output resistance is 9 K Ω minimum.

At the start of a frame transmission, no more than 2 bits of the frame information may be received from the TRMT pair and not transmitted onto the coaxial cable. The first bit transmitted by the 82502 may contain phase violations, however all successive bits of the frame will be valid.

Watchdog Timer (Jabber Function)

The 82502 Watchdog Timer will inhibit continuous transmissions onto the coaxial cable of duration greater than 52 ms \pm 18%. The timer starts timing when the TRMT squelch is turned off to receive valid transmit data on the TRMT pins. If a frame transmission is completed within the 52 ms time slot, the timer is reset 2 μ s to 6 μ s after the last bit of the frame has been transmitted. Two to six microseconds of reset delay is provided so that a short absence of transmit data will not reset the watchdog timer. If a new transmission is started within the reset delay time, the timer will not be reset.

If the timer times out (i.e., transmit frame duration exceeds 52 ms \pm 18%) the transmit section is disabled and the active collision signal is transmitted out onto the collision pair until transmit data received on the TRMT pair is discontinued. When the TRMT inputs become idle, the collision signal is turned off and a 420 ms (typical) non-retriggerable timer is started. During this 420 ms, the transmit section is disabled. The transmit section is re-enabled after 420 ms.

Receive Section

Coaxial Cable Receiver

The 82502's coaxial cable receive pins "V_{DD}" and "CXRD" are connected to the coax cable shield and center conductor, respectively.

The shunt capacitance measured between the V_{DD} and CXRD pins is typically 2.0 pF. The shunt resistance is greater than 1 M Ω . The input leakage current on the CXRD pin is between $-1 \mu\text{A}$ and $20 \mu\text{A}$. These conditions apply in both the power off and power on states.

A noise filter is provided at the V_{DD} and CXRD inputs to reject noise signals during idle. Signals received on the coax whose DC component (frequency less than 1 MHz) does not drop below -120 mV will be rejected. The noise filter will be disabled if the signal's DC component drops below -350 mV . A maximum of 4 bits will be received from the coaxial cable and may not be transmitted onto the RCV pair. The first bit transmitted may contain phase violations, however all successive bits of the frame will be valid.

The coaxial cable receiver compensation circuit is provided such that the combination of the coaxial cable and the receive circuit do not result in more than $\pm 6 \text{ ns}$ of edge jitter (t₁₀) for untapped minimum and maximum length Ethernet cables in a noise-free environment.

The noise filter will remain off if the received signal's AC component is not positive for more than 136 ns, and the DC component remains below -350 mV . While the filter is off, the received data will be transmitted onto the RCV pair with less than 50 ns steady state propagation delay. The timing distortion on the RCV pair output is less than $\pm 2 \text{ ns}$ per edge for a 400 mV peak-to-peak 5 MHz sinusoidal input from the coaxial cable.

The noise filter will turn back on if the received signal's AC component is positive for more than 210 ns, or if the DC component is more positive than -120 mV . The RXD driver is disabled within 275 ns after the last received data transition.

Receive Pair Driver

The RCV outputs are connected to the receive pair of a transceiver cable through a pulse transformer.

The receive pair (RXD/ $\overline{\text{RXD}}$) transceiver cable driver is a current driver. The output pins require $43.2 \Omega \pm 1\%$ pull-up resistors to V_{CC}. The differential output voltage level is between $\pm 580 \text{ mV}$ minimum and

$\pm 1\text{V}$ maximum, for a combined differential inductive load of 25 μH minimum and either 73 Ω or 83 Ω $\pm 1\%$ resistive load.

Between 200 ns and 325 ns after the last output data transition on the RCV/ $\overline{\text{RCV}}$ pins, the 82502 begins incrementally decreasing the RCV output current, using a series of small steps until it becomes idle. The maximum idle current levels on the RCV and $\overline{\text{RCV}}$ pins are 0.2 mA and 7 mA, respectively.

The purpose of the stepping sequence is to guarantee that the RCV/ $\overline{\text{RCV}}$ differential output signal (measured with a $78 \pm 5\%$ terminating resistor in parallel with a minimum magnetizing inductance of 25 μH) will remain high for a minimum of 200 ns following the last output transition, will not undershoot more than 80 mV and will limit the current stored in the inductor to 4 mA after 80 bit times.

Collision Detect Section

The collision presence outputs are connected to the collision pair of a transceiver through a pulse transformer. The collision presence outputs are used by the device to indicate one of three conditions: (1) there are simultaneous transmission attempts by two or more stations on the coax, (2) self test after a transmission proving that the collision circuitry is functional or (3) a frame transmission time exceeds the 52 ms watchdog timer time limit. The active collision presence signals is a 10 MHz $\pm 15\%$ ECL level square wave transmitted on the collision pair of the transceiver cable. The duty cycle of the square wave is better than 40/60 or 60/40. The collision pair driver has the same output signal characteristics as the receive pair driver.

The collision threshold DC level set inside the 82502 corresponds to $-1.495 \pm 5\%$ volts on the coaxial cable. When the collision filter's impulse response is taken into account, the threshold corresponds to a collision threshold between -1.492V and -1.58V . If the DC average signal level detected on the coaxial cable is more negative than the threshold, the on-chip oscillator transmits an active collision presence signal onto the collision pair. The delay in the device from the moment it detects a collision on the CXRD pin to the collision presence signal transmission onto the collision pair is less than 0.9 μs . With a 500 meter coaxial cable, it is less than 2.9 μs including the propagation delay of the coaxial cable.

Self Test

If the HBD input is strapped low, the self test feature of the 82502 is enabled. After each frame transmission, the device transmits a collision presence signal (heartbeat) onto the collision presence pair to indi-

cate that the collision circuitry is operational. The heartbeat begins between 600 ns to 1600 ns following the last positive transition on the transmit pair. The signal's duration is between 0.5 μ s and 1.5 μ s.

If the HBD input is strapped high, the self test feature as well as the 6.4 μ s transmit inhibit timer are disabled.

Design Example

Figure 3 shows the schematic of an IEEE 802.3, 10BASE5 (Ethernet) compatible transceiver based

on the 82502. Power to the 82502 is supplied by an isolated DC-to-DC converter which generates +5V \pm 10% and +10V \pm 10%. (These voltage levels are referenced to V_{SS}; remember that V_{DD} is connected to earth ground.) Small signal, high conductance diodes which have very small capacitance (less than 3 pF at V_d = 0) are connected between the CXTD input pin and the center conductor to reduce the capacitance load on the channel. A 100 Ω fusible resistor on the CXRD pin is to protect the network from being brought down in the event of a short circuit fault between the CXRD pin and GND.

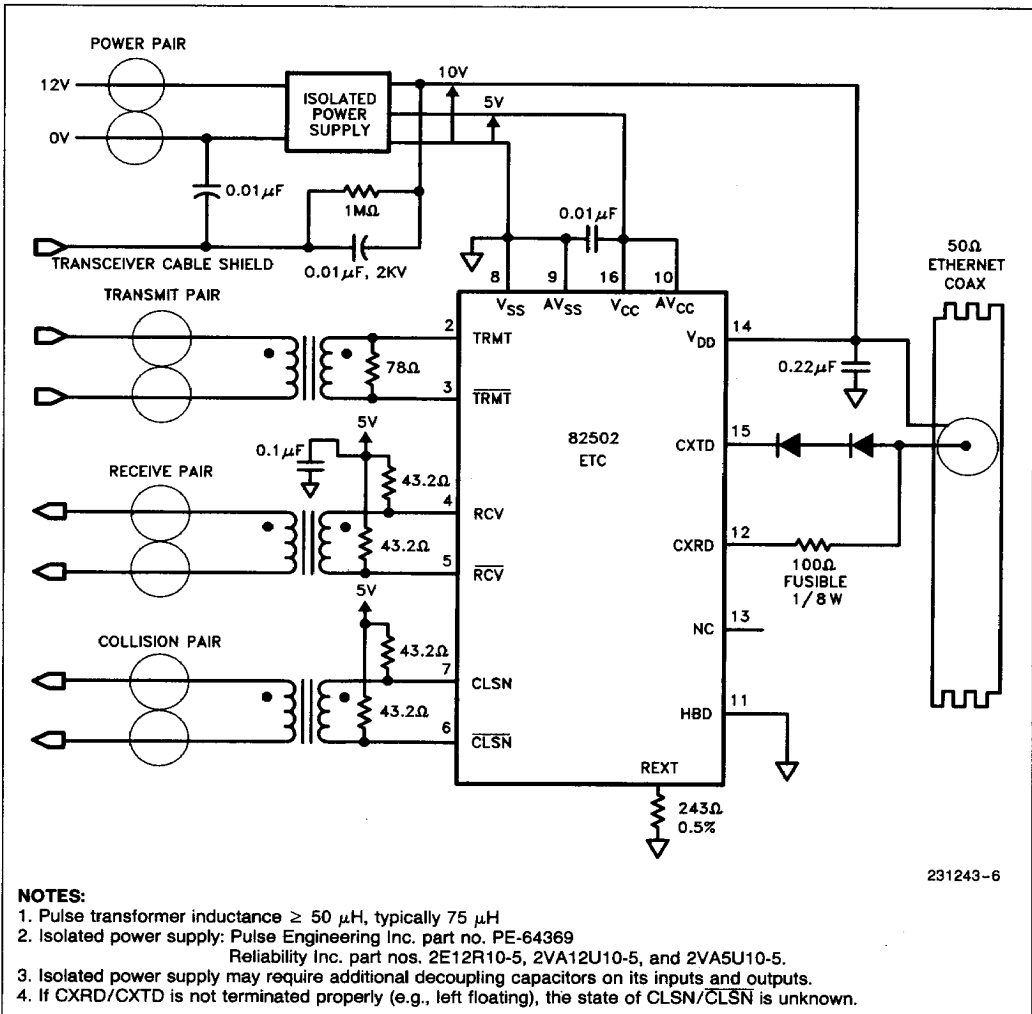


Figure 3. Typical 10BASE5 (Ethernet) Transceiver Implementation Using the 82502

Applications

The 82502 is intended for use in high performance, 10 Mbps LAN applications such as IEEE 802.3 10 Base 5 (Ethernet). Ethernet requires that the 82502 transceiver chip be located in a tap box attached directly to the coaxial cable of the network. A drop cable up to 50 meters in length connects the trans-

ceiver tap box to the data terminal equipment (DTE), see Figure 4.

In Cheapernet applications, a.k.a. IEEE 802.3 10 Base 2, the 82502 would be located inside the DTE, and transformer coupled to the 82C501, see Figure 5. In both applications, the IEEE specifications require that a DC isolated power supply power the 82502.

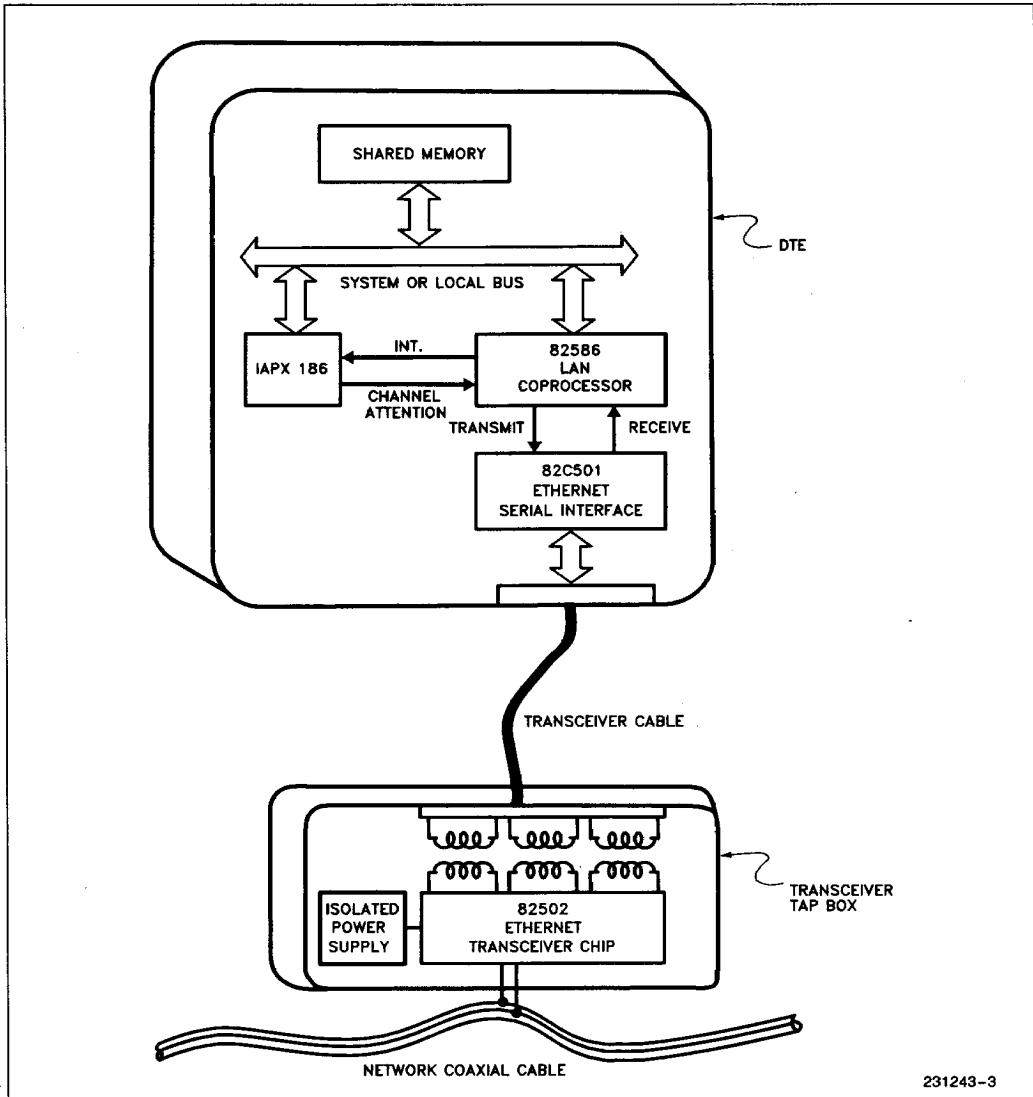


Figure 4. IEEE 802.3 10 Base 5 (Ethernet) configuration supports 100 users per segment, each segment being 500 meters long.

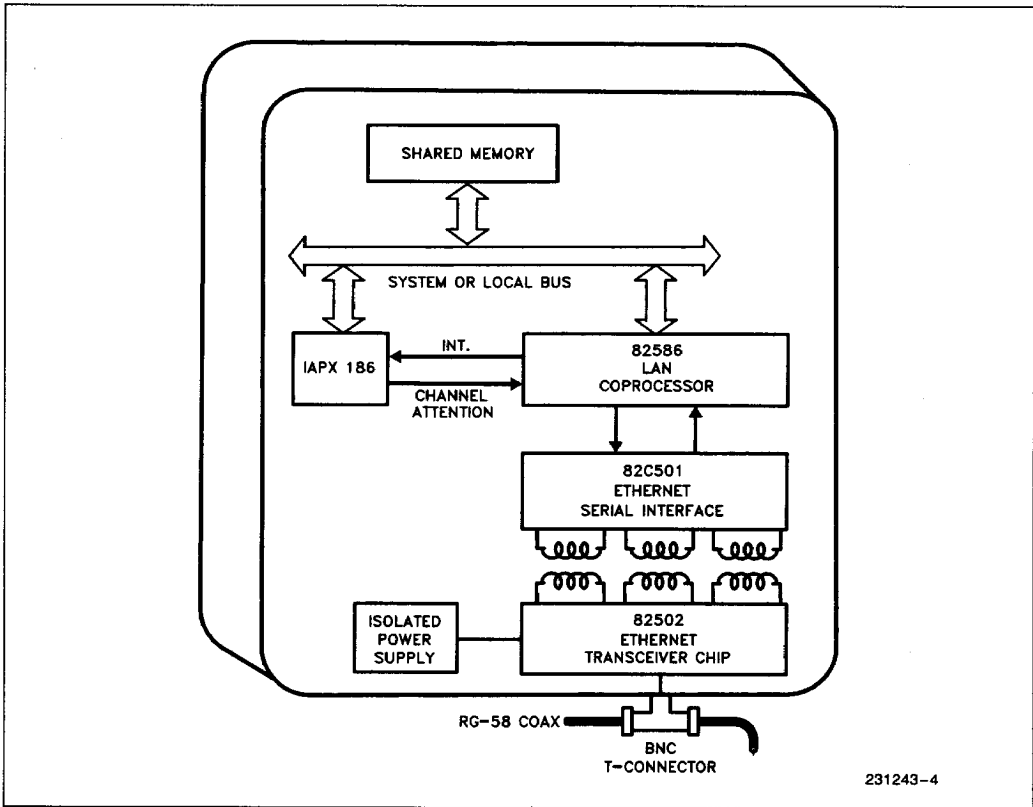


Figure 5. IEEE 802.3 10 Base 2 (Cheapernet) configuration supports 30 users per segment, each segment being 185 meters long.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias -10°C to +80°C
 Storage Temperature -65°C to +150°C
 V_{DD} with Respect to V_{SS} -0.5V to +15V
 V_{CC} with Respect to V_{SS} -0.5V to +11V
 All Input and Output Voltages
 (Except CXTD and CXRD) with
 Respect to V_{SS} -0.5V to +11V
 CXTD Output Voltage with
 Respect to V_{SS} -0.5V to +15V
 CXRD Input Voltage with
 Respect to V_{DD} 0V to -15V,
 > 0V if I_{CXRD} ≤ 200 mA
 Power Dissipation 1.0W

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

NOTICE: Specifications contained within the following tables are subject to change.

Operating maximum ratings assume the device transmitting 90% of its operating time.

D.C. CHARACTERISTICS T_A = 0°C–70°C, T_CMAX = 115°C, V_{CC} = 5V ±10%, V_{DD} = 10V ±10%

Symbol	Parameter	Limits			Units	Conditions
		Min	Typ	Max		
V _{IDF}	Transceiver Cable Input Differential Voltage	±250		±1400	mV	Base to peak
I _{AVEC}	CXTD Output Current DC Component (Including the effects of timing distortion)	37		45	mA	CXTD: 3.3V to 10.3V
I _{ACC}	CXTD Output Current AC Component	±28	±31	±I _{AVEC}	mA	
I _{IDC}	CXTD Idle Output Current			5	µA	CXTD: 0V to 11V
V _{ICAC}	Coax Receiver A.C. Voltage	±200			mV	Base to peak
I _{I LC}	Input Leakage Current CXRD	-1		20	µA	
V _{ODF}	Differential Output Swing RCV and CLSN	±0.58		±1.0	V	R _L = 73Ω to 83 Ω ±1% R _{PULLUP} = 43.2Ω ±1% L ≥ 25 µH
I _{IDT}	Output Idle Current Transceiver Cable	3		7 0.2	mA mA	RCV and CLSN RCV and CLSN
I _{CC}	V _{CC} and AV _{CC} Supply Current			23	mA	
I _{DD}	V _{DD} Supply Current			43	mA	
R _I	Shunt Resistance between V _{DD} and CXRD	1			MΩ	
C _I	Shunt Capacitance between V _{DD} and CXRD		2	3	pF	f = 10 MHz

A.C. CHARACTERISTICS

A.C. Measurement Conditions

I. $T_A = 0^\circ\text{C}$ to 70°C , $T_{C\text{MAX}} = 115^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, $V_{DD} = 10\text{V} \pm 10\%$

II. The A.C. measurements are taken at the following voltage levels for the various kinds of inputs and outputs:

A. Differential Transceiver Cable Inputs and Outputs:

All delay and timing distortion measurements are referenced to the 0V points measured differentially. Rise and fall times are referenced to the 20% and 80% points. The differential voltage swing at the inputs is at least $\pm 275\text{ mV}$ with rise and fall times of 0 to 10 ns.

B. Coaxial Cable Inputs and Outputs:

Delay measurements are referenced to the 50% points of the signals' total swing. V_{DD} is used as the voltage reference. Rise and fall times are measured at the 20% and 80%

points. The differential voltage swing at the inputs is at least $\pm 200\text{ mV}$. The input signal is either a trapezoidal signal with $25 \pm 5\text{ ns}$ rise/fall times or a sine wave.

In order to simulate a collision, DC voltage of -2.2V referenced to V_{DD} is applied to the CXRD pin.

C. Redundant Transmit Squelch Output:

Delay measurements are referenced to the 50% point of the total swing.

III. The A.C. loading for various outputs is as follows:

A. Transceiver cable drive pins:

RCV, $\overline{\text{RCV}}$, CLSN and $\overline{\text{CLSN}}$ are each loaded with 10 pF to ground and 43.2Ω to V_{CC} . A parallel load of $25\ \mu\text{H}$ minimum and 78Ω is connected between RCV and $\overline{\text{RCV}}$. The same load is present on CLSN and $\overline{\text{CLSN}}$.

B. Coaxial Cable Driver Pins:

A 25Ω resistor is connected between V_{DD} and CXRD. One small signal diode is connected between the CXRD and CXTD pins such that it conducts when the 82502 is transmitting.

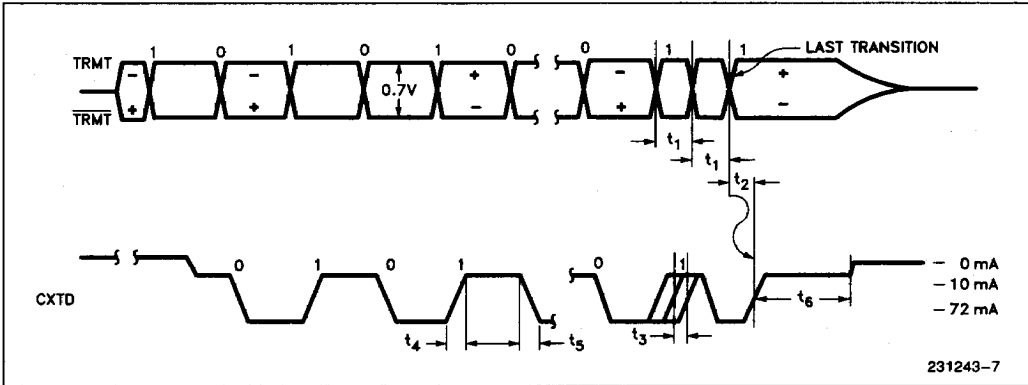
TRANSMIT TIMING

Symbol	Parameter	Limits			Units
		Min	Typ	Max	
t_1	TRMT/TRMT Input Pulse Width	44		106	ns
t_2	Transmit Steady State Delay			50	ns
t_3	CXTD Output Edge Jitter			± 2	ns
t_4	CXTD Rise Time	20		30	ns
t_5	CXTD Fall Time	20		30	ns
t_6	Last Data Transition to CXTD Disabled			250	ns

NOTE:

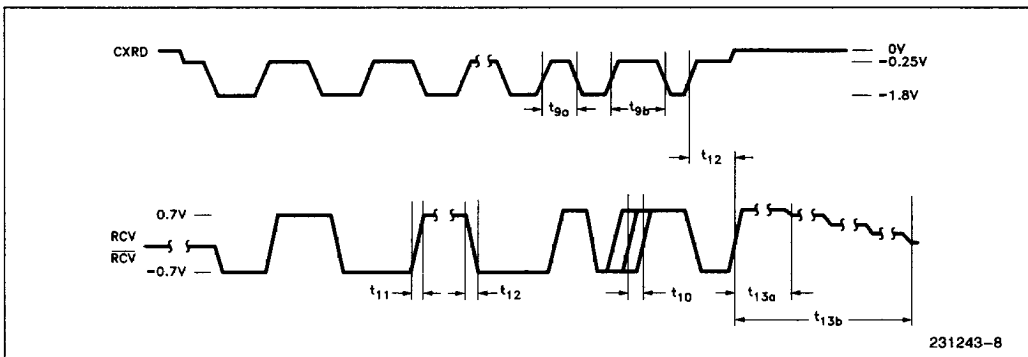
Timings t_7 and t_8 have been deleted.

TRANSMIT TIMING (Continued)



RECEIVE TIMING

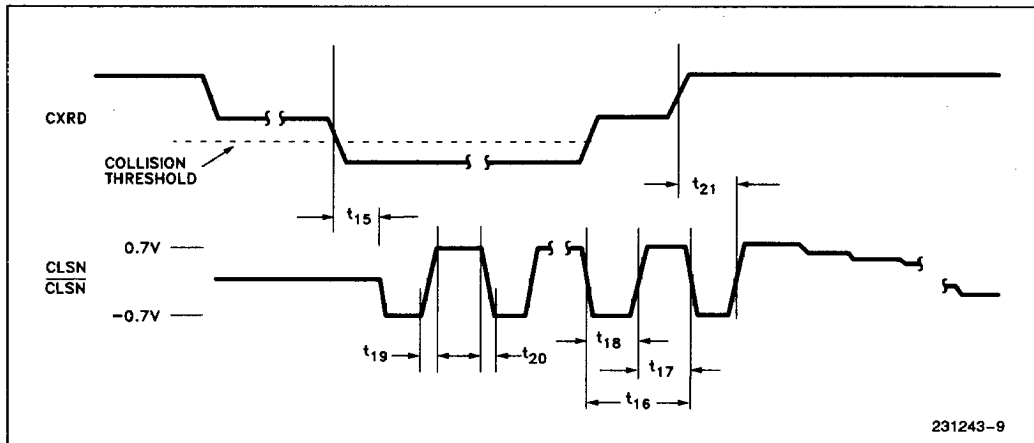
Symbol	Parameter	Limits			Units
		Min	Typ	Max	
t_9	CXRD Input Pulse Width				
	a) Manchester Short Pulse	28		72	ns
	b) Manchester Long Pulse	68		132	ns
t_{10}	RCV/ \overline{RCV} Output Edge Jitter			± 6	ns
t_{11}	RCV/ \overline{RCV} Rise Time		3	6	ns
t_{12}	RCV/ \overline{RCV} Fall Time		3	6	ns
t_{13}	Last RCV/ \overline{RCV} Transition to Idle	200			
	a) RCV/ \overline{RCV} Held High from Last Positive Transition			8000	ns
	b) RCV/ \overline{RCV} Becomes Idle				ns
t_{14}	Receive Steady-State Propagation Delay			50	ns



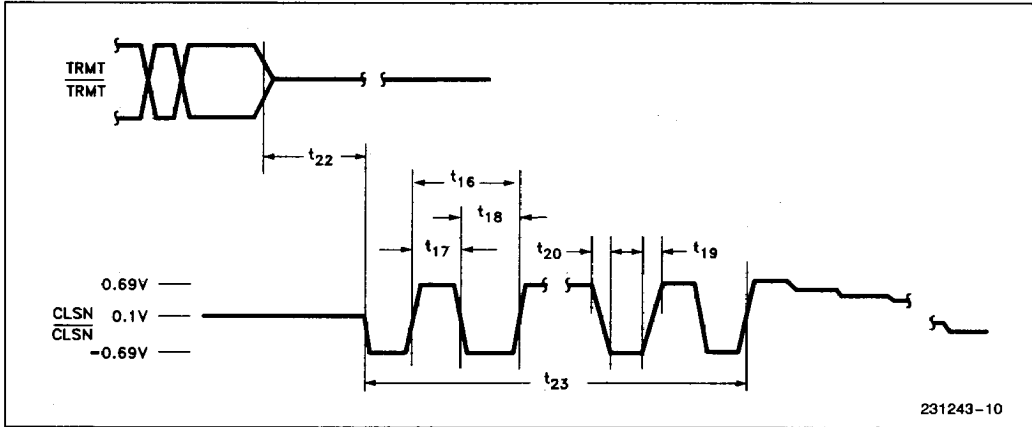
COLLISION AND HEARTBEAT TIMING

Symbol	Parameter	Limits			Units
		Min	Typ	Max	
t ₁₅	Delay from Collision on CXRD to First Negative Transition on CLSN/ $\overline{\text{CLSN}}$			900	ns
t ₁₆	CLSN/ $\overline{\text{CLSN}}$ Cycle Time	86		117	ns
t ₁₇	CLSN/ $\overline{\text{CLSN}}$ High Time	35		70	ns
t ₁₈	CLSN/ $\overline{\text{CLSN}}$ Low Time	35		70	ns
t ₁₉	CLSN/ $\overline{\text{CLSN}}$ Rise Time		3		ns
t ₂₀	CLSN/ $\overline{\text{CLSN}}$ Fall Time		3		ns
t ₂₁	Delay from End of Collision to Last CLSN/ $\overline{\text{CLSN}}$ Transition			2	μs
t ₂₂	Last TRMT/ $\overline{\text{TRMT}}$ Transition to Start of Heartbeat Packet	600		1600	ns
t ₂₃	Heartbeat Packet Duration	500		1500	ns

COLLISION TIMING



HEARTBEAT TIMING



WATCHDOG TIMER TIMING

Symbol	Parameter	Limits			Units
		Min	Typ	Max	
t_{24}	Watchdog Timer Time Out Time	43	52	61	ms
t_{25}	Transmitter Reset Period after CLSN/CLS Transmission due to Watchdog Timer Time Out	340	420	550	ms

WATCHDOG TIMER TIMING

