MULTI-NORM PULSE-PATTERN GENERATOR

GENERAL DESCRIPTION

The SAD1019 is part of a frame transfer image sensor camera system which uses the NXA series of frame transfer image sensors. The device provides the vertical transport pulses necessary, for the operation of the frame transfer image sensors and a start-stop signal for the horizontal clock generator. The drive pulses and clock signals for the SAD1019 are provided by the universal sync generator (SAA1043).

Features

- Vertical transport pulses for the image region and storage region of the image sensor during field blanking (ϕ_A and ϕ_B pulses)
- Colour separation and transport of one line of sensor information to the output register during line blanking (ϕ_B, TG and ϕ_C pulses)
- Other additional pulses required for the control and processing in the frame transfer image sensor camera

PACKAGE OUTLINES

SAD1019: 24-lead DIL; plastic (SOT101B).
SAD1019T: 24-lead mini-pack; plastic (SO24; SOT137A).

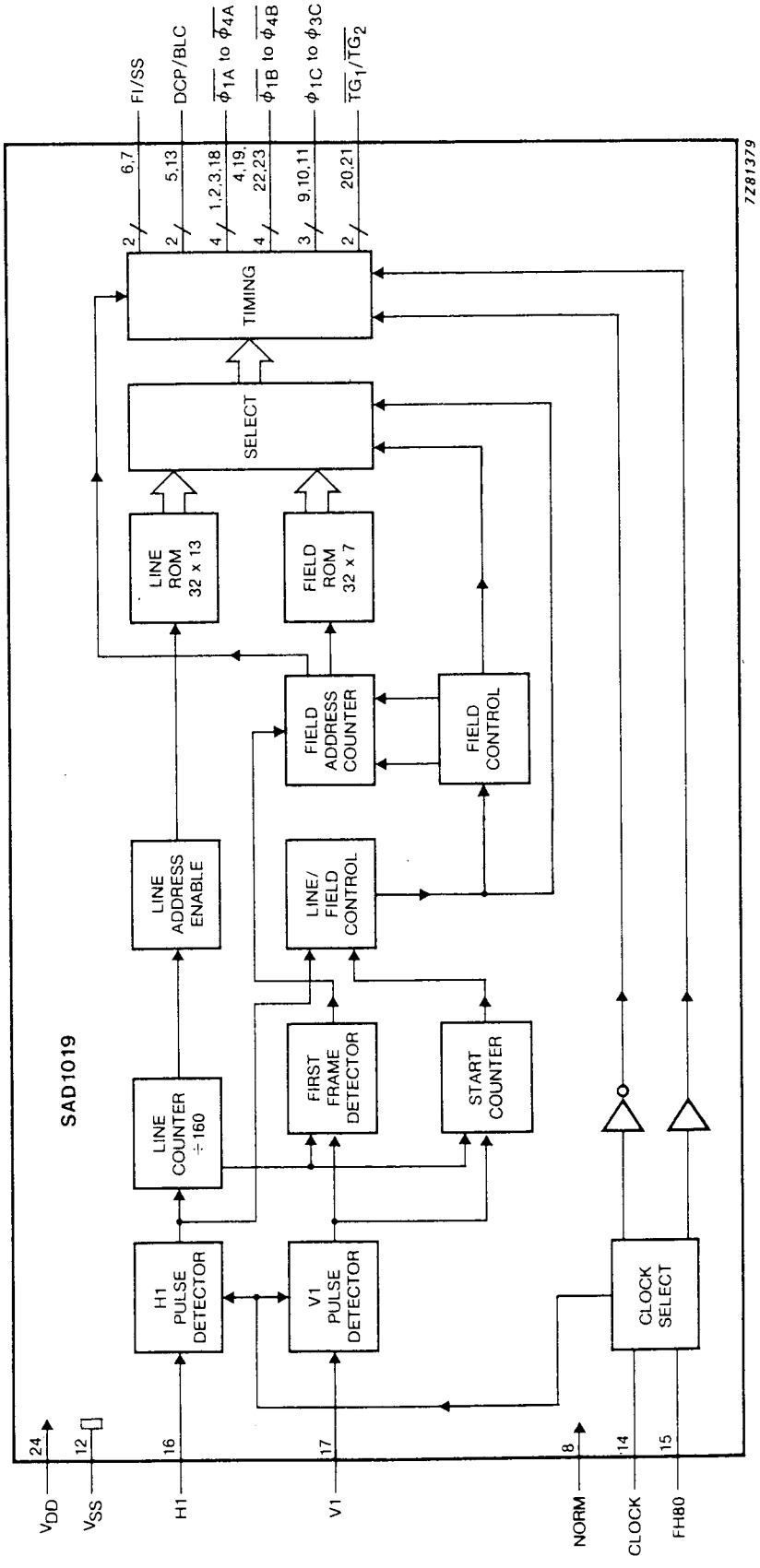


Fig.1 Block diagram.

PINNING

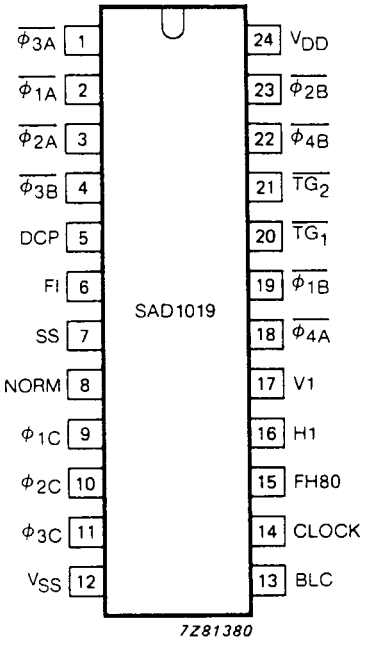


Fig.2 Pinning diagram.

Power supplies

V_{DD}	positive supply voltage (+ 5 V)
V_{SS}	ground (0 V)

Inputs (CMOS)

CLOCK	clock input from SAA1043, typ. 2.5 MHz (625 lines) or typ. 2.51748 MHz (525 lines). 5 MHz mode, typ. 5 MHz (625 lines) or 5.03496 MHz (525 lines)
FH80	clock input from SAA1043, typ. 1.25 MHz (625 lines) or 1.25874 MHz (525 lines)
H1	H1 input from SAA1043, typ. 15.625 kHz (625 lines) or typ. 15.734 kHz (525 lines)
V1	V1 input from SAA1043, typ. 50 Hz (625 lines) or 59.94 Hz (525 lines)
NORM	norm-selection input, 625 lines = LOW, 525 lines = HIGH

Outputs (CMOS push-pull)

$\overline{\phi 1A}$ to $\overline{\phi 4A}$	sensor image section control to drivers
$\overline{\phi 1B}$ to $\overline{\phi 4B}$	sensor storage section control to drivers
$\phi 1C$ to $\phi 3C$	low frequency outputs for transport pulses to pixel oscillator
DCP	DC clamp pulse
FI	frame identification
SS	start/stop for pixel generator
BLC	black-level clamping
$\overline{TG_1}$ and $\overline{TG_2}$	transfer gate control to drivers

FUNCTIONAL DESCRIPTION

625 line mode (NORM = LOW, see Figs 3 to 7)

One complete cycle of the multi-norm pulse-pattern generator (MNPPG) occurs after a command from the synchronization pulse generator (SYN). This cycle consists of 294 line cycles which are used to read out the sensor information followed by transport of the integrated information from the image area to the storage area of the sensor. Once this cycle has been completed the device enters into a 'wait' status period which lasts until the device receives a start command from the SYN.

The cycle is restarted with a V-pulse from the SYN. The falling edge of this pulse is detected in the MNPGG and results in a reset of the start counter as well as providing the field information (field 1/2). The start counter counts 11 lines and then the line cycle information is read from the line ROM. The start of the line cycle occurs at line 22 in frame 1 and line 335 in frame 2. The H1 pulse of the SYN controls the position of the line cycle with respect to the SYN pulses. The H1 pulse sets the correct value in the line counter of the MNPPG.

The control counter counts the number of line cycles and switches the line cycle to field cycle after 294 lines (in both fields), then the field cycle information is read from the field ROM. The control counter was reset before the switch over had taken place, it now counts the field cycles. The field cycle lasts for 294 cycles of the $\overline{\phi 4B}$ pulse and then the device enters the wait status period again.

The device will continue to operate in the manner described, until the overall system is switched off.

525 line mode (NORM = HIGH)

The basic operation is identical except for variations in the start points and number of transports (see Figs 8 to 12).

Operating modes

Synchronization generator (SAA1043)

The H1 pulse from the SAA1043, due to internal delays, is out of phase with the MNPPG clock signal. The following method is used to obtain the correct phase relationship between the H1 pulse and the MNPPG output. The H1 pulse and the FH80 are clocked into a flip-flop, at the output of the flip-flop the timing of the H1 and FH80 signals are in phase. The output of the flip-flop is sampled with that of the CLOCK, which is in phase with the FH80. In this way a reliable fixed phase relationship between SYN and MNPPG is obtained.

Other operating modes

- single 2.5 MHz operation:
  If another synchronization pulse generator is used, in which an H1 pulse is in phase with the CLOCK, a single 2.5 MHz clock signal can be used.

  Connect the 2.5 MHz to the CLOCK and with delay circuitry (RC elements, 50 ns approx.) to FH80.
- single 5 MHz operation:
  If another synchronization pulse generator is used, in which an H1 pulse is in phase with the CLOCK, a single 5 MHz clock signal can be used.

  Connect the 5 MHz to the CLOCK and connect FH80 to ground.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range (pin 24)	V_{DD}	−0.5	+ 7.0	V
Supply current (pin 24)	I_{DD}	–	50	mA
Supply current (pin 12)	I_{SS}	–	50	mA
Input voltage range	V_I	−0.5	V_{DD} + 0.5*	V
Input current	$\pm I_I$	–	10	mA
Output current	$\pm I_O$	–	10	mA
Total power dissipation per package	P_{tot}	–	500	mW
Power dissipation per output	P_O	–	25	mW
Operating ambient temperature range	T_{amb}	−25	+ 70	°C
Storage temperature range	T_{stg}	−55	+ 150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is good practice to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

* V_{DD} + 0.5 V not to exceed 7.0 V.

CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; T_{amb} = 25 °C, unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Current						
Supply current	on all outputs; I_O = 0 mA	I_{DD}	–	–	10	μA
Inputs H1, V1, NORM, CLOCK and FH80						
Input voltage HIGH		V_{IH}	$0.7V_{DD}$	–	–	V
Input voltage LOW	CMOS compatible	V_{IL}	–	–	$0.3V_{DD}$	V
Outputs						
Output voltage HIGH	all outputs except BLC; $-I_O$ = 0.8 mA; V_{DD} = 5 V	V_{OH}	–	–	$V_{DD}-0.5$	V
Output voltage LOW	all outputs except BLC; I_O = 2.9 mA; V_{DD} = 5 V	V_{OL}	–	–	0.5	V
Black level clamping (BLC)						
Output voltage HIGH	$-I_O$ = 2.6 mA; V_{DD} = 5 V	V_{OH}	–	–	$V_{DD}-0.5$	V
Output voltage LOW	I_O = 2.9 mA; V_{DD} = 5 V	V_{OL}	–	–	0.5	V

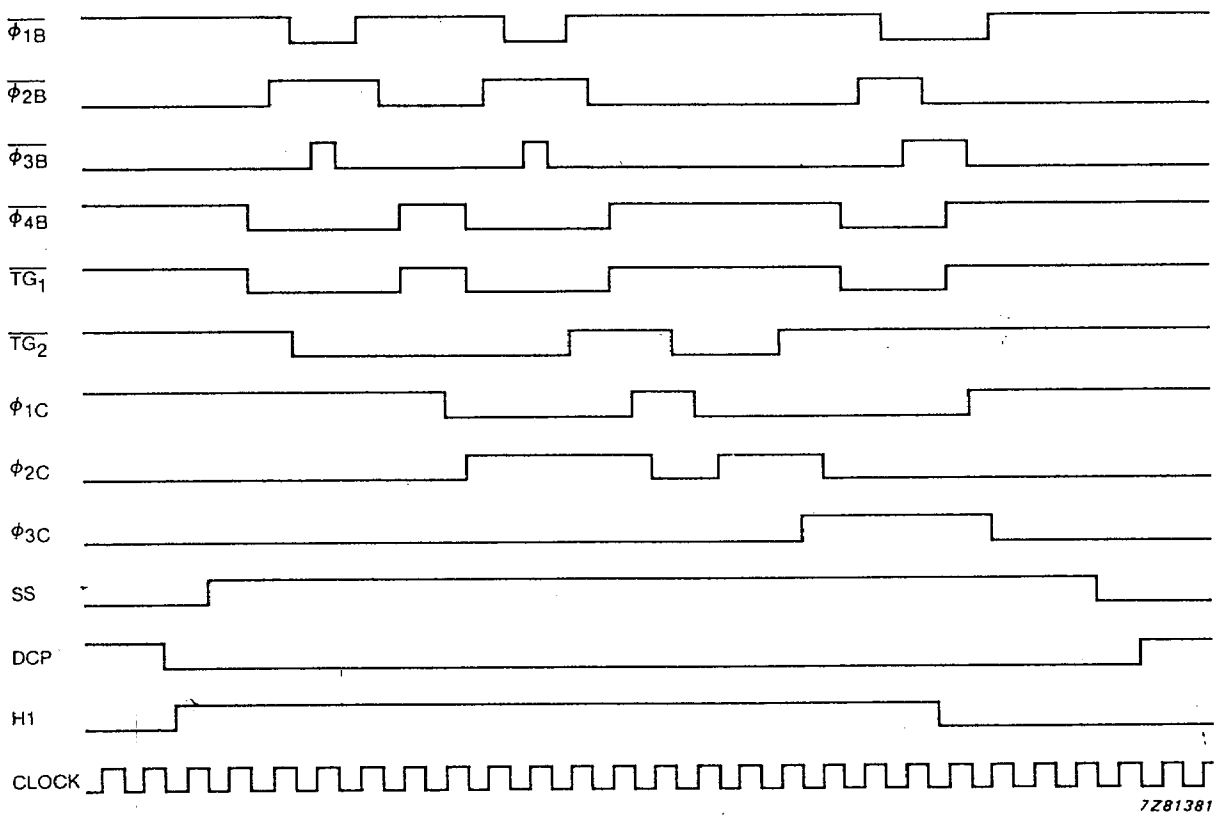
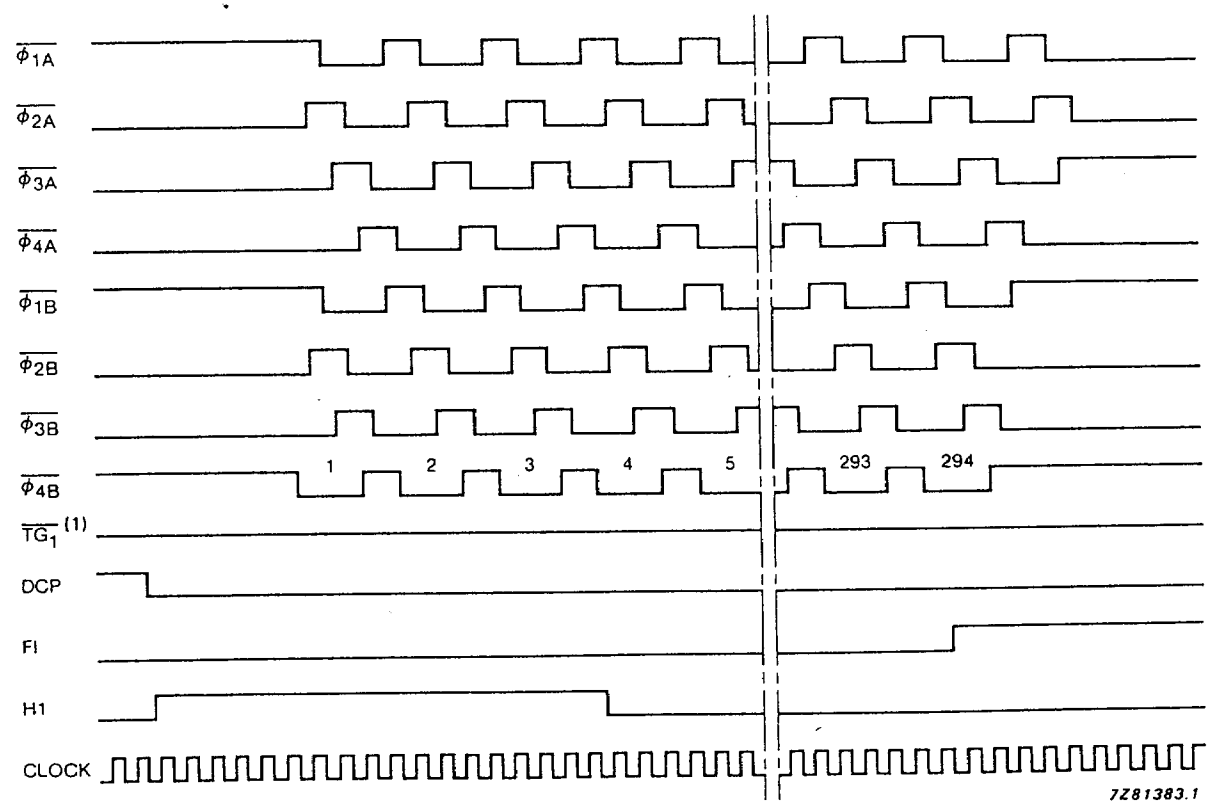
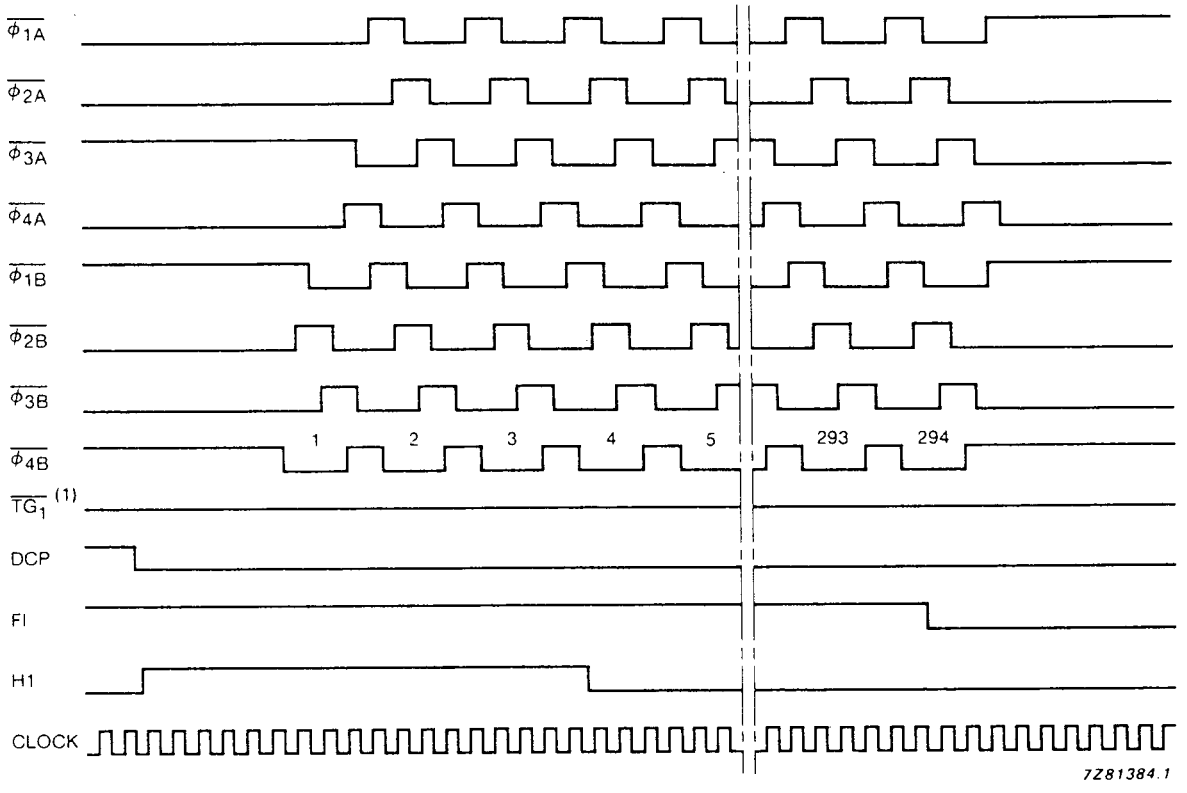


Fig.3 Line transport (625 lines).



(1) $\overline{TG_1}$ = HIGH state.

Fig.4 Image sensor transport, field 2 (625 lines).



(1) $\overline{TG_1}$ = HIGH state.

Fig.5 Image sensor transport, field 1 (625 lines).

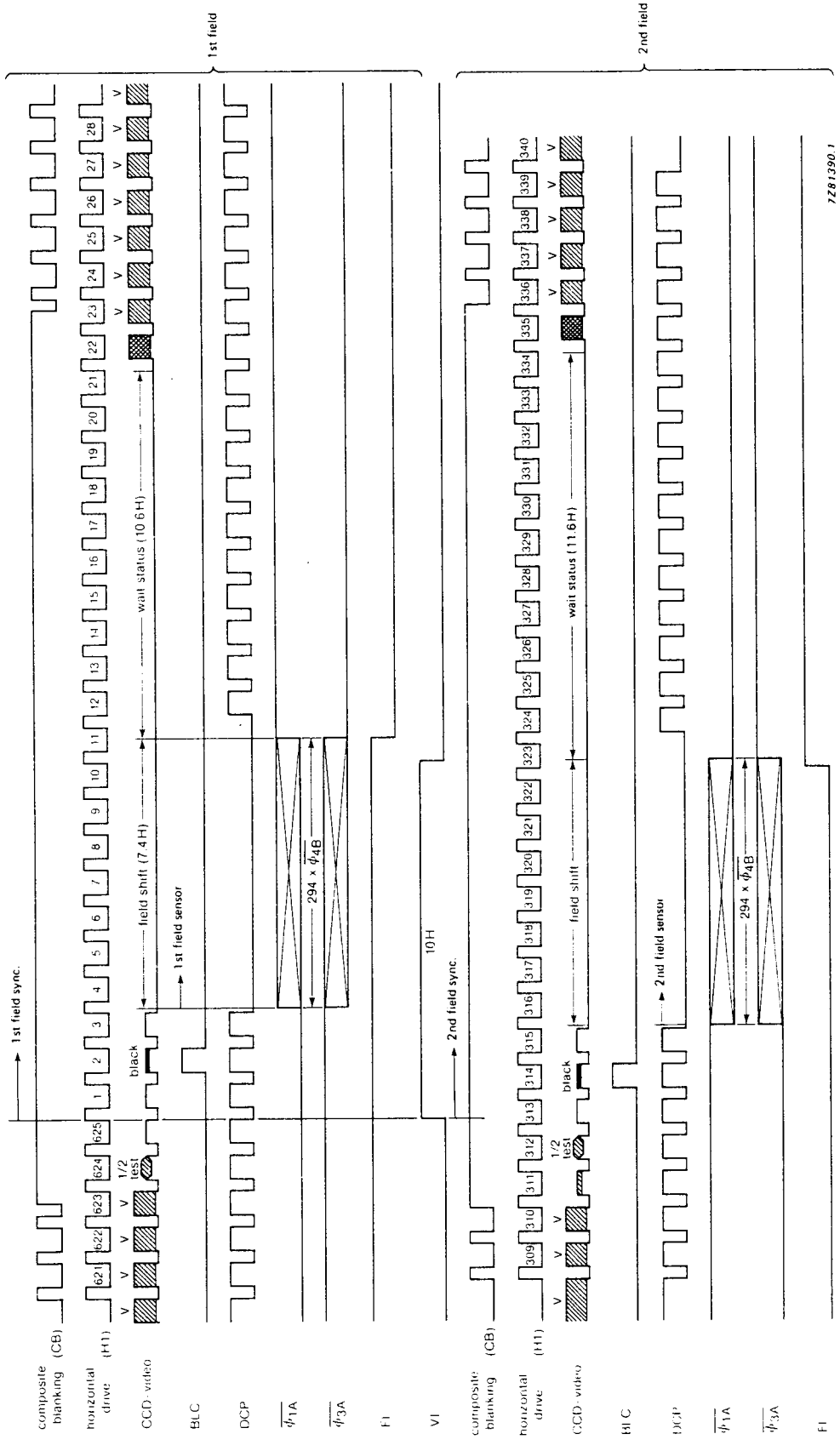


Fig.6 Pulse pattern during field blanking (625 lines).

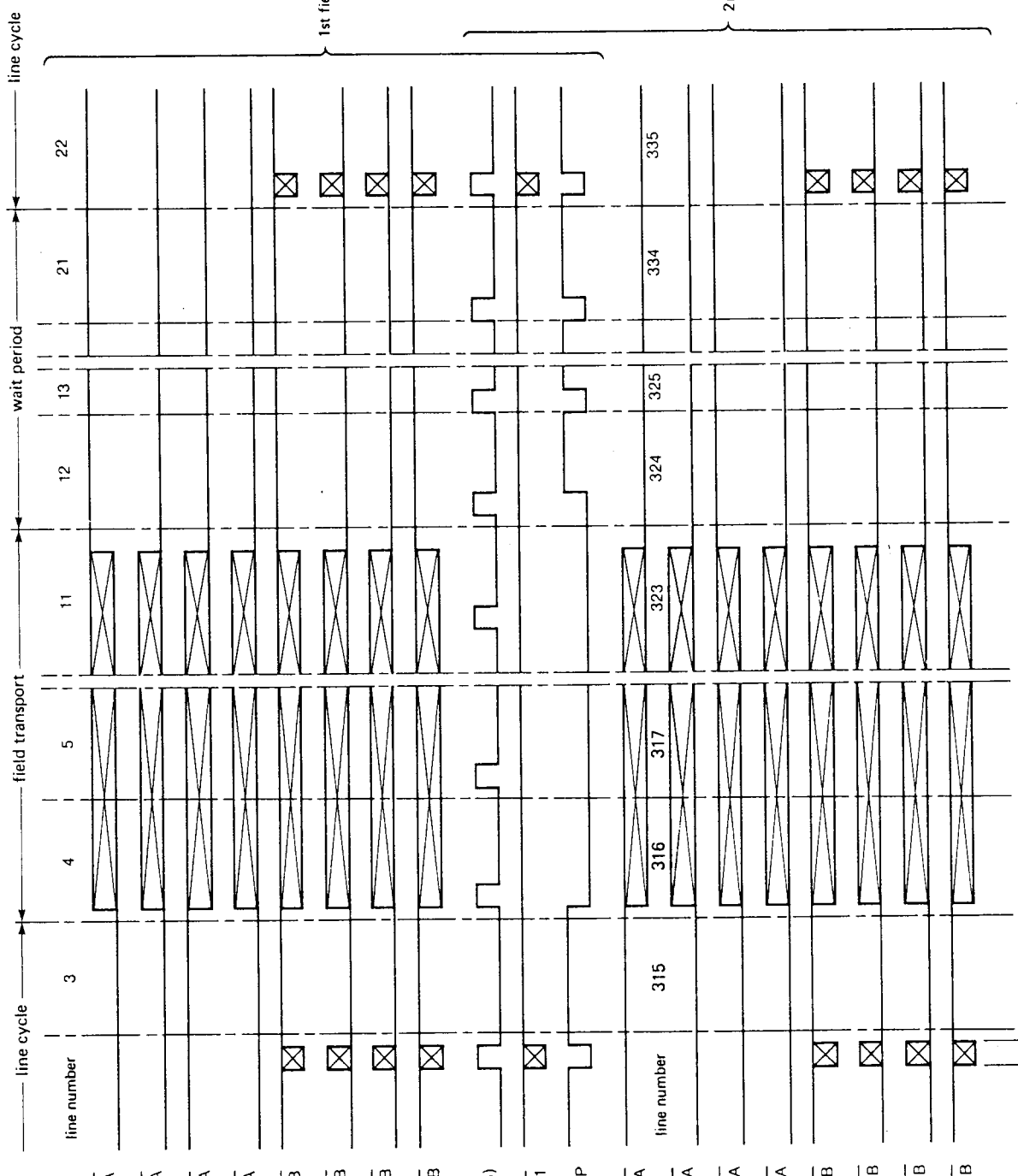


Fig.7 MNPPG cycles during field blanking (625 lines).

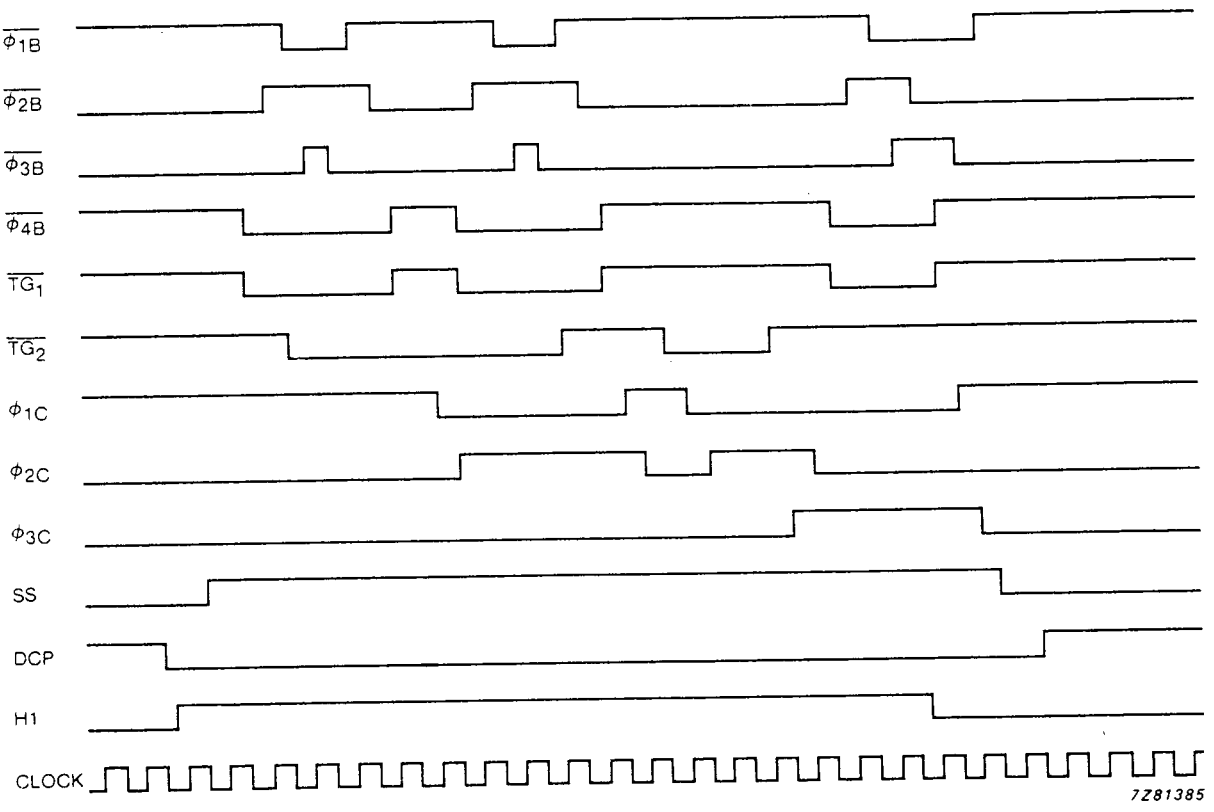
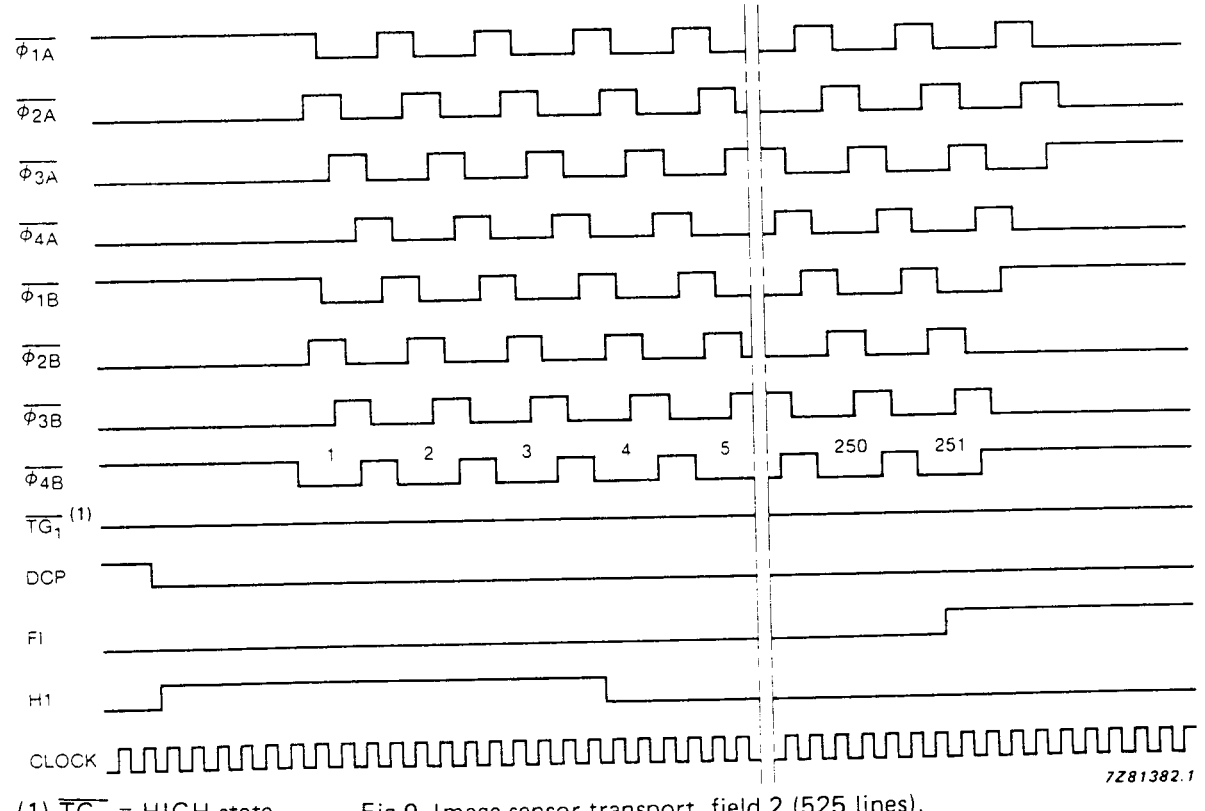
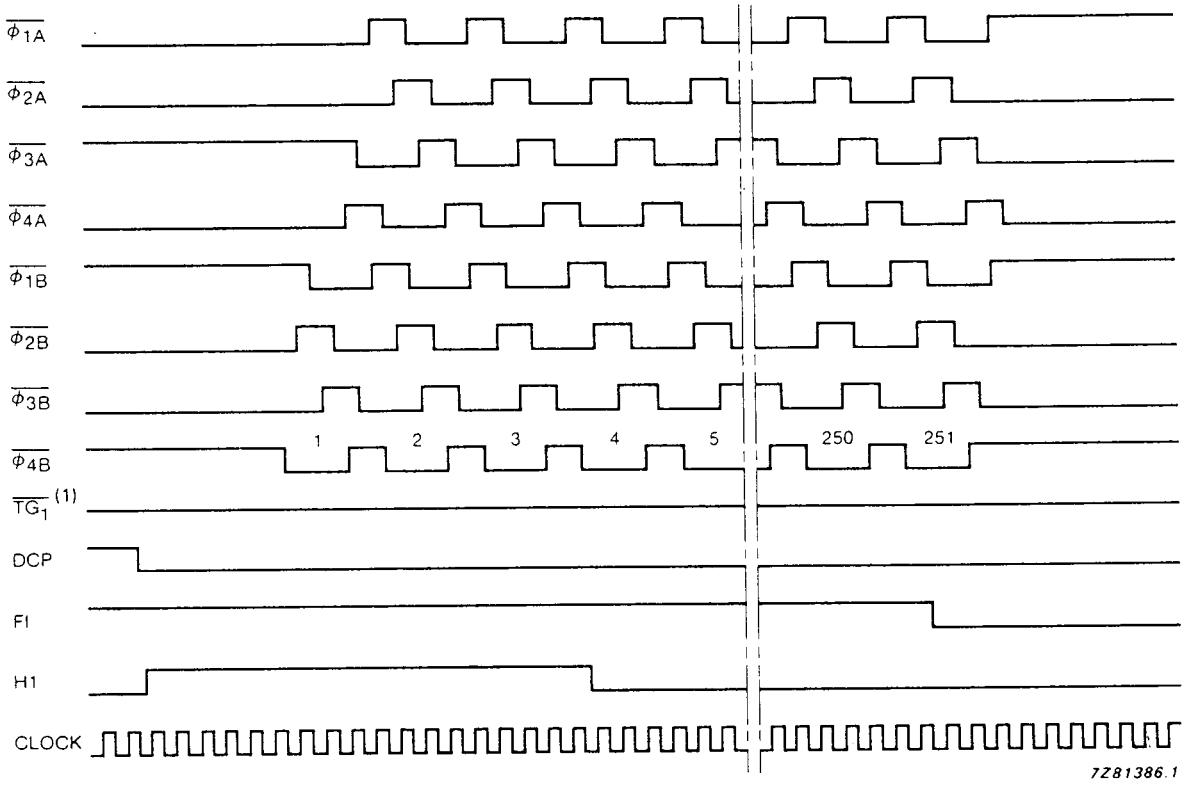


Fig.8 Line transport (525 lines).



(1) $\overline{TG_1}$ = HIGH state.

Fig.9 Image sensor transport, field 2 (525 lines).



(1) $\overline{TG_1}$ = HIGH state.

Fig.10 Image sensor transport, field 1 (525 lines).

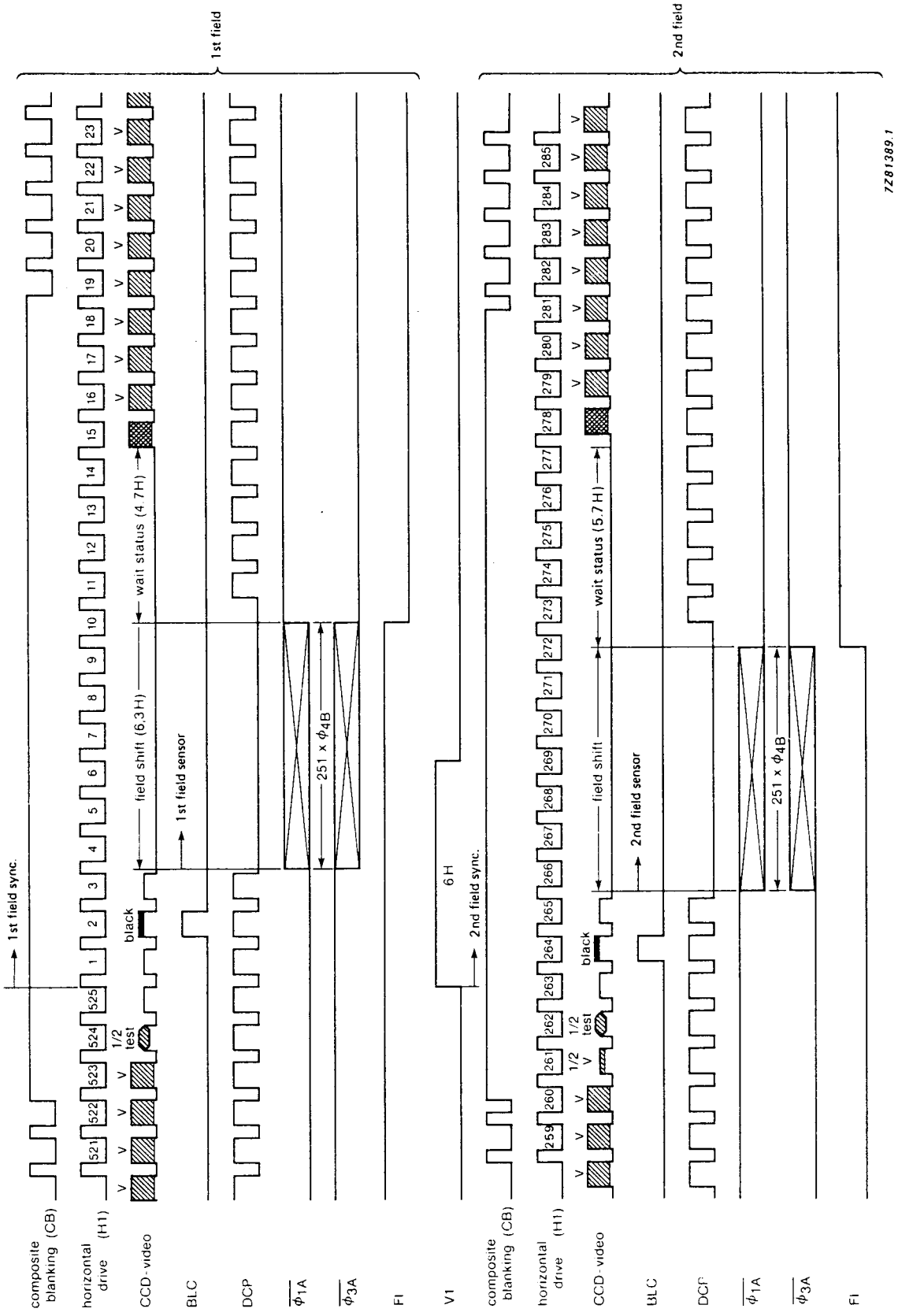


Fig.11 Pulse pattern during field blanking (525 lines

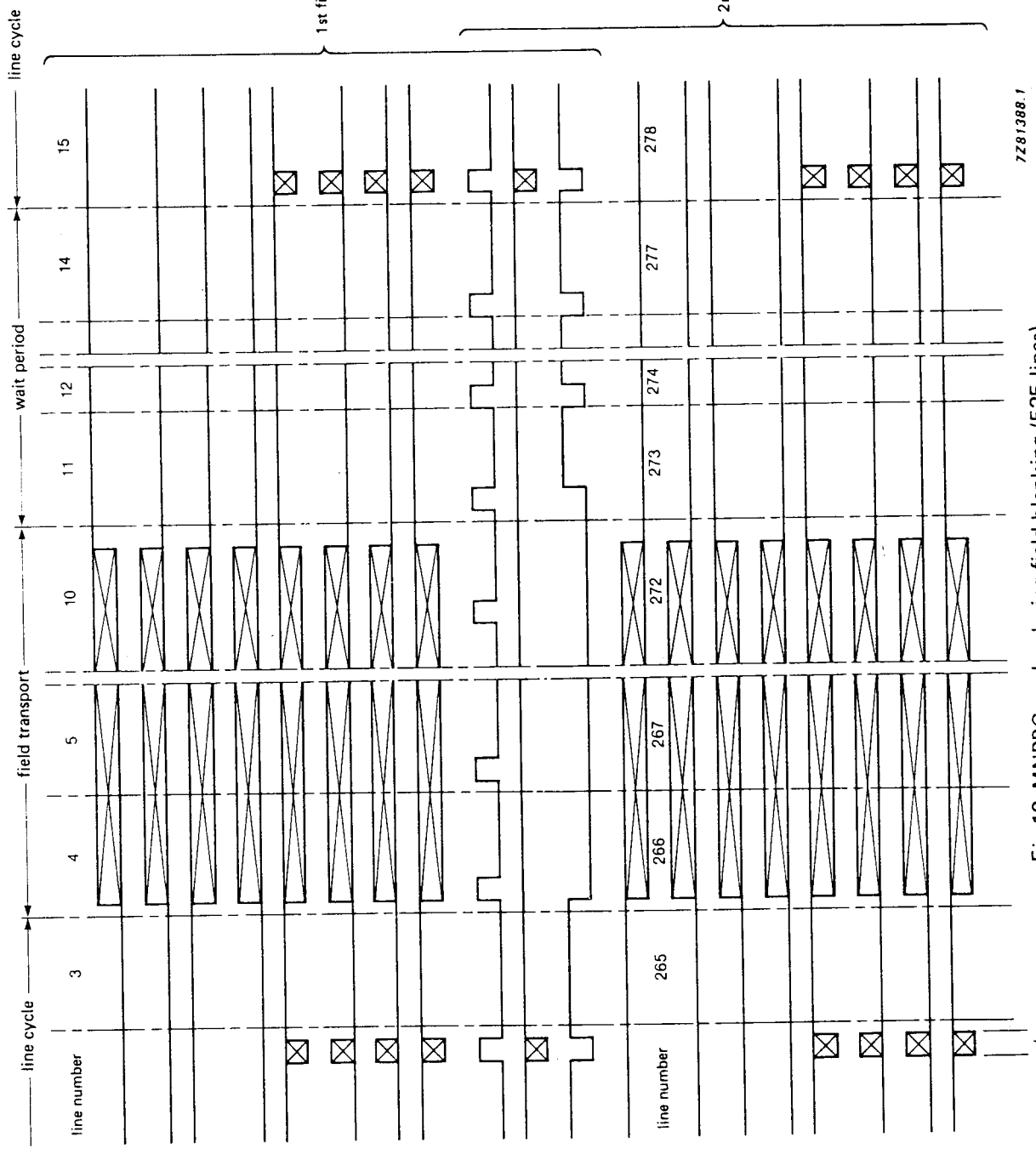


Fig.12 MNPPG cycles during field blanking (525 lines).