Integrated Device Technology, Inc.

RISC CPU PROCESSOR

IDT79R3000A
IDT79R3000AE

FEATURES:

- Enhanced instruction set compatible version of the IDT79R2000, IDT79R3000 RISC CPUs.
- Upwardly pin-compatible with IDT79R3000 RISC CPU.
- IDT79R3000A "E" version relaxes system memory timing requirements in a high-speed systems.
- Full 32-bit Operation—Thirty-two 32-bit registers and all instructions and addresses are 32-bit.
- Efficient Pipelining—The CPU's 5-stage pipeline design assists in obtaining an execution rate approaching one instruction per cycle. Pipeline stalls and exceptions are handled precisely and efficiently.
- On-Chip Cache Control—The IDT79R3000A provides a high-bandwidth memory interface that handles separate external Instruction and Data Caches ranging in size from 4 to 256kB each. Both caches are accessed during a single CPU cycle. All cache control is on-chip.
- On-Chip Memory Management Unit—A fully-associative, 64-entry Translation Look-aside Buffer (TLB) provides fast address translation for virtual-to-physical memory mapping of the 4gB virtual address space.
- Dynamically able to switch between Big- and Little-Endian byte ordering conventions.
- Coprocessor Interface—The IDT79R3000A generates all addresses and handles memory interface control for up to three additional tightly coupled external processors.
- Optimizing Compilers are available for C, Fortran, Pascal, COBOL, Ada, PL/1, and C++.
- UNIX™ System V.4 and BSD 4.3 operating systems supported.
- High-speed CMOS technology.
- 16.7 through 40MHz clock rates yield up to 32VUPS sustained throughput.
- Supports independent multi-word block refill of both the instruction and data caches with variable block sizes.
- Supports concurrent refill and execution of instructions.
- Partial word stores executed as read-modify-write operations.
- 6 external interrupt inputs, 2 software interrupts, with single cycle latency to exception handler routine.
- Flexible multiprocessing support on chip with no impact on uniprocessor designs.

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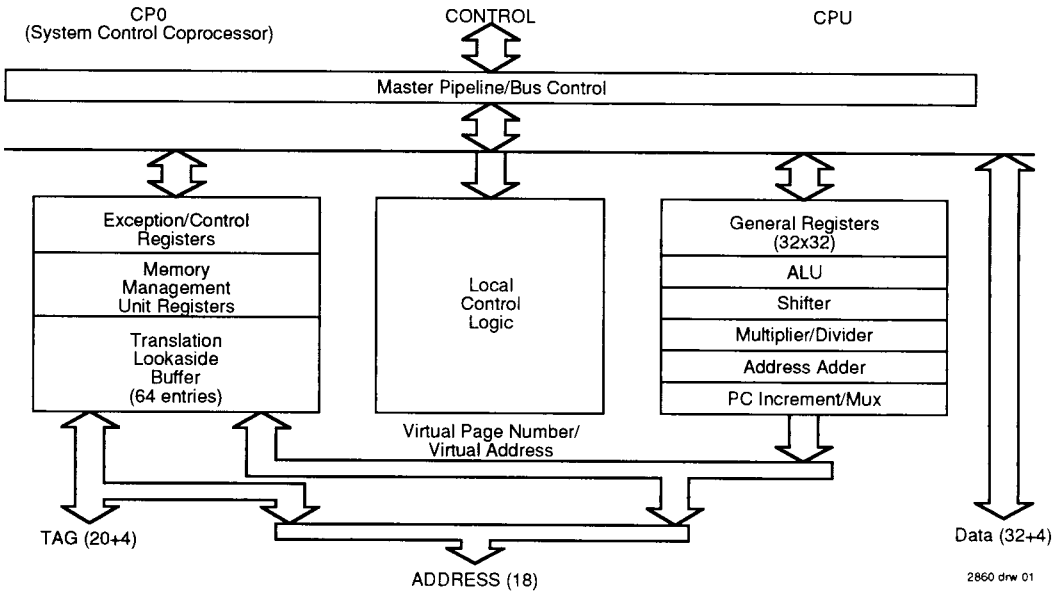
IDT79R3000A PROCESSOR BLOCK DIAGRAM



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DESCRIPTION

The IDT79R3000A RISC Microprocessor consists of two tightly-coupled processors integrated on a single chip. The first processor is a full 32-bit CPU based on RISC (Reduced Instruction Set Computer) principles to achieve a new standard of microprocessor performance. The second processor is a system control coprocessor, called CP0, containing a fully-associative 64-entry TLB (Translation Look-aside Buffer), MMU (Memory Management Unit) and control registers, supporting a 4gB virtual memory subsystem, and a Harvard Architecture Cache Controller achieving a bandwidth of 320mB/second using industry standard static RAMs.

This data sheet provides an overview of the features and architecture of the IDT79R3000A CPU, Revision 3.0. A more detailed description of the operation of the device is incorporated in the *IDT79R3000A Family Hardware User Manual*, and a more detailed architectural overview is provided in the *MIPS RISC Architecture* book, both available from IDT. Documentation providing details of the software and development environments supporting this processor are also available from IDT.

IDT79R3000A CPU Registers

The IDT79R3000A CPU provides 32 general-purpose 32-bit registers, a 32-bit Program Counter, and two 32-bit registers that hold the results of integer multiply and divide operations. Only two of the 32 general registers have a special purpose: register r0 is hard-wired to the value "0", which is a useful constant, and register r31 is used as the link register in jump-and-link instructions (return address for subroutine calls).

The CPU registers are shown in Figure 2. Note that there is no Program Status Word (PSW) register shown in this figure: the functions traditionally provided by a PSW register are instead provided in the Status and Cause registers incorporated within the System Control Coprocessor (CP0).

Instruction Set Overview

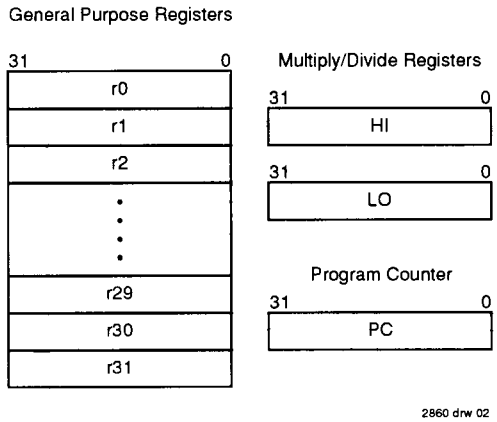

Figure 2. IDT79R3000A CPU Registers

All IDT79R3000A instructions are 32 bits long, and there are only three instruction formats. This approach simplifies instruction decoding, thus minimizing instruction execution time. The IDT79R3000A processor initiates a new instruction on every run cycle, and is able to complete an instruction on almost every clock cycle. The only exceptions are the Load instructions and Branch instructions, which each have a single cycle of latency associated with their execution. Note, however, that in the majority of cases the compilers are able to fill these latency cycles with useful instructions which do not require the result of the previous instruction. This effectively eliminates these latency effects.

The actual instruction set of the CPU was determined after extensive simulations to determine which instructions should be implemented in hardware, and which operations are best synthesized in software from other basic instructions. This methodology resulted in the IDT79R3000A having the highest performance of any available microprocessor.

The IDT79R3000A instruction set can be divided into the following groups:

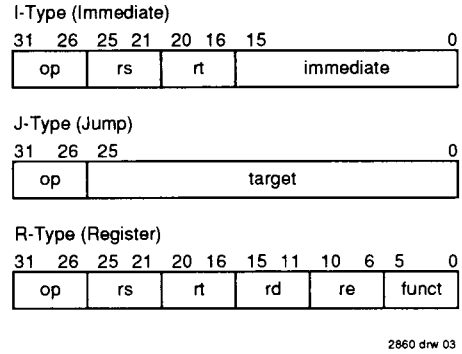

Figure 3. IDT79R3000A Instruction Formats

- **Load/Store** instructions move data between memory and general registers. They are all I-type instructions, since the only addressing mode supported is base register plus 16-bit, signed immediate offset.

  The Load instruction has a single cycle of latency, which means that the data being loaded is not available to the instruction immediately after the load instruction. The compiler will fill this delay slot with either an instruction which is not dependent on the loaded data, or with a NOP instruction. There is no latency associated with the store instruction.

  Loads and Stores can be performed on byte, half-word, word, or unaligned word data (32-bit data not aligned on a modulo-4 address). The CPU cache is constructed as a write-through cache.
- **Computational** instructions perform arithmetic, logical and shift operations on values in registers. They occur in both R-type (both operands and the result are registers) and I-type (one operand is a 16-bit immediate) formats.

Note that computational instructions are three operand instructions; that is, the result of the operation can be stored into a different register than either of the two operands. This means that operands need not be overwritten by arithmetic operations. This results in a more efficient use of the large register set.

- **Jump and Branch** instructions change the control flow of a program. Jumps are always to a paged absolute address formed by combining a 26-bit target with four bits of the Program counter (J-type format, for subroutine calls), or 32-bit register byte addresses (R-type, for returns and dispatches). Branches have 16-bit offsets relative to the program counter (I-type). Jump and Link instructions save a return address in Register 31. The IDT79R3000A instruction set features a number of branch conditions. Included is the ability to compare a register to zero and branch, and also the ability to branch based on a comparison between two registers. Thus, net performance is increased since software does not have to perform arithmetic instructions prior to the branch to set up the branch conditions.
- **Coprocessor** instructions perform operations in the coprocessors. Coprocessor Loads and Stores are I-type. Coprocessor computational instructions have coprocessor-dependent formats (see coprocessor manuals).
- **Coprocessor 0** instructions perform operations on the System Control Coprocessor (CP0) registers to manipulate the memory management and exception handling facilities of the processor.
- **Special** instructions perform a variety of tasks, including movement of data between special and general registers, system calls, and breakpoint. They are always R-type.

Table 1 lists the instruction set of the IDT79R3000A processor.

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IDT79R3000A INSTRUCTION SUMMARY

OP	Description	OP	Description
	Load/Store Instructions		**Multiply/Divide Instructions**
LB	Load Byte	MULT	Multiply
LBU	Load Byte Unsigned	MULTU	Multiply Unsigned
LH	Load Halfword	DIV	Divide
LHU	Load Halfword Unsigned	DIVU	Divide Unsigned
LW	Load Word	MFHI	Move From HI
LWL	Load Word Left	MTHI	Move To HI
LWR	Load Word Right	MFLO	Move From LO
SB	Store Byte	MTLO	Move To LO
SH	Store Halfword		
SW	Store Word		**Jump and Branch Instructions**
SWL	Store Word Left	J	Jump
SWR	Store Word Right	JAL	Jump and Link
		JR	Jump to Register
	Arithmetic Instructions	JALR	Jump and Link Register
	(ALU Immediate)	BEQ	Branch on Equal
ADDI	Add Immediate	BNE	Branch on Not Equal
ADDIU	Add Immediate Unsigned	BLEZ	Branch on Less than or Equal to Zero
SLTI	Set on Less Than Immediate	BGTZ	Branch on Greater Than Zero
SLTIU	Set on Less Than Immediate Unsigned	BLTZ	Branch on Less Than Zero
		BGEZ	Branch on Greater than or Equal to Zero
ANDI	AND Immediate		
ORI	OR Immediate	BLTZAL	Branch on Less Than Zero and Link
XORI	Exclusive OR Immediate	BGEZAL	Branch on Greater than or Equal to Zero and Link
LUI	Load Upper Immediate		
			Special Instructions
	Arithmetic Instructions	SYSCALL	System Call
	(3-operand, register-type)	BREAK	Break
ADD	Add		
ADDU	Add Unsigned		**Coprocessor Instructions**
SUB	Subtract	LWCz	Load Word from Coprocessor
SUBU	Subtract Unsigned	SWCz	Store Word to Coprocessor
SLT	Set on Less Than	MTCz	Move To Coprocessor
		MFCz	Move From Coprocessor
SLTU	Set on Less Than Unsigned	CTCz	Move Control to Coprocessor
AND	AND	CFCz	Move Control From Coprocessor
OR	OR	COPz	Coprocessor Operation
XOR	Exclusive OR	BCzT	Branch on Coprocessor z True
NOR	NOR	BCzF	Branch on Coprocessor z False
	Shift Instructions		**System Control Coprocessor**
SLL	Shift Left Logical		**(CP0) Instructions**
SRL	Shift Right Logical	MTC0	Move To CP_0
SRA	Shift Right Arithmetic	MFC0	Move From CP_0
SLLV	Shift Left Logical Variable	TLBR	Read indexed TLB entry
SRLV	Shift Right Logical Variable	TLBWI	Write Indexed TLB entry
SRAV	Shift Right Arithmetic Variable	TLBWR	Write Random TLB entry
		TLBP	Probe TLB for matching entry
		RFE	Restore From Exception

2860 tbl 01

IDT79R3000A System Control Coprocessor (CP0)

The IDT79R3000A can operate with up to four tightly-coupled coprocessors (designated CP0 through CP3). The System Control Coprocessor (or CP0), is incorporated on the IDT79R3000 chip and supports the virtual memory system and exception handling functions of the IDT79R3000A. The virtual memory system is implemented using a Translation Look-aside Buffer and a group of programmable registers as shown in Figure 4.

SYSTEM CONTROL COPROCESSOR (CP0) REGISTERS

The CP0 registers shown in Figure 4 are used to control the memory management and exception handling capabilities of the IDT79R3000A. Table 2 provides a brief description of each register.

SYSTEM CONTROL COPROCESSOR (CPO) REGISTERS

Register	Description
EntryHi	HIGH half of a TLB entry
EntryLo	LOW half of a TLB entry
Index	Programmable pointer into TLB array
Random	Pseudo-random pointer into TLB array
Status	Mode, interrupt enables, and diagnostic status info
Cause	Indicates nature of last exception
EPC	Exception Program Counter
Context	Pointer into kernel's virtual Page Table Entry array
BadVA	Most recent bad virtual address
PRId	Processor revision identification (Read only)

2860 tbl 02

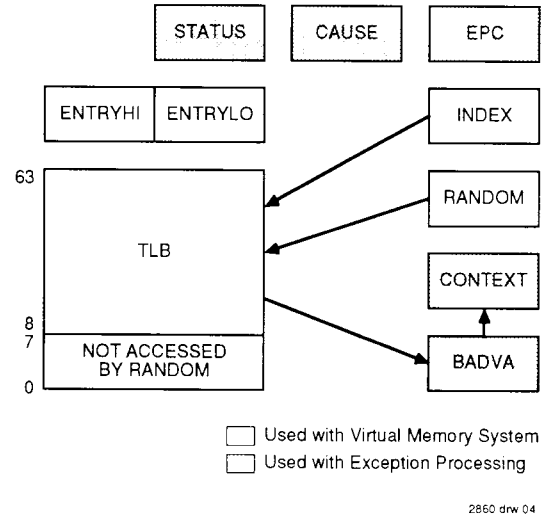


Figure 4. The System Coprocessor Registers

Memory Management System

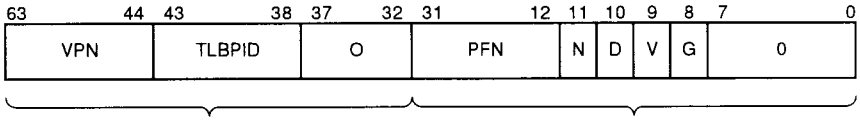
The IDT79R3000A has an addressing range of 4gB. However, since most IDT79R3000A systems implement a physical memory smaller than 4gB, the IDT79R3000A provides for the logical expansion of memory space by translating addresses composed in a large virtual address space into available physical memory address. The 4gB address space is divided into 2gB which can be accessed by both the users and the kernel, and 2gB for the kernel only.

The TLB (Translation Lookaside Buffer)

Virtual memory mapping is assisted by the Translation Lookaside Buffer (TLB). The on-chip TLB provides very fast virtual memory access and is well-matched to the requirements of multi-tasking operating systems. The fully-associative TLB contains 64 entries, each of which maps a 4kB page, with controls for read/write access, cacheability, and process identification. The TLB allows each user to access up to 2gB of virtual address space.

Figure 5 illustrates the format of each TLB entry. The Translation operation involves matching the current Process ID (PID) and upper 20 bits of the address against PID and VPN (Virtual Page Number) fields in the TLB. When both match (or the TLB entry is Global), the VPN is replaced with the PFN (Physical Frame Number) to form the physical address.

TLB misses are handled in software, with the entry to be replaced determined by as imple RANDOM function. The routine to process a TLB miss in the UNIX environment requires only 10-12 cycles, which compares favorably with many CPUs which perform the operation in hardware.



VPN – Virtual Page Number
TLBPID – Process ID
PFN – Physical Frame Number
N – Non-cacheable flag
D – Dirty flag (Write protect)
V – Valid entry flag
G – Global flag (ignore PID)
0 – Reserved

2860 drw 05

Figure 5. TLB Entry Format

IDT79R3000 Operating Modes

The IDT79R3000A has two operating modes: User mode and Kernel/mode. The IDT79R3000A normally operates in the User mode until an exception is detected forcing it into the Kernel mode. It remains in the Kernel mode until a Restore From Exception (RFE) instruction is executed. The manner in which memory addresses are translated or mapped depends on the operating mode of the IDT79R3000A (Figure 6) shows the MMU translation performed for each of the operating modes.

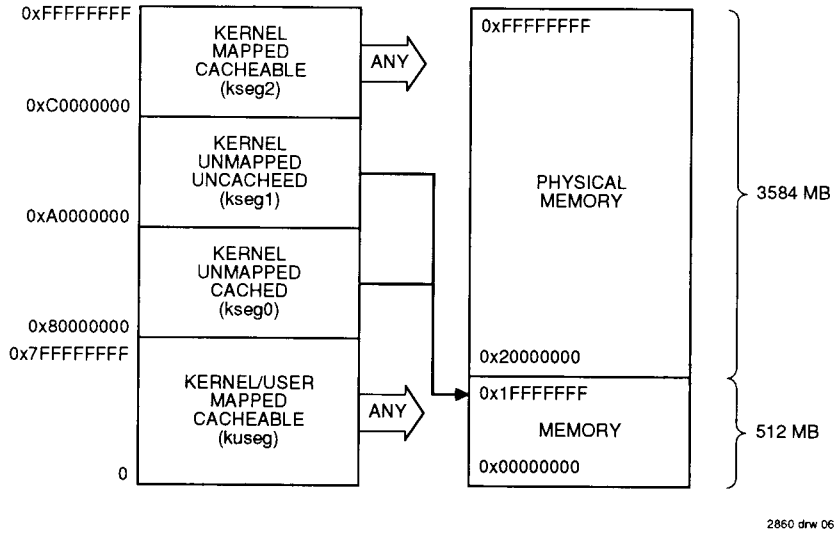


Figure 6. IDT79R3000A Virtual Address Mapping

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User Mode—in this mode, a single, uniform virtual address space (kuseg) of 2gB is available. Each virtual address is extended with a 6-bit process identifier field to form unique virtual addresses. All references to this segment are mapped through the TLB. Use of the cache for up to 64 processes is determined by bit settings for each page within the TLB entries.

Kernel Mode—four separate segments are defined in this mode:

- *kuseg*—when in the kernel mode, references to this segment are treated just like user mode references, thus streamlining kernel access to user data.
- *kseg0*—references to this 512mB segment use cache memory but are not mapped through the TLB. Instead, they always map to the first 0.5gB of physical address space.
- *kseg1*—references to this 512mB segment are not mapped through the TLB and do not use the cache. Instead, they are hard-mapped into the same 0.5gB segment of physical address space as kseg0.
- *kseg2*—references to this 1gB segment are always mapped through the TLB and use of the cache is determined by bit settings within the TLB entries.

IDT79R3000 Pipeline Architecture

The execution of a single IDT79R3000A instruction consists of five primary steps:

1) **IF** — Fetch the instruction (I-Cache).
2) **RD** — Read any required operands from CPU registers while decoding the instruction.
3) **ALU** — Perform the required operation on instruction operands.
4) **MEM**— Access memory (D-Cache).
5) **WB** — Write back results to register file.

Each of these steps requires approximately one CPU cycle, as shown in Figure 7 (parts of some operations overlap into another cycle while other operations require only 1/2 cycle).

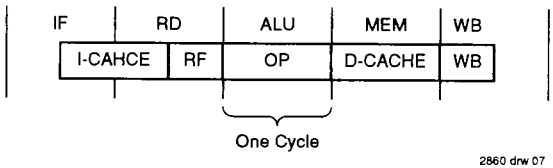

Figure 7. IDT79R3000A Instruction Pipeline

INSTRUCTION EXECUTION

The IDT79R3000A uses a 5-stage pipeline to achieve an instruction execution rate approaching one instruction per CPU cycle. Thus, execution of five instructions at a time are overlapped as shown in Figure 8.

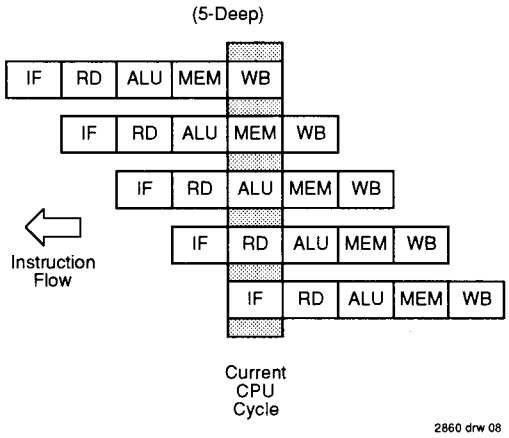

Figure 8. IDT79R3000A Execution Sequence

This pipeline operates efficiently because different CPU resources (address and data bus accesses, ALU operations, register accesses, and so on) are utilized on a non-interfering basis.

Memory System Hierarchy

The high performance capabilities of the IDT79R3000A processor demand system configurations incorporating techniques frequently employed in large, mainframe computers but seldom encountered in systems based on more traditional microprocessors.

A primary goal of systems employing RISC techniques is to minimize the average number of cycles each instruction requires for execution. In order to achieve this goal, RISC processors incorporate a number of RISC techniques, including a compact and uniform instruction set, a deep instruction pipeline (as described above), and utilization of optimizing compilers. Many of the advantages obtained from these techniques can, however, be negated by an inefficient memory system.

Figure 9 illustrates memory in a simple microprocessor system. In this system, the CPU outputs addresses to memory and reads instructions and data from memory or writes data to memory. The address space is completely undifferentiated: instructions, data, and I/O devices are all treated the same. In such a system, a primary limiting performance factor is memory bandwidth.

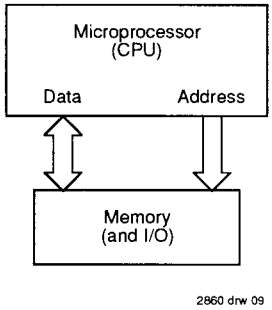

Figure 9. A Simple Microprocessor Memory System

Figure 10 illustrates a memory system that supports the significantly greater memory bandwidth required to take full advantage of the IDT79R3000A's performance capabilities. The key features of this system are:

- **External Cache Memory**—Local, high-speed memory (called cache memory) is used to hold instructions and data that is repetitively accessed by the CPU (for example, within a program loop) and thus reduces the number of references that must be made to the slower-speed main

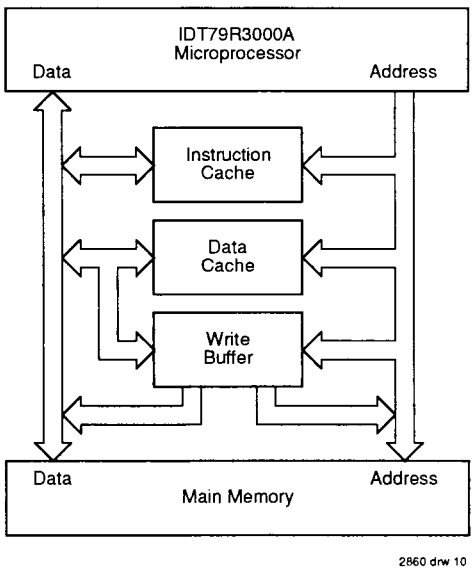

Figure 10. An IDT79R3000A System with a High-Performance Memory System

memory. Some microprocessors provide a limited amount of cache memory on the CPU chip itself. The external caches supported by the IDT79R3000A can be much larger; while a small cache can improve performance of some programs, significant improvements for a wide range of programs require large caches.

- **Separate Caches for data and Instructions**—Even with high-speed caches, memory speed can still be a limiting factor because of the fast cycle time of a high-performance microprocessor. The IDT79R3000A supports separate caches for instructions and data and alternates accesses of the two caches during each CPU cycle. Thus, the processor can obtain data and instructions at the cycle rate of the CPU using caches constructed with commercially available IDT static RAM devices.
  In order to maximize bandwidth in the cache while minimizing the requirement for SRAM access speed, the IDT79R3000A divides a single-processor clock cycle into two phases. During one phase, the address for the data cache access is presented while data previously addressed in the instruction cache is read; during the next phase, the data operation is completed while the instruction cache is being addressed. Thus, both caches are read in a single processor cycle using only one set of address and data pins.

- **Write Buffer**—in order to ensure data consistency, all data that is written to the data cache must also be written out to main memory. The cache write model used by the IDT79R3000A is that of a write-through cache; that is, all data written by the CPU is immediately written into the main memory. To relieve the CPU of this responsibility (and the inherent performance burden) the IDT79R3000A supports an interface to a write buffer. The IDT79R3020 Write Buffer captures data (and associated addresses) output by the CPU and ensures that the data is passed on to main memory.

IDT79R3000A Processor Subsystem Interfaces

Figure 11 illustrates the three subsystem interfaces provided by the IDT79R3000A processor:

- **Cache control** interface (on-chip) for separate data and instruction caches permits implementation of off-chip caches using standard IDT SRAM devices. The IDT79R3000A directly controls the cache memory with a minimum of external components. Both the instruction and data cache can vary from 0 to 256kB (64K entries). The IDT79R3000A also includes the TAG control logic which determines whether or not the entry read from the cache is the desired data. The IDT79R3000A cache controller implements a direct mapped cache for high net performance (bandwidth). It has the ability to refill multiple words when a cache miss occurs, thus reducing the effective miss rate to less than 2% for large caches. When a cache miss occurs, the IDT79R3000A can support refilling the cache in 1, 4, 8, 16, or 32-word blocks to minimize the effective penalty of having to access main memory. The IDT79R3000A also incorporates the ability to perform instruction streaming; while the cache is refilling, the processor can resume execution once the missed word is obtained from main memory. In this way, the processor can continue to execute concurrently with the cache block refill.
- **Memory controller** interface for system (main) memory. This interface also includes the logic and signals to allow operation with a write buffer to further improve memory bandwidth. In addition to the standard full word access, the memory controller supports the ability to write bytes and half-words by using partial word operations. The memory controller also supports the ability to retry memory accesses if, for example, the data returned from memory is invalid and a bus error needs to be signalled.
- **Coprocessor Interface**—The IDT79R3000A features a tightly coupled co-processor interface in which all co-processors maintain synchronization with the main processor; reside on the same data bus as the main processor; and participate in bus transactions in an identical manner to the main processor. The IDT79R3000A generates all required cache and memory control signals, including cache and memory addresses for attached coprocessors. As a result, only the data bus and a few control signals need to be connected to a coprocessor.
  The interface supports three types of coprocessor instructions: loads/stores, coprocessor operations, and processor-coprocessor transfers. Note that coprocessor loads and stores occur directly between the coprocessor and memory, without requiring the data to go through the CPU. Synchronization between the CPU and external coprocessors is achieved using a Phased-Lock Loop interface to the coprocessor. The coprocessor physical interface also includes coprocessor condition signals (CpCond(n)), which are used in coprocessor branch instructions, and a coprocessor busy signal (CpBusy) which is used to stall the CPU if the coprocessor needs to hold off subsequent operations.

  Finally, a precise exception interface is defined between the CPU and coprocessors using the external interrupt inputs of the CPU. This allows a coprocessor exception, even if it was the result of a multi-cycle operation, to be traced to the precise coprocessor operation which caused it. This is an important feature for languages which can define specific error handlers for each task.
  The interface supports up to four separate coprocessors. Coprocessor 0 is defined to be the system control coprocessor, and resides on the same chip as the CPU unit. Coprocessor 1 is the Floating Point Accelerator, IDT79R3010A. Coprocessors 2 and 3 are available to support an interface to application specific functions.

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MULTIPROCESSING SUPPORT

The IDT79R3000A supports multiprocessing applications in a simple but effective way. Multiprocessing applications require cache coherency across the multiple processors. The IDT79R3000A offers two signals to support cache coherency: the first, MPStall, stalls the processor within two cycles of being received and keeps it from accessing the cache. This allows an external agent to snoop into the processor data cache. The second signal, MPInvalidate, causes the processor to write data on the data cache bus which indicates the externally addressed cache entry is invalid. Thus, a subsequent access to that location would result in a cache miss, and the data would be obtained from main memory.

The two MP signals would be generated by a external logic which utilizes a secondary cache to perform bus snooping functions. The IDT79R3000A does not impose an architecture for this secondary cache, but rather is flexible enough to support a variety of application specific architecture stand still maintain cache coherency. Further, there is no impact on designs which do not require this feature. The IDT79R3000A has further improved on the microprocessor support found in the IDT79R3000, by allowing the use of cache RAMs with internal address latches in multiprocessor systems.

ADVANCED FEATURES

The IDT79R3000A offers a number of additional features such as the ability to swap the instruction and data caches, facilitating diagnostics and cache flushing. Another feature isolates the caches, which forces cache hits to occur regardless of the contents of the tag fields. The IDT79R3000A allows the processor to execute user tasks of the opposite byte ordering (endianness) of the operating system, and further allows parity checking to be disabled. More details on these features can be found in the IDT79R3000A Family Hardware User's Manual.

Further features of the IDT79R3000A are configured during the last four cycles prior to the negation of the RESET input. These functions include the ability to select cache sizes and cache refill block sizes; the ability to utilize the multiprocessor interface; whether or not instruction streaming is enabled; whether byte ordering follows "Big-Endian" or "Little-Endian" protocols, etc. Table 3 shows the configuration options selected at Reset. These are further discussed in the *Hardware User's Manual.*

BACKWARD COMPATIBILITY WITH IDT79R2000

The IDT79R3000A can be used in sockets designed for the IDT79R3000. The pin-out of the IDT79R3000A has been selected to ensure this compatibility, with new functions mapped onto previously unused pins. The instruction set is compatible with that of the IDT79R2000 at the binary level. As a result, code written for the older processor can be executed. New features can be selectively disabled.

In most IDT79R3000 applications, the IDT79R3000A can be placed in the socket with no modification to initialization settings. Further application assistance on this topic is available from IDT.

PACKAGE THERMAL SPECIFICATIONS

The IDT79R3000A utilizes special packaging techniques to improve both the thermal and electrical characteristics of the microprocessor.

In order to improve the electrical characteristics of the device, the package is constructed using multiple signal planes, including individual power planes and ground planes to reduce noise associated with high-frequency TTL parts. In addition, the 175-pin PGA package utilizes extra power and ground pins to reduce the inductance from the internal power planes to the power planes of the PC Board.

In order to improve the electrical characteristics of the microprocessor, the device is housed using cavity down packaging. In addition, these packages incorporate a copper-tungsten thermal slug designed to efficiently transfer heat from the die to the case of the package, and thus effectively lower the thermal resistance of the package. The use of an additional external heat sink affixed to the package thermal slug further decreases the effective thermal resistance of the package.

The case temperature may be measured in any environment to determine whether the device is within the specified operating range. The case temperature should be measured at the center of the top surface opposite the package cavity (the package cavity is the side where the package lid is mounted).

The equivalent allowable ambient temperature, T_A, can be calculated using the thermal resistance from case to ambient (θ_{ca}) for the given package. The following equation relates ambient and case temperature:

$$T_A = T_c - P * \theta_{ca}$$

where P is the maximum power consumption, calculated by using the maximum Icc from the DC Electrical Characteristics section.

Typical values for θ_{ca} at various airflows are shown in table 4 for various CPU packages.

R3000A PACKAGE CHARACTERISTICS

	Airflow - (ft/min)					
0	200	400	600	800	1000	
Øca (175-PGA, 144-PGA)	21	7	3	2	1	0.5
Øca (172 Quad Flatpack)	23	9	4	3	2.5	1.5

2860 tbl 03

R3000A MODE SELECTABLE FEATURES

Input	W Cycle	X Cycle	Y Cycle	Z Cycle
Int0	DBlkSize0	DBlkSize1	Extend Cache	Big Endian
Int1	IBlkSize0	IBlkSize1	MPAdrDisable	TriState
Int2	DispPar/RevEnd	IStream	IgnoreParity	NoCache
Int3	Reserved(1)	StorePartial	MultiProcessor	BusDriveOn
Int4	PhaseDelayOn(2)	PhaseDelayOn(2)	PhaseDelayOn(2)	PhaseDelayOn(2)
Int5	R3000 Mode(2)	R3000 Mode(2)	R3000 Mode(2)	R3000 Mode(2)

2860 tbl 04

NOTES:
1. Reserved entries must be driven high.
2. These values must be driven stable throughout the enfire RESET period.

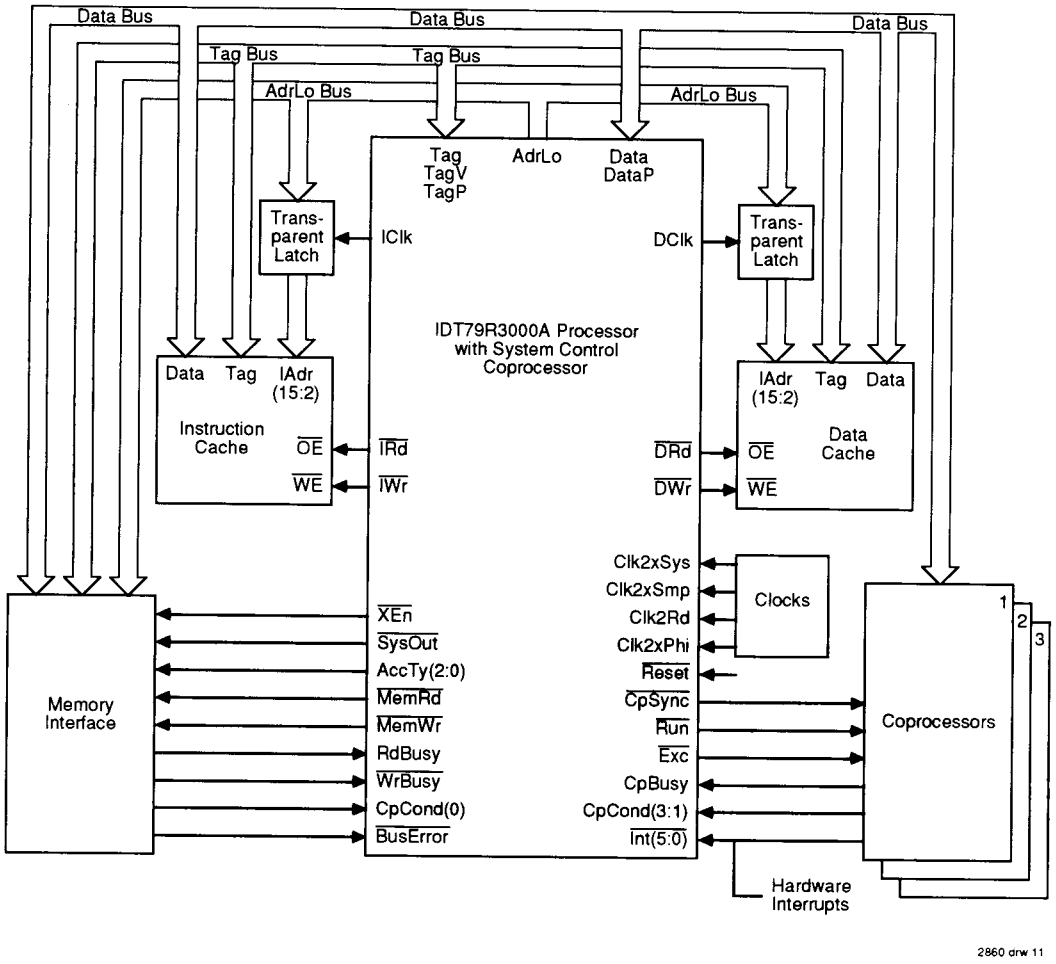

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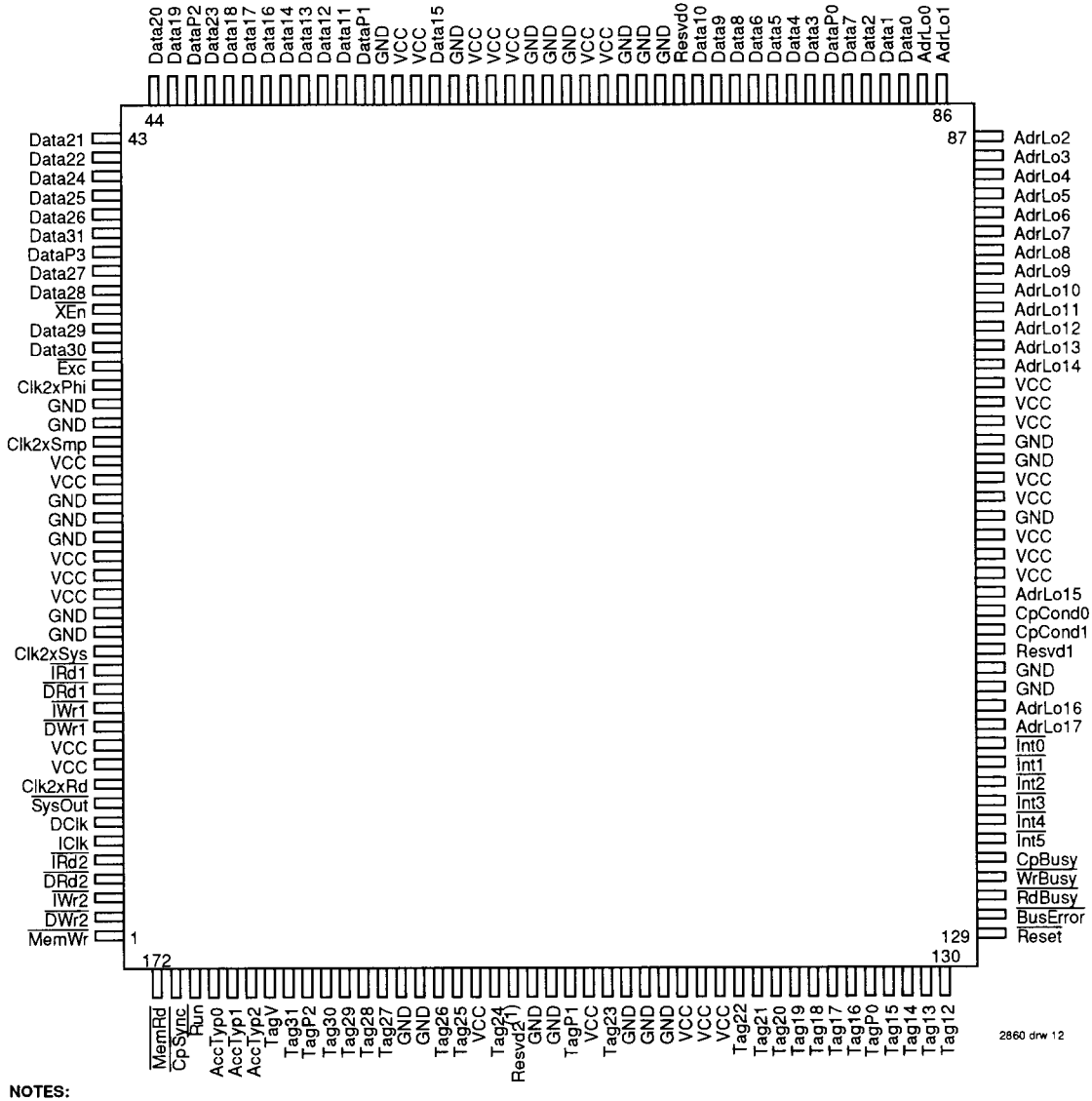
Figure 11. IDT79R3000A Subsystem Interfaces Example; 64 KB Caches

PIN CONFIGURATION



NOTES:

1. Reserved pins must not be connected.
2. AdrLo 16 and 17 are multifunction pins which are controlled by mode select programming on interrupt pins at reset time
   AdrLo 16: MP Invalidate, CpCond (2).
   AdrLo 17: MP Stall, CpCond (3).

172-Pin Flatpack (Top View)

PIN CONFIGURATION

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	(No Pin)	AdrLo 6	AdrLo 10	AdrLo 11	VCC	AdrLo 14	AdrLo 15	CpCond 0	AdrLo 16	AdrLo 17	$\overline{\text{Int(2)}}$	$\overline{\text{Int(5)}}$	Wr Busy	$\overline{\text{Reset}}$	VCC
B	AdrLo 3	$\overline{\text{DRd2}}$	AdrLo 7	AdrLo 9	AdrLo 12	$\overline{\text{IRd2}}$	AdrLo 13	CpCond 1	$\overline{\text{Int(1)}}$	$\overline{\text{Int(3)}}$	Cp Busy	$\overline{\text{Bus Error}}$	DWr2	Tag12	Tag15
C	AdrLo 0	AdrLo 4	VCC	AdrLo 5	AdrLo 8	GND	GND	VCC	$\overline{\text{Int(0)}}$	$\overline{\text{Int(4)}}$	Rd Busy	GND	Tag13	TagP0	Tag18
D	Data 1	AdrLo 2	GND	GND	VCC	GND	VCC	GND	VCC	GND	VCC	GND	Tag14	Tag17	Tag19
E	DataP 0	Data 0	AdrLo 1	VCC								VCC	Tag16	Tag20	VCC
F	VCC	Data 7	Data 2	GND								GND	GND	Tag21	Tag23
G	Data 4	Data 3	GND	VCC								VCC	GND	Tag22	TagP1
H	Data 6	Data 5	Data 8	GND								GND	VCC	Tag25	Tag24
J	Data 10	DataP 1	Data 9	VCC								VCC	Tag28	Tag29	Tag26
K	Data 15	Data 11	GND	GND								GND	GND	TagP2	Tag27
L	VCC	Data 12	Data 17	VCC								VCC	Acc Typ2	Tag31	Tag30
M	Data 13	Data 16	DataP 2	GND	VCC	GND	VCC	GND	VCC	GND	VCC	GND	GND	Acc Typ1	VCC
N	Data 14	Data 18	Data 19	GND	Data 24	DataP 3	VCC	VCC	GND	GND	$\overline{\text{DRd1}}$	$\overline{\text{Mem Wr}}$	$\overline{\text{Mem Rd}}$	$\overline{\text{Run}}$	TagV
P	Data 23	Data 20	$\overline{\text{IWr2}}$	Data 22	Data 26	Data 27	$\overline{\text{XEn}}$	Data 30	Clk2x Sys	Clk2x Rd	DClk	$\overline{\text{IRd1}}$	$\overline{\text{IWr1}}$	$\overline{\text{Cp Sync}}$	Acc Typ0
Q	VCC	Data 21	Data 25	Data 31	Data 28	GND	Data 29	$\overline{\text{Excep-tion}}$	Clk2x Phi	Clk2x Smp	$\overline{\text{SysOut}}$	VCC	IClk	$\overline{\text{DWr1}}$	VCC

2860 drw 13

NOTE:

1. AdrLo 16 and 17 are multifunction pins which are controlled by mode select programming on interrupt pins at reset time
   AdrLo 16: MP Invalidate, CpCond (2).
   AdrLo 17: MP Stall, CpCond (3).

175-Pin PGA (Top View)

PIN CONFIGURATION

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	VCC	AdrLo 6	AdrLo 10	AdrLo 11	VCC	AdrLo 14	AdrLo 15	CpCond 0	AdrLo 16	AdrLo 17	$\overline{\text{Int(2)}}$	$\overline{\text{Int(5)}}$	Wr Busy	$\overline{\text{Reset}}$	VCC
B	AdrLo 3	$\overline{\text{DRd2}}$	AdrLo 7	AdrLo 9	AdrLo 12	$\overline{\text{IRd2}}$	AdrLo 13	CpCond 1	$\overline{\text{Int(1)}}$	$\overline{\text{Int(3)}}$	Cp Busy	$\overline{\text{Bus Error}}$	$\overline{\text{DWr2}}$	Tag12	Tag15
C	AdrLo 0	AdrLo 4	VCC	AdrLo 5	AdrLo 8	GND	GND	VCC	$\overline{\text{Int(0)}}$	$\overline{\text{Int(4)}}$	Rd Busy	GND	Tag13	TagP0	Tag18
D	Data 1	AdrLo 2	GND	GND									Tag14	Tag17	Tag19
E	DataP 0	Data 0	AdrLo 1										Tag16	Tag20	VCC
F	VCC	Data 7	Data 2										GND	Tag21	Tag23
G	Data 4	Data 3	GND										GND	Tag22	TagP1
H	Data 6	Data 5	Data 8										VCC	Tag25	Tag24
J	Data 10	DataP 1	Data 9										Tag28	Tag29	Tag26
K	Data 15	Data 11	GND										GND	TagP2	Tag27
L	VCC	Data 12	Data 17										Acc Typ2	Tag31	Tag30
M	Data 13	Data 16	DataP 2										GND	Acc Typ1	VCC
N	Data 14	Data 18	Data 19	GND	Data 24	DataP 3	VCC	VCC	GND	GND	$\overline{\text{DRd1}}$	$\overline{\text{Mem Wr}}$	$\overline{\text{Mem Rd}}$	$\overline{\text{Run}}$	TagV
P	Data 23	Data 20	$\overline{\text{IWr2}}$	Data 22	Data 26	Data 27	$\overline{\text{XEn}}$	Data 30	Clk2x Sys	Clk2x Rd	DClk	$\overline{\text{IRd1}}$	$\overline{\text{IWr1}}$	$\overline{\text{Cp Sync}}$	Acc Typ0
Q	VCC	Data 21	Data 25	Data 31	Data 28	GND	Data 29	$\overline{\text{Excep-tion}}$	Clk2x Phi	Clk2x Smp	$\overline{\text{SysOut}}$	VCC	IClk	$\overline{\text{DWr1}}$	VCC

NOTE:

1. AdrLo 16 and 17 are multifunction pins which are controlled by mode select programming on interrupt pins at reset time
   AdrLo 16: MP Invalidate, CpCond (2).
   AdrLo 17: MP Stall, CpCond (3).

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144-Pin PGA (Top View)

PIN DESCRIPTIONS

Pin Name	I/O	Description
Data (0-31)	I/O	A 32-bit bus used for all instruction and data transmission among the processor, caches, memory interface, and coprocessors.
DataP (0-3)	I/O	A 4-bit bus containing even parity over the data bus.
Tag (12-31)	I/O	A 20-bit bus used for transferring cache tags and high addresses between the processor, caches, and memory interface.
TagV	I/O	The tag validity indicator.
Tag P (0-2)	I/O	A 3-bit bus containing even parity over the concatenation of TagV and Tag.
AdrLo (0-17)	O	An 18-bit bus containing byte addresses used for transferring low addresses from the processor to the caches and memory interface. (AdrLo 16: CpCond (2), AdrLo 17: CpCond (3) set by reset initialization).
$\overline{\text{IRd1}}$	O	Read enable for the instruction cache.
$\overline{\text{IWr1}}$	O	Write enable for the instructon cache.
$\overline{\text{IRd2}}$	O	An identical copy of $\overline{\text{IRd1}}$ used to split the load.
$\overline{\text{IWr2}}$	O	An identical copy of $\overline{\text{IWr1}}$ used to split the load.
IClk	O	The instruction cache address latch clock. This clock runs continuously.
$\overline{\text{DRd1}}$	O	The read enable for the data cache.
$\overline{\text{DWr1}}$	O	The write enable for the data cache.
$\overline{\text{DRd2}}$	O	An identical copy of $\overline{\text{DRd1}}$ used to split the load.
$\overline{\text{DWr2}}$	O	An identical copy of $\overline{\text{DWr1}}$ used to split the load.
DClk	O	The data cache address latch clock. This clock runs continuously.
$\overline{\text{XEn}}$	O	The read enable for the Read Buffer.
AccTyp(0-2)	O	A 3-bit bus used to indicate the size of data being transferred on the data bus, whether or not a data transfer is occurring, and the purpose of the transfer.
$\overline{\text{MemWr}}$	O	Signals the occurrence of a main memory write.
$\overline{\text{MemRd}}$	O	Signals the occurrence of a main memory read.
$\overline{\text{BusError}}$	I	Signals the occurrence of a bus error during a main memory read or write.
$\overline{\text{Run}}$	O	Indicates whether the processor is in the run or stall state.
$\overline{\text{Exception}}$	O	Indicates that the instruction about to commit state should be aborted and other exception related information.
$\overline{\text{SysOut}}$	O	A reflection of the internal processor clock used to generate the system clock.
$\overline{\text{CpSync}}$	O	A clock which is identical to $\overline{\text{SysOut}}$ and used by coprocessors for timing synchronization with the CPU.
RdBusy	I	The main memory read stall termination signal. In most system designs RdBusy is normally asserted and is deasserted only to indicate the successful completion of a memory read. RdBusy is sampled by the processor only during memory read stalls.
$\overline{\text{WrBusy}}$	I	The main memory write stall initiation/termination signal.
CpBusy	I	The coprocessor busy stall initiation/termination signal.
CpCond (0-1)	I	A 2-bit bus used to transfer conditional branch status from the coprocessors to the main processor.
CpCond (2-3)	I	Conditional branch status from coprocessors to the processor. Function is provided on AdrLo 16/17 pins and is selected at reset time.
MPStall	I	Multiprocessing Stall. Signals to the processor that it should stall accesses to the caches in a multiprocessing environment. This is physically the same pin as CpCond3; its use is determined at RESET initialization.
MPInvalidate	I	Multiprocessing Invalidate. Signals to the processor that it should issue invalidate data on the cache data bus. The address to be invalidated is externally provided. This is the same pin as CpCond2; its use is determined at RESET initialization.
$\overline{\text{Int}}$ (0-5)	I	A 6-bit bus used by the memory interface and coprocessors to signal maskable interrupts to the processor. At reset time, mode select values are read in.

2860 tbl 05

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PIN DESCRIPTIONS (Continued)

Pin Name	I/O	Description
Clk2xSys	I	The master double frequency input clock used for generating $\overline{SysOut}$.
Clk2xSmp	I	A double frequency clock input used to determine the sample point for data coming into the processor and coprocessors.
Clk2xRd	I	A double frequency clock input used to determine the enable time of the cache RAMs.
Clk2xPhi	I	A double frequency clock input used to determine the position of the internal phases, phase1 and phase2.
$\overline{Reset}$	I	Synchronous initialization input used to force execution starting from the reset memory address. $\overline{Reset}$ must be deasseted synchronously but asserted asynchronously. The deassertion of $\overline{Reset}$ must be synchronized by the leading edge of $\overline{SysOut}$.

2860 tbl 06

ABSOLUTE MAXIMUM RATINGS(1, 3)

Symbol	Rating	Commercial	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A, T_C	Operating Temperature	0 to +70(4) (Ambient) 0 to +90(5) (Case)	°C
T_{BIAS}	Case Temperature Under Bias	–55 to +125(4) 0 to +90(5)	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{IN}	Input Voltage	–0.5 to +7.0	V

2860 tbl 07

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{IN} minimum = –3.0V for pulse width less than 15ns. V_{IN} should not exceed V_{CC} +0.5 Volts.
3. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.
4. 16-33 MHz only.
5. 37-40 MHz only.

AC TEST CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V_{IH}	Input HIGH Voltage	3.0	—	V
V_{IL}	Input LOW Voltage	—	0.4	V
V_{IHS}	Input HIGH Voltage	3.5	—	V
V_{ILS}	Input LOW Voltage	—	0.4	V

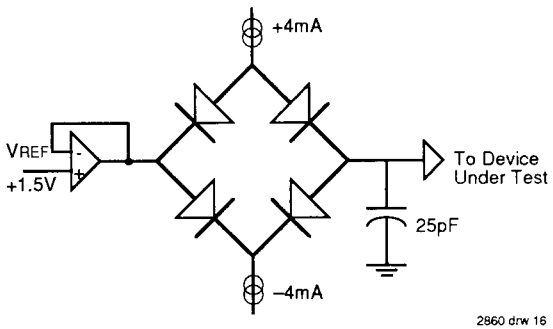
2860 tbl 08

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Commercial 16-33 MHz	0°C to +70°C (Ambient)	0V	5.0 ±5%
Commercial 40 MHz	0°C to +90°C (Case)	0V	5.0 ±5%

2860 tbl 09

OUTPUT LOADING FOR AC TESTING



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DC ELECTRICAL CHARACTERISTICS
COMMERCIAL TEMPERATURE RANGE (T_A = 0°C to +70°C, V_{CC} = +5.0V ±5%)

Symbol	Parameter	Test Conditions	79R3000A				79R3000AE				Unit
			16.67MHz		20.0MHz		25.0MHz		33.33MHz		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = -4mA	3.5	—	3.5	—	3.5	—	3.5	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4mA	—	0.4	—	0.4	—	0.4	—	0.4	V
V_{OHC}	Output HIGH Voltage(7)	V_{CC} = Min., I_{OH} = -4mA	4.0	—	4.0	—	4.0	—	4.0	—	V
V_{OHT}	Output HIGH Voltage(4,6)	V_{CC} = Min., I_{OH} = -8mA	2.4	—	2.4	—	2.4	—	2.4	—	V
V_{OLT}	Output LOW Voltage(4,6)	V_{CC} = Min., I_{OL} = 8mA	—	0.8	—	0.8	—	0.8	—	0.8	V
V_{IH}	Input HIGH Voltage(5)		2.0	—	2.0	—	2.0	—	2.0	—	V
V_{IL}	Input LOW Voltage(1)		—	0.8	—	0.8	—	0.8	—	0.8	V
V_{IHS}	Input HIGH Voltage(2,5)		3.0	—	3.0	—	3.0	—	3.0	—	V
V_{ILS}	Input LOW Voltage(1,2)		—	0.4	—	0.4	—	0.4	—	0.4	V
C_{IN}	Input Capacitance(6)		—	10	—	10	—	10	—	10	pF
C_{OUT}	Output Capacitance(6)		—	10	—	10	—	10	—	10	pF
I_{CC}	Operating Current	V_{CC} = 5V, T_A = 70°C	—	450	—	550	—	650	—	750	mA
I_{IH}	Input HIGH Leakage(3)	V_{IH} = VCC	—	100	—	100	—	100	—	100	µA
I_{IL}	Input LOW Leakage(3)	V_{IL} = GND	–100	—	–100	—	–100	—	–100	—	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = VCC, V_{OL} = GND	–100	100	–100	100	–100	100	–100	100	µA

2860 tbl 10

NOTES:

1. V_{IL} Min. = –3.0V for pulse width less than 15ns. V_{IL} should not fall below –0.5 Volts for larger periods.
2. V_{IHS} and V_{ILS} apply to Clk2xSys, Clk2xSmp, Clk2xRd, Clk2xPhi, CpBusy, and $\overline{\text{Reset}}$.
3. These parameters do not apply to the clock inputs.
4. V_{OHT} and V_{OLT} apply to the bidirectional data and tag busses only. Note that V_{IH} and V_{IL} also apply to these signals. V_{OHT} and V_{OLT} are provided to give the designer further information about these specific signals.
5. V_{IH} should not be held above V_{CC} + 0.5 volts.
6. Guaranteed by design.
7. V_{OHC} applies to $\overline{\text{RUN}}$ and $\overline{\text{Exception}}$.

5

DC ELECTRICAL CHARACTERISTICS
COMMERCIAL TEMPERATURE RANGE (T_C = 0°C to +90°C, V_{CC} = +5.0V ±5%)

Symbol	Parameter	Test Conditions	79R3000AE 40.0MHz Min.	79R3000AE 40.0MHz Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = -4mA	3.5	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4mA	—	0.4	V
V_{OHC}	Output HIGH Voltage(7)	V_{CC} = Min., I_{OH} = –4mA	4.0	—	V
V_{OHT}	Output HIGH Voltage(4,6)	V_{CC} = Min., I_{OH} = –8mA	2.4	—	V
V_{OLT}	Output LOW Voltage(4,6)	V_{CC} = Min., I_{OL} = 8mA	—	0.8	V
V_{IH}	Input HIGH Voltage(5)		2.0	—	V
V_{IL}	Input LOW Voltage(1)		—	0.8	V
V_{IHS}	Input HIGH Voltage(2,5)		3.0	—	V
V_{ILS}	Input LOW Voltage(1,2)		—	0.4	V
C_{IN}	Input Capacitance(6)		—	10	pF
C_{OUT}	Output Capacitance(6)		—	10	pF
I_{CC}	Operating Current	V_{CC} = 5V, T_A = 70°C	—	850	mA
I_{IH}	Input HIGH Leakage(3)	V_{IH} = VCC	—	100	µA
I_{IL}	Input LOW Leakage(3)	V_{IL} = GND	–100	—	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = VCC, V_{OL} = GND	–100	100	µA

2860 tbl 12

NOTES:

1. V_{IL} Min. = –3.0V for pulse width less than 15ns. V_{IL} should not fall below –0.5 Volts for larger periods.
2. V_{IHS} and V_{ILS} apply to Clk2xSys, Clk2xSmp, Clk2xRd, Clk2xPhi, CpBusy, and $\overline{\text{Reset}}$.
3. These parameters do not apply to the clock inputs.
4. V_{OHT} and V_{OLT} apply to the bidirectional data and tag busses only. Note that V_{IH} and V_{IL} also apply to these signals. V_{OHT} and V_{OLT} are provided to give the designer further information about these specific signals.
5. V_{IH} should not be held above V_{CC} + 0.5 volts.
6. Guaranteed by design.
7. V_{OHC} applies to $\overline{\text{RUN}}$ and $\overline{\text{Exception}}$.

AC ELECTRICAL CHARACTERISTICS(1,2,3)
COMMERCIAL TEMPERATURE RANGE (TA = 0°C to +70°C, Vcc = +5.0V ±5%)

Symbol	Parameter	Test Conditions	79R3000A				79R3000AE				Unit
			16.67MHz		20.0MHz		25.0MHz		33.33MHz		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Clock											
TCkHigh	Input Clock HIGH(2)	Note 7	12.5	—	10	—	8.0	—	6.0	—	ns
TCkLow	Input Clock LOW(2)	Note 7	12.5	—	10	—	8.0	—	6.0	—	ns
TCkP	Input Clock Period(2)		30	500	25	500	20	500	15	500	ns
	Clk2xSys to Clk2XSmp(6)		0	tcyc/4	0	tcyc/4	0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xRd(6)		0	tcyc/4	0	tcyc/4	0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xPhi(6)		9.0	tcyc/4	7.0	tcyc/4	5.0	tcyc/4	3.5	tcyc/4	ns
Run Operation											
TDEn	Data Enable(3)		—	–2.0	—	–2.0	—	–1.5	—	–1.5	ns
TDDis	Data Disable(3)		—	–1.0	—	–1.0	—	–0.5	—	–0.5	ns
TDVal	Data Valid	Load= 25pF	—	3.0	—	3.0	—	2.0	—	2.0	ns
TWrDly	Write Delay	Load= 25pF	—	5.0	—	4.0	—	3.0	—	2.0	ns
TDS	Data Set-up		9.0	—	8.0	—	6.0	—	4.5	—	ns
TDH	Data Hold(3)		–2.5	—	–2.5	—	–2.5	—	–2.5	—	ns
TCBS	CpBusy Set-up		13	—	11	—	9.0	—	7.0	—	ns
TCBH	CpBusy Hold		–2.5	—	–2.5	—	–2.5	—	–2.5	—	ns
TAcTy	Access Type (1:0)	Load= 25pF	—	7.0	—	6.0	—	5.0	—	3.5	ns
TAT2	Access Type 2	Load= 25pF	—	17	—	14	—	12	—	8.5	ns
TMWr	Memory Write	Load= 25pF	—	27	—	23	—	18	—	9.5	ns
TExc	Exception	Load= 25pF	—	7.0	—	7.0	—	5.0	—	3.5	ns
TAval	Address Valid	Load= 25pF	—	2.0	—	2.0	—	1.5	—	1.0	ns
TIntS	$\overline{\text{Int(n)}}$ Set-up		9.0	—	8.0	—	6.0	—	4.5	—	ns
TIntH	$\overline{\text{Int(n)}}$ Hold		–2.5	—	–2.5	—	–2.5	—	–2.5	—	ns
Stall Operation											
TSAVal	Address Valid	Load= 25pF	—	30	—	23	—	20	—	15	ns
TSAcTy	Access Type	Load= 25pF	—	27	—	23	—	18	—	13.5	ns
TMRdi	Memory Read Initiate	Load= 25pF	1.0	27	1.0	23	1.0	18	1.0	13.5	ns
TMRdt	Memory Read Terminate	Load= 25pF	—	27	—	23	—	18	—	10	ns
TStl	Run Terminate	Load= 25pF	3.0	17	3.0	15	3.0	10	2.0	7.5	ns
TRun	Run Initiate	Load= 25pF	—	7.0	—	6.0	—	4.0	—	3.0	ns
TSMWr	Memory Write	Load= 25pF	3.0	27	3.0	23	3.0	18	2.0	9.5	ns
TSExc	Exception Valid	Load= 25pF	—	15	—	13	—	10	—	7.5	ns
Reset Initialization											
TRST	Reset Pulse Width		6.0	—	6.0	—	6.0	—	6.0	—	Tcyc
TrstPLL	Reset timing, Phase-lock on(4,5)		3000	—	3000	—	3000	—	3000	—	Tcyc
Trstcp	Reset timing, Phase-lock off(4,5)		128	—	128	—	128	—	128	—	Tcyc
Capacitive Load Deration											
CLD	Load Derate(6)		0.5	2.0	0.5	1.0	0.5	1.0	0	1.0	ns/25pF

2860 tbl 13

NOTES:
1. All timings are referenced to 1.5V.
2. The clock parameters apply to all four 2xClocks: Clk2xSys, Clk2xSmp, Clk2xRd, and Clk2xPhi.
3. This parameter is guaranteed by design.
4. These parameters apply when the IDT79R3010 Floating Point Coprocessor is connected to the CPU. With phase lock on, $\overline{\text{Reset}}$ must be asserted for the longer of 3000 clock cycles or 200 microseconds.
5. Tcyc is one CPU clock cycle (two cycles of a 2x clock).
6. With the exception of the $\overline{\text{Run}}$ signal, no two signals on a given device will derate for a given load by a difference greater than 15%.
7. Clock transition time < 2.5ns for 33.33MHz; clock transition time < 5ns for other speeds.

AC ELECTRICAL CHARACTERISTICS(1,2,3)
COMMERCIAL TEMPERATURE RANGE (Tc = 0°C to +90°C, Vcc = +5.0V ±5%)

Symbol	Parameter	Test Conditions	79R3000AE 40.0MHz Min.	79R3000AE 40.0MHz Max.	Unit
Clock					
TCkHigh	Input Clock High(2)	Note 7	5.0	—	ns
TCkLow	Input Clock Low(2)	Note 7	5.0	—	ns
TCkP	Input Clock Period(2)		12.5	500	ns
	Clk2xSys to Clk2XSmp(6)		0	tcyc/4	ns
	Clk2xSmp to Clk2xRd(6)		0	tcyc/4	ns
	Clk2xSmp to Clk2xPhi(6)		3.0	tcyc/4	ns
Run Operation					
	TDEn	Data Enable(3)	—	–1.5	ns
TDDis	Data Disable(3)		—	–0.5	ns
TDVal	Data Valid	Load= 25pF	—	1.5	ns
TWrDly	Write Delay	Load= 25pF	—	2.0	ns
TDS	Data Set-up		4.0	—	ns
TDH	Data Hold(3)		–2.5	—	ns
TCBS	CpBusy Set-up		6.0	—	ns
TCBH	CpBusy Hold		–2.5	—	ns
TAcTy	Access Type (1:0)	Load= 25pF	—	3.0	ns
TAT2	Access Type 2	Load= 25pF	—	7.5	ns
TMWr	Memory Write	Load= 25pF	—	9.0	ns
TExc	Exception	Load= 25pF	—	3.0	ns
TAval	Address Valid	Load= 25pF	—	0.5	ns
TIntS	$\overline{\text{Int(n)}}$ Set-up		4.0	—	ns
TIntH	$\overline{\text{Int(n)}}$ Hold		–2.5	—	ns
Stall Operation					
TSAVal	Address Valid	Load= 25pF	—	12.5	ns
TSAcTy	Access Type	Load= 25pF	—	9.0	ns
TMRdi	Memory Read Initiate	Load= 25pF	—	9.0	ns
TMRdt	Memory Read Terminate	Load= 25pF	—	9.0	ns
TStl	Run Terminate	Load= 25pF	2.0	6.0	ns
TRun	Run Initiate	Load= 25pF	—	3.0	ns
TSMWr	Memory Write	Load= 25pF	2.0	9.0	ns
TSExc	Exception Valid	Load= 25pF	—	6.0	ns
Reset Initialization					
TRST	Reset Pulse Width		6.0	—	Tcyc
TrstPLL	Reset timing, Phase-lock on(4,5)		3000	—	Tcyc
Trstcp	Reset timing, Phase-lock off(4,5)		128	—	Tcyc
Capacitive Load Deration					
CLD	Load Derate(6)		0	1.0	ns/25pF

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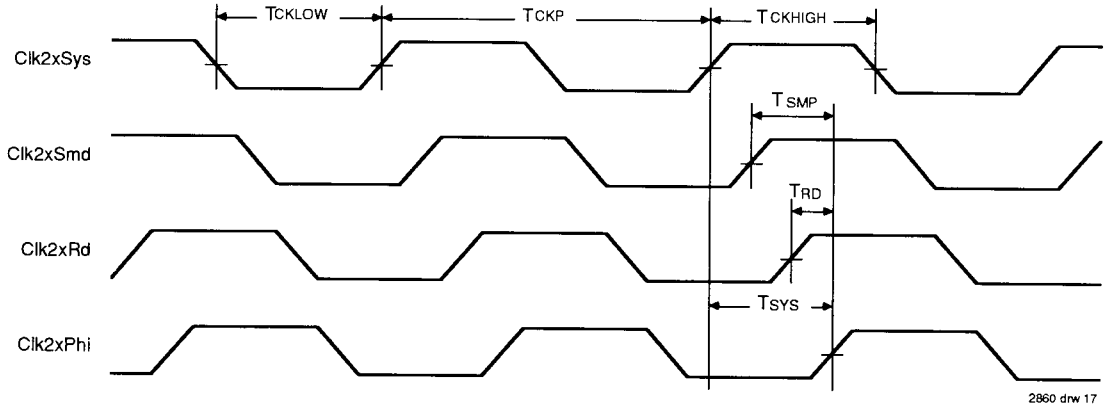
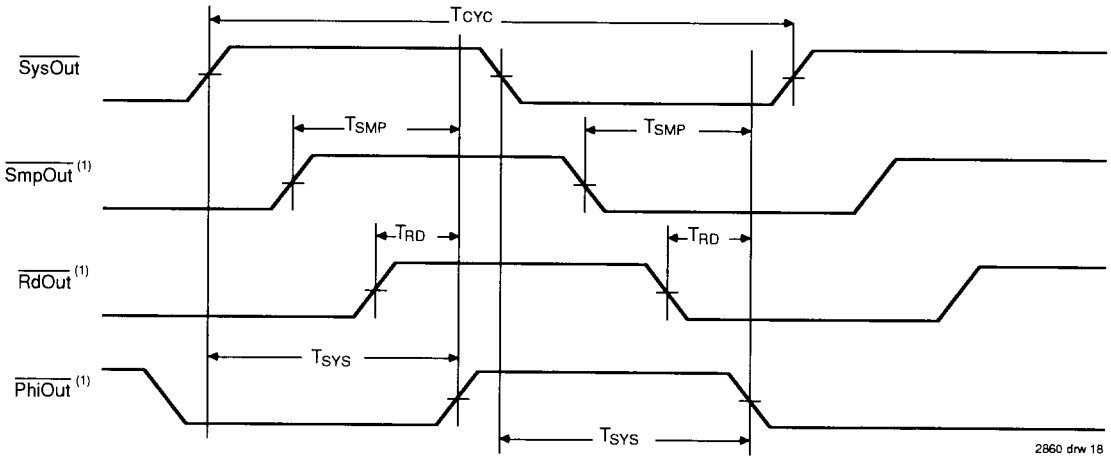
NOTES:
1. All timings are referenced to 1.5V.
2. The clock parameters apply to all four 2xClocks: Clk2xSys, Clk2xSmp, Clk2xRd, and Clk2xPhi.
3. This parameter is guaranteed by design.
4. These parameters apply when the IDT79R3010 Floating Point Coprocessor is connected to the CPU. With phase lock on, $\overline{\text{Reset}}$ must be asserted for the longer of 3000 clock cycles or 200 microseconds.
5. Tcyc is one CPU clock cycle (two cycles of a 2x clock).
6. With the exception of the $\overline{\text{Run}}$ signal, no two signals on a given device will derate for a given load by a difference greater than 15%.
7. Clock transition time < 2.5ns.

INPUT CLOCK TIMING



PROCESSOR REFERENCE CLOCK TIMING



NOTE:
1. These signals are not actually output from the processor. They are drawn to provide a reference for other timing diagrams.

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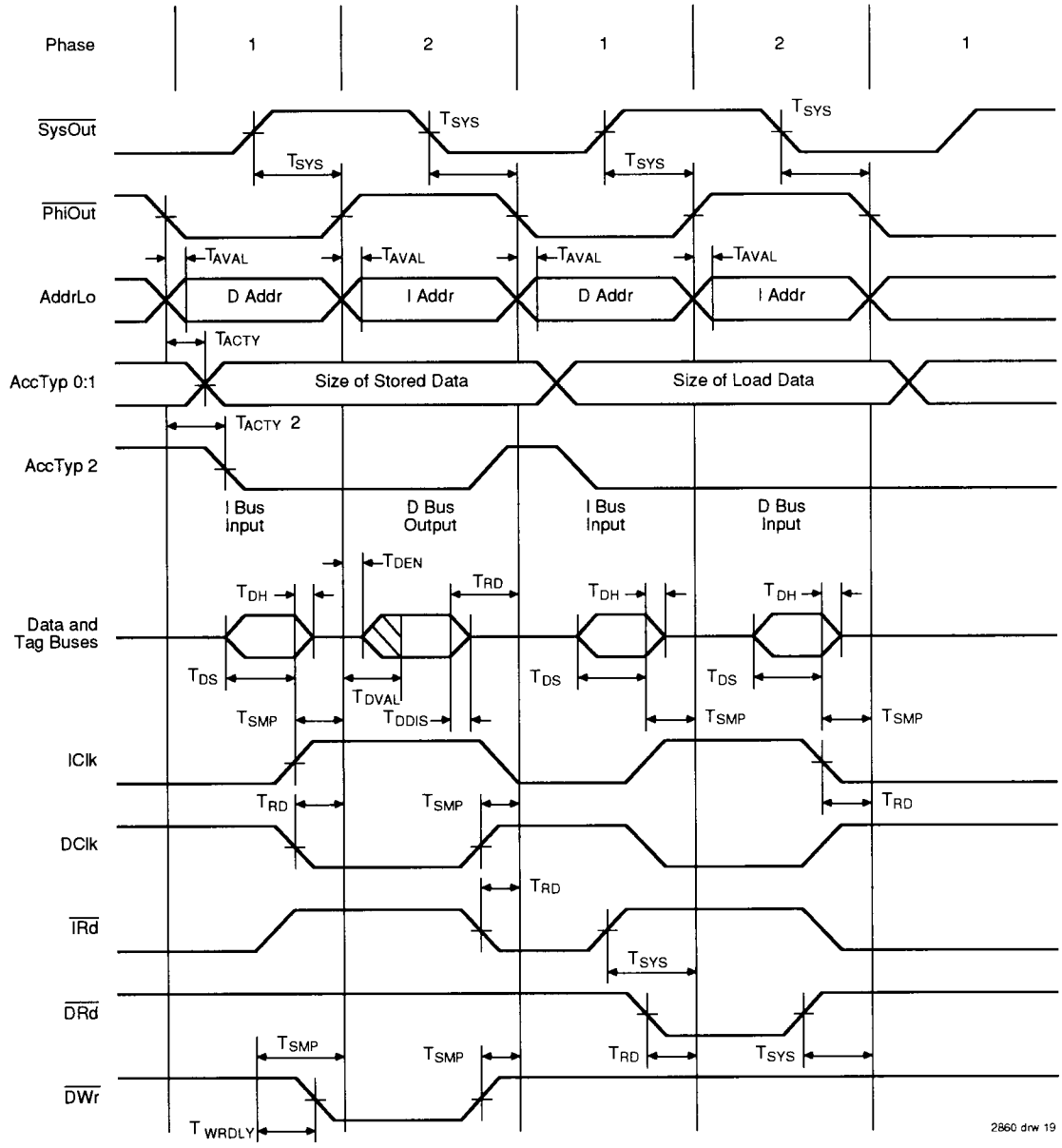
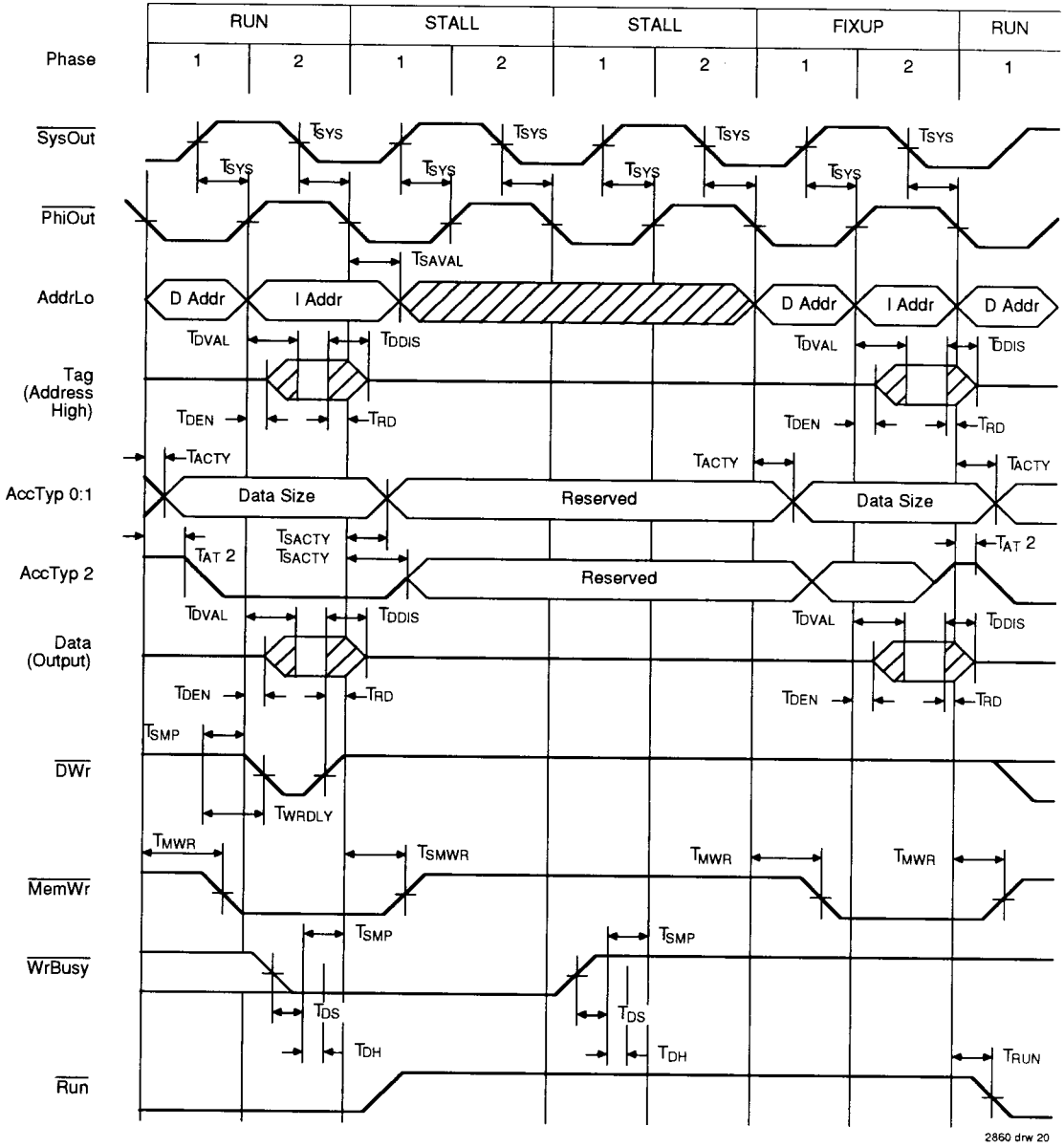
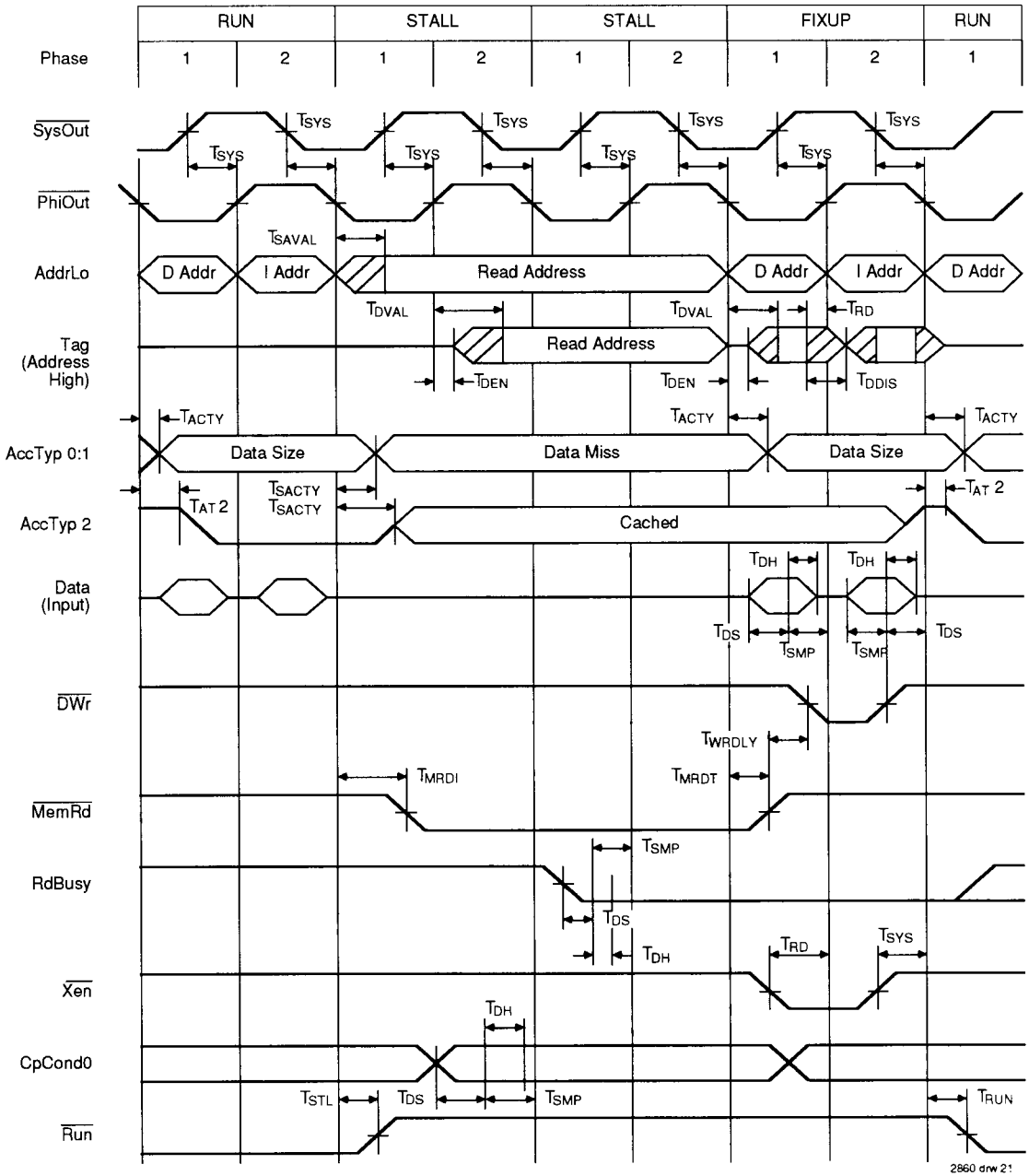
SYNCHRONOUS MEMORY (CACHE) TIMING



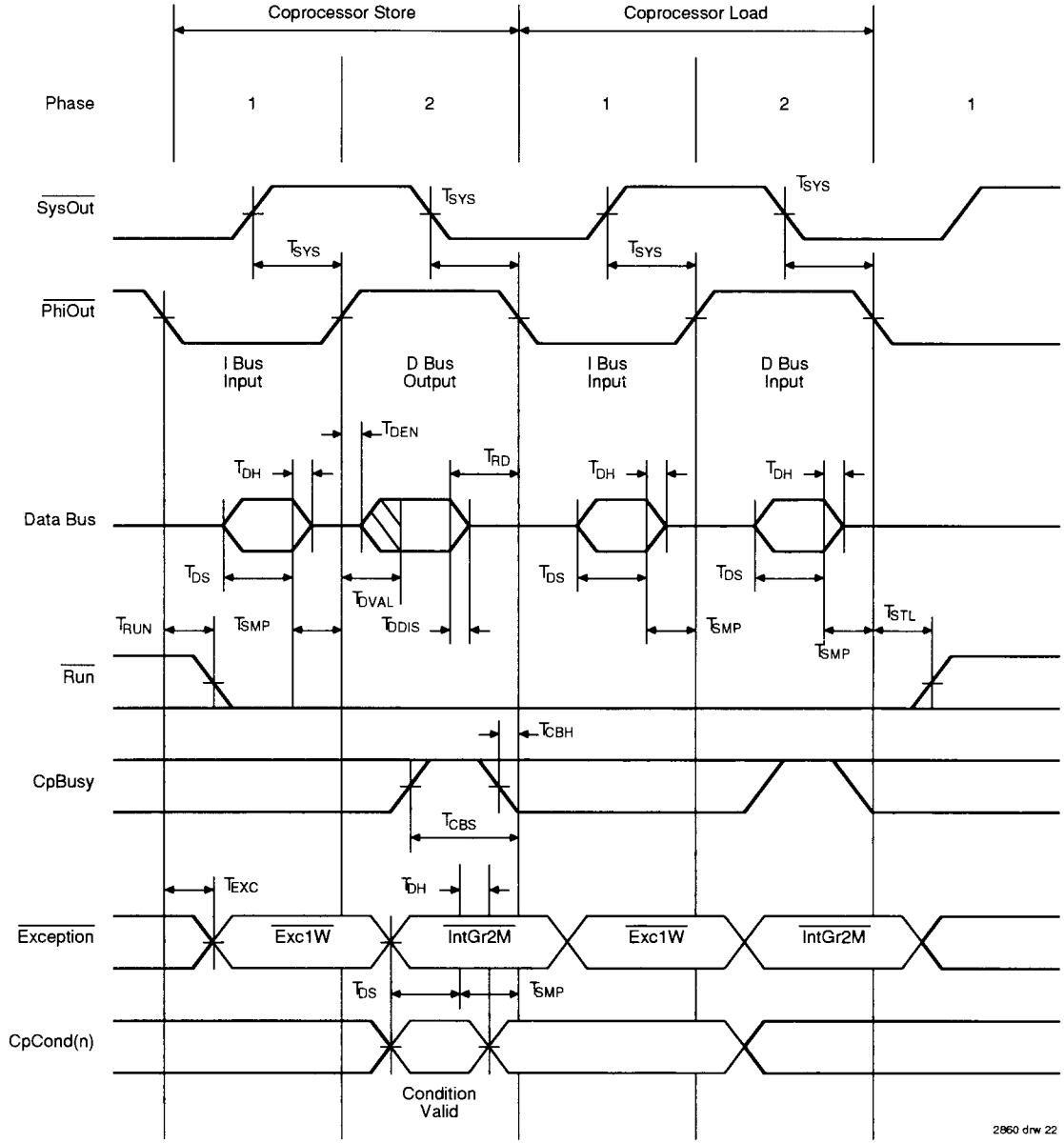
MEMORY WRITE TIMING



MEMORY READ TIMING



COPROCESSOR LOAD/STORE TIMING



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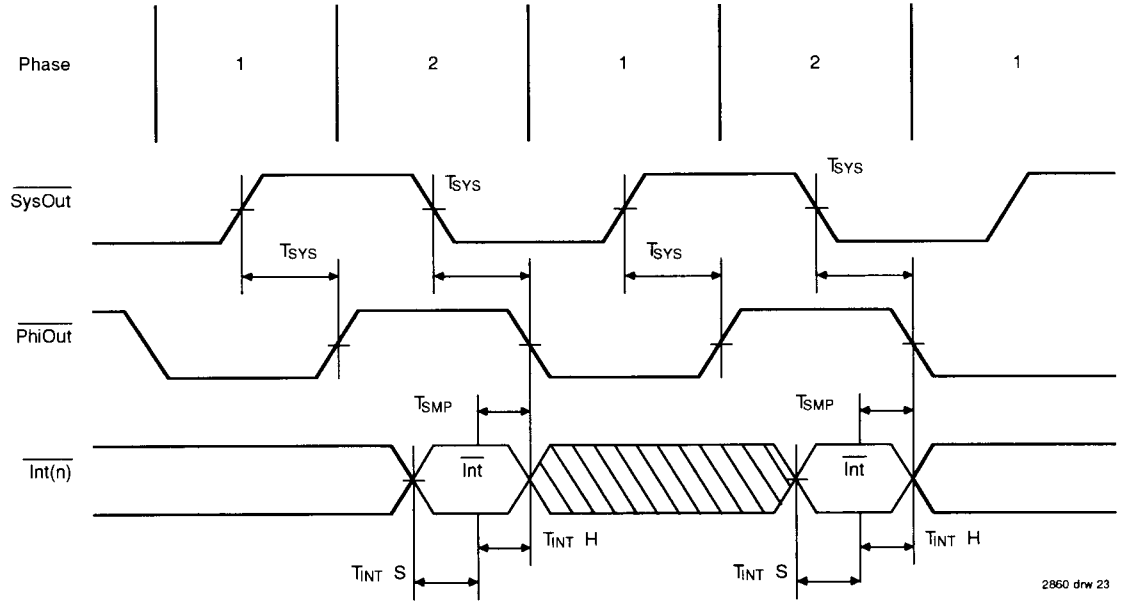
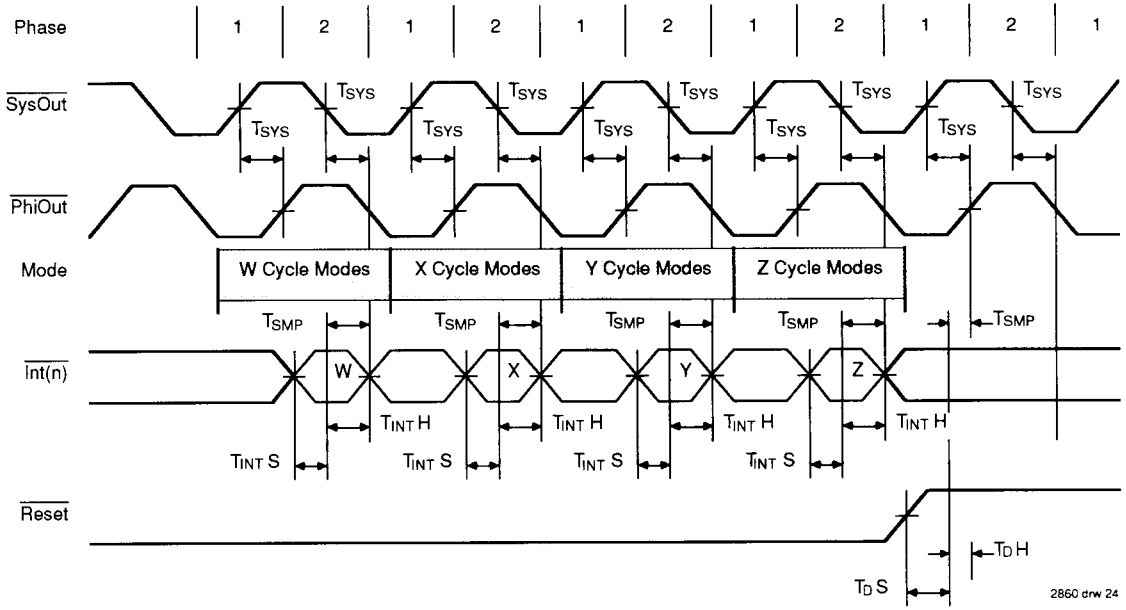
INTERRUPT TIMING



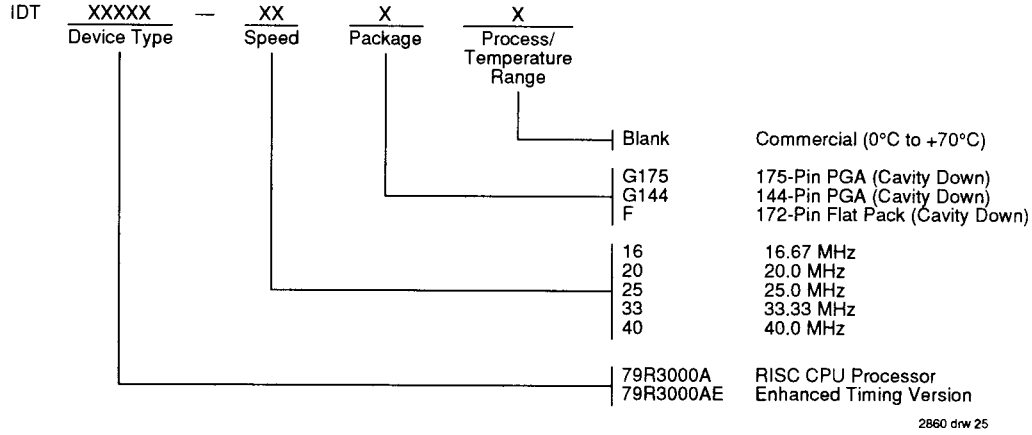
MODE VECTOR INITIALIZATION



NOTES:

1. Reset must be negated synchronously; however, it should be asserted asynchronously. Designs must not rely on the proper functioning of $\overline{\text{SysOut}}$ prior to the assertion of $\overline{\text{Reset}}$.
2. If $\overline{\text{Phase-Lock On}}$ or $\overline{\text{R3000 Mode}}$ are asserted as mode select options, they should be asserted throughout the $\overline{\text{Reset}}$ period, to insure that the slowest coprocessor in the system has sufficient time to lock to the CPU clocks.
3. $\overline{\text{Reset}}$ is actually sampled in both Phase 1 and Phase 2. To insure proper initialization, it must be negated relative to the end of Phase 1.

ORDERING INFORMATION



VALID COMBINATIONS

IDT	79R3000A - 16, 20	All Packages
	79R3000AE - 25, 33, 40	All Packages

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