SMC82C37AC/-4/-5

CMOS PROGRAMMABLE DMA CONTROLLER

●Four DMA Channels
●Low Supply Current

■DESCRIPTION

The SMC82C37AC/-4/-5 is an enhanced CMOS version of a programmable 4-channel Direct Memory Access (DMA) controller. The device is designed to improve system performance by permitting the CPU to off-load the task of moving blocks of data to and from memory via one of the DMA channels.

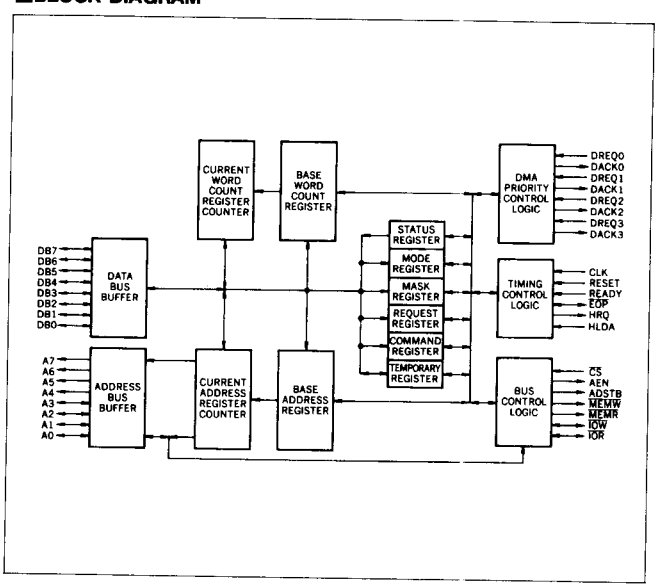
■FEATURES

- ●Four DMA channels
- ●High data transfer rates ; up to 1.6M bytes/second
- ●Enable/disable control of DMA request
- ●Programmable features ·····Logic polarity of DREQ and DACK
  Fixed or rotating priority
  Address increment or decrement
- ●Automatic features ·····Channel initialization
- ●External DMA termination
- ●Single power supply ·····5V±10%
- ●Package·····40-pin DIP (plastic)

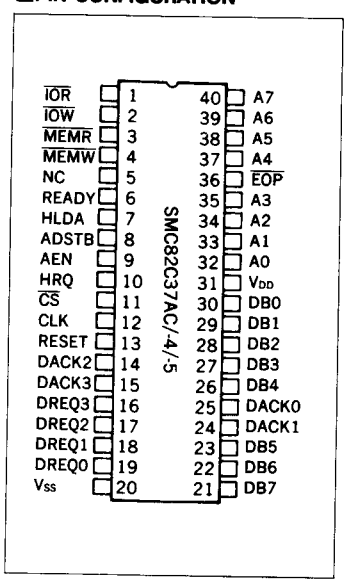
- ●Clock frequency
  - −SMC82C37AC : 3.1MHz
  - −SMC82C37AC-4 : 4MHz
  - −SMC82C37AC-5*: 5MHz

  *Under development

■BLOCK DIAGRAM



■PIN CONFIGURATION



■ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.3 to 7	V
Input voltage	V_I	−0.3 to V_{DD}+0.3	V
Output voltage	V_O	−0.3 to V_{DD}+0.3	V
Operating free-air temperature range	T_{opr}	0 to 70	°C
Storage temperature range	T_{stg}	−65 to 150	°C

■RECOMMENDED OPERATING CONDITIONS

(Ta=0 to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}	—	4.5	5	5.5	V
Supply voltage	V_{SS}	—	—	0	—	V

■ELECTRICAL CHARACTERISTICS

●DC Electrical Characteristics

(V_{DD}=5V±10%, V_{SS}=0V, Ta=0 to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Low level input voltage	V_{IL}		−0.3	—	0.8	V
High level input voltage	V_{IH}		2.0	—	V_{CC}+0.3	V
Low level output voltage	V_{OL}	I_{OL}=2.0mA (data bus) I_{OL}=3.2mA (other outputs)	—	—	0.45	V
High level output voltage	V_{OH}	I_{OH}=−200μA	2.4	—	—	V
		I_{OH}=−100μA (HRQ only)	3.2	—	—	V
Input current	I_I	V_I=0 to V_{DD}	−10	—	10	μA
Off state output current	I_{OZ}	V_I=0 to V_{DD}	−10	—	10	μA
Supply current from V_{DD}	I_{DD}	V_{IH}=V_{DD}, V_{IL}=V_{SS}, f_{CLK}=1/t_{cy} Min	—	—	15	mA

●AC Electrical Characteristics

○Slave mode

(V_{DD}=5V±10%, V_{SS}=0V, Ta=0 to 70°C)

Parameter	Symbol	Conditions	SMC82C37AC		SMC82C37AC-4		SMC82C37AC-5		Unit
			Min	Max	Min	Max	Min	Max	
Address or $\overline{CS}$ setup time before read	t_{AR}	—	0	—	0	—	0	—	ns
$\overline{CS}$ setup time before write rising edge	t_{CW}	—	200	—	150	—	150	—	ns
Address setup time before write rising edge	t_{AW}	—	200	—	150	—	150	—	ns
Data setup time before write rising edge	t_{DW}	—	200	—	150	—	100	—	ns
Address or $\overline{CS}$ hold time after read	t_{RA}	—	0	—	0	—	0	—	ns
$\overline{CS}$ hold time after write	t_{WC}	—	0	—	0	—	0	—	ns
Address hold time after write	t_{WA}	—	0	—	0	—	0	—	ns
Data hold time after write	t_{WD}	—	0	—	0	—	0	—	ns
Read pulse width	t_{RW}	—	300	—	250	—	200	—	ns
Write pulse width	t_{WWS}	—	200	—	200	—	160	—	ns
Reset pulse width	t_{RSTW}	—	300	—	300	—	300	—	ns
Supply voltage setup time before reset	t_{RSTD}	—	500	—	500	—	500	—	ns
Reset setup time before read or write	t_{RSTS}	—	2t_{CY}	—	2t_{CY}	—	2t_{CY}	—	ns
Data output enable after read	t_{RDE}	—	—	200	—	200	—	140	ns
Data output disable after read	t_{RDF}	—	0	100	0	100	0	70	ns

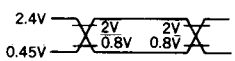
○DMA mode

(V_{DD}=5V±10%, V_{SS}=0V, Ta=0 to 70°C)

Parameter	Symbol	Conditions	SMC82C37AC		SMC82C37AC-4		SMC82C37AC-5		Unit
			Min	Max	Min	Max	Min	Max	
Propagation time from clock to AEN	t_{AEL}	—	—	300	—	225	—	200	ns
Propagation time from clock to AEN	t_{AET}	—	—	200	—	150	—	130	ns
Propagation time from clock to address active	t_{FAAB}	—	—	250	—	190	—	170	ns
Propagation time from clock to address stable	t_{ASM}	—	—	250	—	190	—	170	ns
Propagation time from clock to address floating	t_{AFAB}	—	—	150	—	120	—	90	ns
Propagation time from clock to data active	t_{FADB}	—	—	300	—	225	—	200	ns
Propagation time from clock to data floating	t_{AFDB}	—	—	250	—	190	—	170	ns
Propagation time from clock to ADSTB	t_{STL}	—	—	200	—	150	—	130	ns
Propagation time from clock to ADSTB	t_{STT}	—	—	140	—	110	—	90	ns
Data setup time before ADSTB	t_{ASS}	—	100	—	100	—	100	—	ns
Data hold time after ADSTB	t_{AHS}	—	50	—	40	—	30	—	ns
Propagation time from clock to read or write active	t_{FAC}	—	—	200	—	150	—	150	ns
Propagation time from clock to read or write	t_{DCL}	—	—	270	—	200	—	190	ns
Propagation time from clock to read	t_{DCTR}	—	—	270	—	210	—	190	ns
Propagation time from clock to write	t_{DCTW}	—	—	200	—	150	—	130	ns
Propagation time from clock to read or write floating	t_{AFC}	—	—	150	—	120	—	120	ns
Address hold time after read	t_{AHR}	—	t_{CY}-100	—	t_{CY}-100	—	t_{CY}-100	—	ns
Address hold time after write	t_{AHW}	—	t_{CY}-50	—	t_{CY}-50	—	t_{CY}-50	—	ns
Data setup time before $\overline{MEMW}$	t_{ODV}	—	200	—	125	—	125	—	ns
Data hold time after $\overline{MEMW}$	t_{ODH}	—	20	—	20	—	10	—	ns
Propagation time from clock to $\overline{DACK}$	t_{AK}	—	—	250	—	220	—	170	ns
Propagation time from clock to $\overline{EOP}$ output		—	—	250	—	190	—	170	ns
Propagation time from clock to HRQ "H" 2.0V	t_{DQ}	—	—	160	—	120	—	120	ns
Propagation time from clock to HRQ "H" 3.3V		—	—	250	—	190	—	120	ns
Clock high width	t_{CH}	—	120	—	100	—	80	—	ns
Clock low width	t_{CL}	—	150	—	110	—	68	—	ns
Clock period	t_{CY}	—	320	—	250	—	200	—	ns
External $\overline{EOP}$ setup time before clock	t_{EPS}	—	60	—	45	—	40	—	ns
External $\overline{EOP}$ pulse width	t_{EPW}	—	300	—	225	—	220	—	ns
DREQ setup time before clock	t_{DS}	—	0	—	0	—	0	—	ns
Ready setup time before clock	t_{RS}	—	100	—	60	—	60	—	ns
Ready hold time after clock	t_{RH}	—	20	—	20	—	20	—	ns
HLDA setup time before clock	t_{HS}	—	100	—	75	—	75	—	ns
Data setup time before $\overline{MEMR}$	t_{IDS}	—	250	—	190	—	170	—	ns
Data hold time after $\overline{MEMR}$	t_{IDH}	—	0	—	0	—	0	—	ns

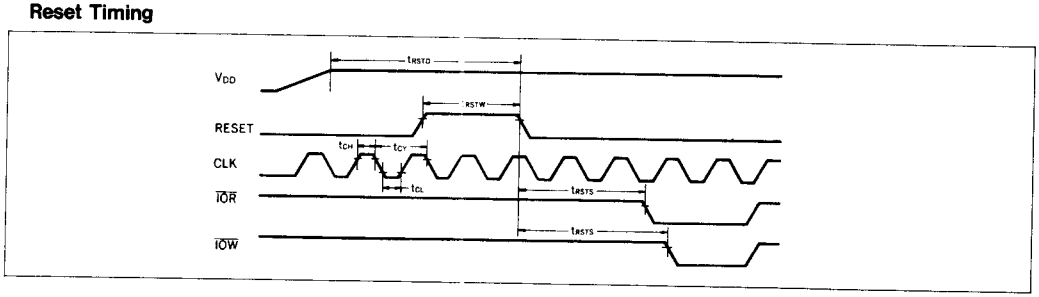
Notes : AC testing waveform

Input pulse level	0.45V to 2.4V	Reference level		
Input pulse rise time	10ns	input	V_{IH}=2V, V_{IL}=0.8V	
Input pulse fall time	10ns	output	V_{OH}=2V, V_{OL}=0.8V	

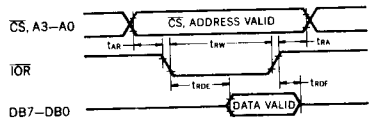


●Timing Chart

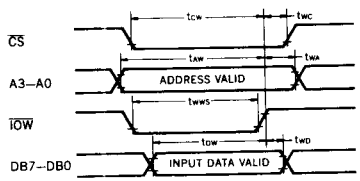
Reset Timing



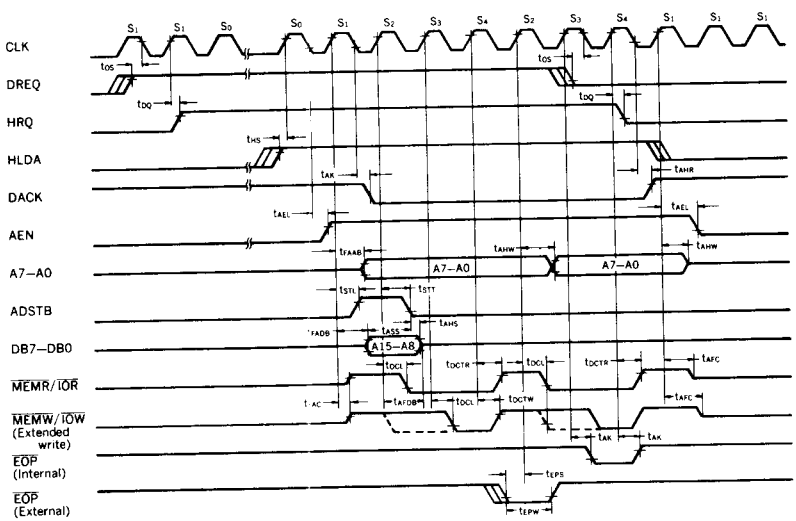
Slave Mode Timing (READ)



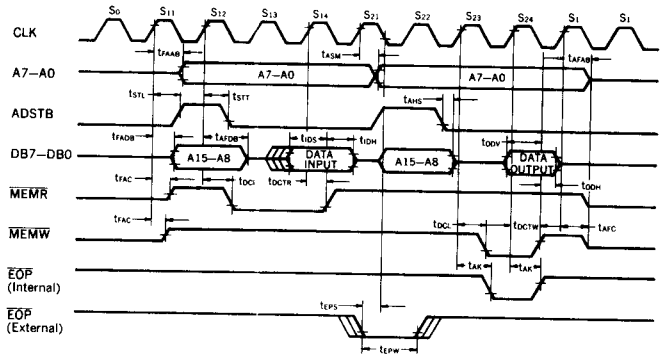
Slave Mode Timing (WRITE)



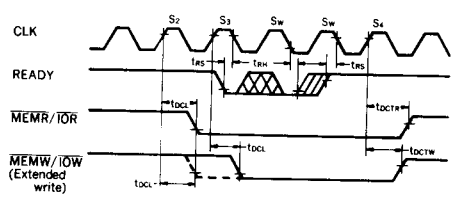
DMA Transfer



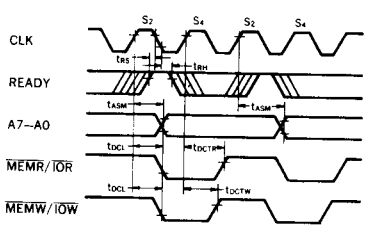
Memory to Memory Transfer



Ready Input Timing



Compressed Transfer Timing



■FUNCTIONS

The SMC82C37AC/-4/-5 is a programmable 4-channel DMA controller. The device offers a variety of programmable control features that can be dynamically reconfigured under program control. There are three programmable transfer modes : single, block and demand. There is also a full 64K address and word count capability per channel.

The device consists of three basic control blocks : the timing control block, the program command control block and the priority encoder block. To start a DMA operation, set a start address, an end address, a mode, and commands. The device requests control of the system bus when HRQ=1 is valid. The CPU acknowledges that it has relinquished control of the system bus via the hold acknowledge pin (HLDA=1) to the SMC 82C37AC/-4/-5. A DACK signal is then sent to the highest priority channel and DMA operation begins.

In the process of the DMA operation, addressing is performed in two bytes. The low byte is outputs A7–A0 and the high byte is outputs DB7–DB0; the high byte is sent to an external address latch. After the address is transmitted, the read/write control signals are sent to memory ($\overline{MEMR}$/$\overline{MEMW}$) or to a peripheral ($\overline{IOR}$/$\overline{IOW}$).

■APPLICATIONS

DMA control of peripheral equipment such as floppy disks and CRT terminals that require high-speed data transfer.

■PACKAGE DIMENSIONS