

PIN	FUNCTION
1	LOAD
2	VCC
3	SDCLK
4	GND
5	DATA
6	RST
7	NC
8	NC

**Notes:**

1. All dimensions are in millimeters (inches).
2. Tolerance is  $\pm 0.25(0.01)$  unless otherwise noted.

**Features**

- 4 DIGITS, 5\*8 DOT MATRIX.
- 8 BITS SERIAL DATA INPUT REGISTER AND LATCH REGISTER.
- 10\*14 BITS STATIC RAM.
- INTERNAL OSCILLATOR INCLUDED.
- THE RESET INPUT WILL CLEAR THE MULTIPLEX COUNTER, ALL REGISTERS AND USER RAM. THE SOFTWARE RESET WILL CLEAR THE ADDRESS REGISTER AND USER RAM. BOTH RESETS MAKE THE DISPLAY BE BLANK.
- INTERNAL SOFTWARE BRIGHTNESS CONTROL=0%, 6.6%, 13%, 20%, 27%, 40%, 53%, 100%.
- THERE ARE FOUR 100% BRIGHTNESS CONTROL PINS. V1G AND V2G CONTROL THE BRIGHTNESS FOR ANODE DRIVERS G0-G4 WHILE V1Y AND V2Y CONTROL Y0-Y4.
- BUILT-IN DECODERS MULTIPLEXERS AND LED DRIVERS.
- HARDWARE/SOFTWARE CLEAR FUNCTIONS.
- GRAY FACE, WHITE DOT SEGMENT.
- RoHS COMPLIANT.

**Description**

- THE ON-BOARD CMOS HAS A 10\*14 BIT RAM, ONE BIT ASSOCIATED WITH ONE LED, EACH TO GENERATE USER DEFINED CHARACTERS.
- THE PRODUCT IS DESIGNED FOR WORK WITH THE SERIAL PORT OF MOST COMMON MICROPROCESSORS. DATA IS TRANSFERRED INTO THE DISPLAY THROUGH AND SERIAL DATA INPUT (DATA), CLOCKED BY THE SERIAL DATA CLOCK (SDCLK), AND ENABLED BY THE LOAD INPUT LOAD.

■ **TIMING CHART AND TIMING CONDITIONS**

Figure 1. BASIC SEQUENCE

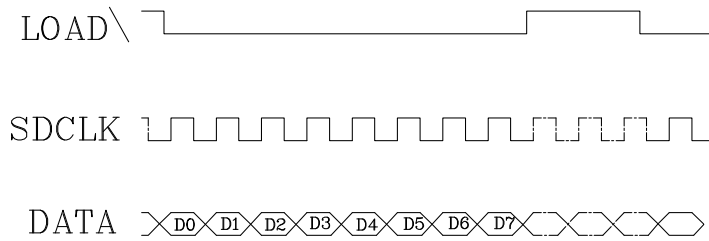
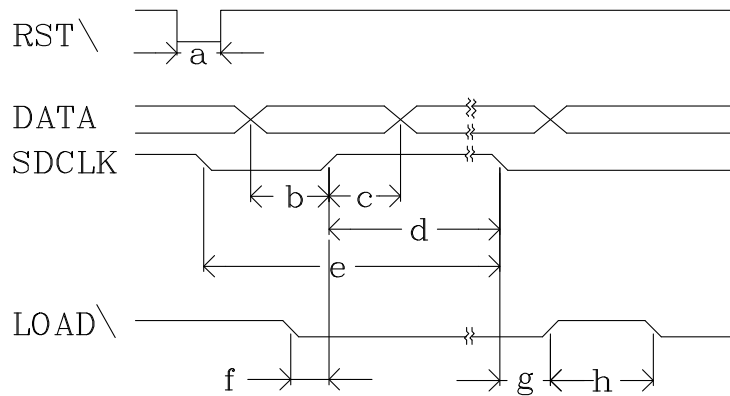
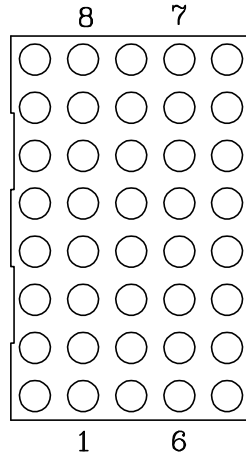


Figure 2. TIMING CONDITIONS.



VCC=+5V Ta=+25°C, UNLESS OTHERWISE SPECIFIED				
ITEM	CHARACTERISTIC	SYMBOL	VALUE	UNIT
a	RESET ACTIVE TIME	Trst	600	nS
b	DATA SETUP TIME	Tds	40	nS
c	DATA HOLD TIME	Tdh	20	nS
d	SERIAL DATA CLOCK PULSE WIDTH	TCLK-PUL	1	uS
e	SERIAL DATA COLCK PERIOD TIME	TCLK-PRD	2	uS
f	LOAD SETUP TIME	Tlds	40	nS
g	LOAD HOLD TIME	Tldh	0	nS
h	TIME BETWEEN LOAD	TBL	600	nS

Figure 3. Top view —— character



**Maximum Ratings**

- DC Supply Voltage..... -0.5 to +5.5 Vdc
- Input Voltage Levels Relative
- To Ground ..... -0.5 to Vcc +0.5 Vdc
- Operating Temperature..... 0 ° C to +45 ° C
- Maximum Solder Temperature 0.063"
- Below Seating Plane, T<5 sec..... 260 ° C

**■ DC ELECTRICAL CHARACTERISTICS**

Ta=+25 ° C, UNLESS OTHER WISE SPECIFIED						
CHARACTERISTIC	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE	Vcc	-	4.5	5.0	5.5	V
LOGIC INPUT LOW	VIL	Vcc=5V	-	-	1.5	V
LOGIC INPUT HIGH	VIH	Vcc=5V	3.5	-	-	V
LOGIC OUTPUT LOW	Vol	Vcc=5V	-	-	1.5	V
LOGIC OUTPUT HIGH	VoH	Vcc=5V	3.5	-	-	V
ANODE COLUMN DRIVER CURRENT	Ic	100% BRIGHTNESS	50	-	-	mA
CATHODE ROW DRIVER CURRENT	Ir	100% BRIGHTNESS	375	-	-	mA
DRIVER LEAKAGE CURRENT	IL	ALL DISPLAY BE BLANK	-	-	1	uA
SERIAL DATA CLOCK FREQUENCY	FSDCLK	Vcc=5V	500	-	-	KHz
SCANNING CLOCK FREQUENCY	FCLK	Vcc=5V	-	344	-	KHz

**YELLOW MMYK60/IC**

DESCRIPTION	Emitting Material	SYMBOL	MIN.	TYP.	UNITS
LUMINOUS INTENSITY CHARACTER AVERAGE (#DISPLAYED ALL DIGITS)	InGaAlP	IV	18000	47090	ucd
DOMINANT WAVELENGTH		$\lambda D$	-	590	nm
PEAK WAVELENGTH		$\lambda P$	-	590	nm
SPECTRAL LINE HALF-WIDTH		$\Delta\lambda 1/2$	-	20	nm

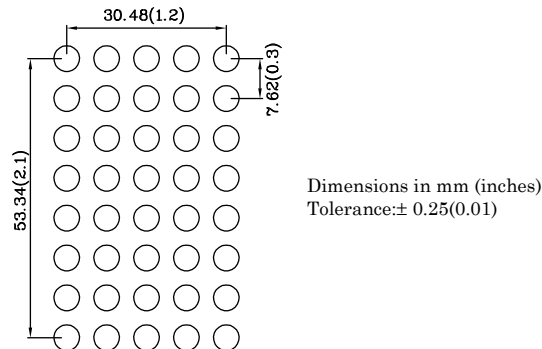
NOTES:

- 1.DOT TO DOT INTENSITY MATCHING AT 100% BRIGHTNESS IS 1.8:1.
- 2.DISPLAYS ARE BINNED FOR HUE AT 2 nm INTERVALS.
- 3.DISPLAYS WITHIN A GIVEN INTENSITY CATEGORY HAVE AN INTENSITY MATCHING OF 1.5:1(MAX).

**PIN ASSIGNMENT**

PIN	FUNCTION	PIN	FUNCTION
1	LOAD\	5	DATA
2	VCC	6	RST\
3	SDCLK	7	NC
4	GND	8	NC

**Figure 4. DOT MATRIX FORMAT.**



**SWITCHING SPECIFICATIONS**

(OVER OPERATING TEMPERATURE RANGE AND VCC=4.5V TO 5.5V)

SYMBOL	DESCRIPTION	MIN	UNITS
TRC	RESET ACTIVE TIME	600	ns
TLDS	LOAD SETUP TIME	40	ns
TDS	DATA SETUP TIME	40	ns
TSDCLK	CLOCK PERIOD	200	ns
TSDCW	CLOCK WIDTH	70	ns
TLDH	LOAD HOLD TIME	0	ns
TdH	DATA HOLD TIME	20	ns
TWR	TOTAL WRITE TIME	19.9	us
TBL	TIME BETWEEN LOADS	600	ns

NOTES:

- 1.TSDCW IS THE MINIMUM TIME THE SDCLK MAY BE LOW OR HIGH.
- 2.THE SDCLK PERIOD MUST BE A MINIMUM OF 200ns.

**DISPLAY COLUMN AND ROW FORMAT**

	C0	C1	C2	C3	C4
ROW0	1	1	1	1	1
ROW1	0	0	1	0	0
ROW2	0	0	1	0	0
ROW3	0	0	1	0	0
ROW4	0	0	1	0	0
ROW5	0	0	1	0	0
ROW6	0	0	1	0	0
ROW7	0	0	1	0	0

1=DISPLAY DOT "ON"  
0=DISPLAY DOT "OFF"

**PAD DESCRIPTIONS**

NAME	TYPE	DESCRIPTION
VCC	POWER	POSITIVE POWER SUPPLY
VSS	GOUND	NEGATIVE POWER SUPPLY
DATA	INPUT	DATA IS A SERIAL DATA INPUT PIN. D0 IS THE LEAST SIGNIFICANT DATA INPUT, AND D7 IS THE MOST SIGNIFICANT DATA INPUT .D0 IS LOADED FIRST AND D7 IS LOADED LAST. THE DATA BITS ARE BROKEN INTO TWO GROUPS CONSISTING OF BITS D0 TO D4 AND D5 TO D7. BITS D0 TO D4 CAN REPRESENT THE DISPLAY ADDRESS, DISPLAY DATA, AND CONTROL WORD DATA. BITS D5 TO D7 WILL REPRESENT THE OPERATION CODE FOR DIGIT ADDRESS, COLUMN DATA CONTROL, CONTROL WORD ADDRESS OR SOFTWARE CLEAR.
SDCLK	INPUT	SDCLK (SERIAL DATA CLK) IS USED TO LOAD DATA INTO THE 8 BIT SERIAL DATA REGISTER. THE DATA IS TRANSFERRED INTO THE SERIAL DATA REGISTER ON A LOW TO HIGH TRANSITION.
RST\	INPUT	RESET WHEN LOW, THE MULTIPLEX COUNTER, ALL REGISTERS AND USER RAM WILL BE CLEARED. THE DISPLAY WILL BE BLANK.
LOAD\	INPUT	LOAD\ IS A ACTIVE LOW ENABLE INPUT. WHEN LOAD\ IS LOW, DATA CAN BE CLOCKED INTO THE 8 BIT SERIAL SHIFT REGISTER. WHEN LOAD\ GOES HIGH THE CONTENTS OF THE 8 BIT SERIAL SHIFT REGISTER WILL BE EVALUATED BY THE INTERNAL CIRCUITRY.
CLK	BIDIRECTION	CLK IS AN OSCILLATOR OUTPUT WHICH CAN BE OUERDRIVEN FOR TESE.

**COLUMN DATA RANGES**

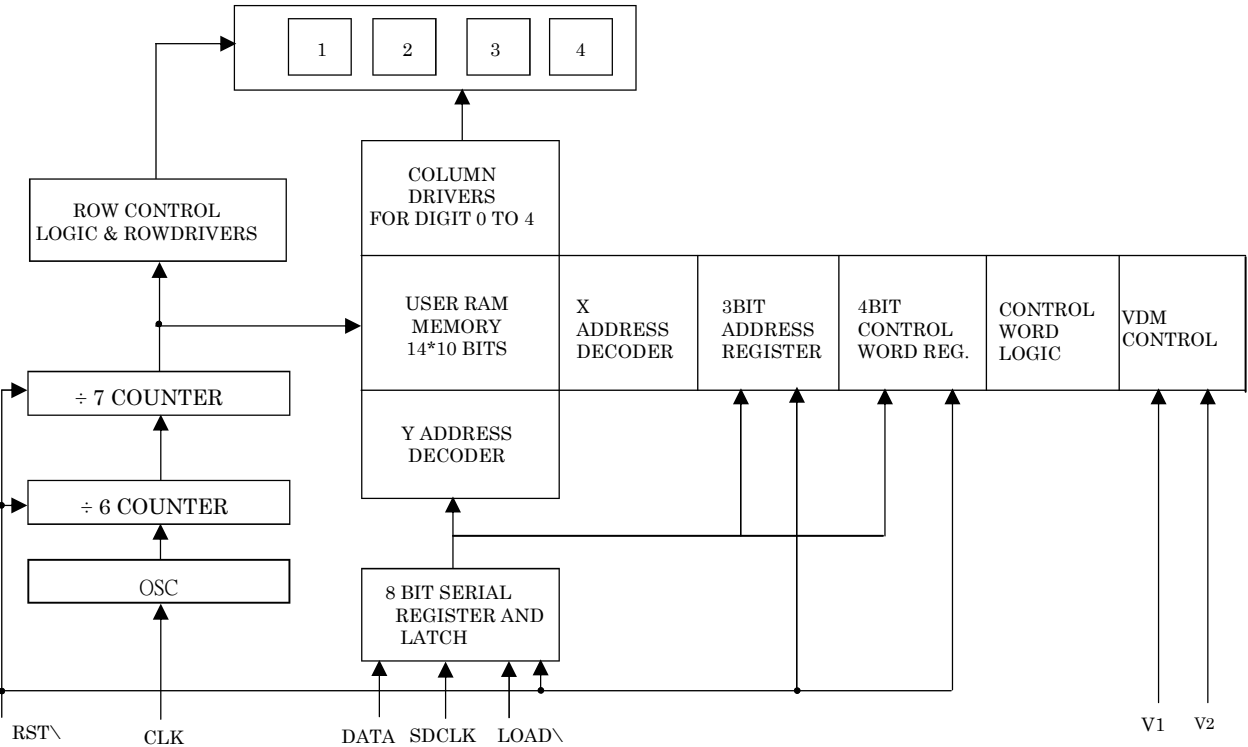
ROW0	00H TO 1FH	ROW4	00H TO 1FH
ROW1	00H TO 1FH	ROW5	00H TO 1FH
ROW2	00H TO 1FH	ROW6	00H TO 1FH
ROW3	00H TO 1FH	ROW7	00H TO 1FH

**Operation of the MMYK60/IC**

The MMYK60/IC display consists of a CMOS IC containing control logic and drivers for one 5x8 character. These components are assembled in a compact plastic package. Individual LED dot addressability allows the user great freedom in creating special characters or mini-icons. The user Definable Character Set examples illustrate 26 different character. The serial data interface provides a highly efficient interconnection between the display and the mother board.

The on-board CMOS IC is the electronic heart of the display. The IC accepts decoded serial data, which is stored in the internal RAM. Asynchronously the RAM is read by the character multiplexer at a strobe rate that results in a flicker free display. Figure 7 shows the functional of the IC. These include: the input serial data register and control logic, user RAM memory 14\*10 bits, X address decoder, 3 bit address register, 4 bit control word register, control word logic, VDM control, row control logic & row drivers.

Figure 5. FUNCTION BLOCK DIAGRAM



**FUNCTION DESCRIPTION**

(a) BASIC DESTRUCTION SET:

INSTRUCTION	OP CODE	ADDRESS	DATA	COMMENTS
LCD	0 X X		D4 D3 D2 D1 D0	LOAD COLUMN DATA
LDA	1 0 1	X X A2 A1 A0		LOAD DIGIT ADDRESS
SCL	1 1 0	0 0 0 0 0		SOFTWARE CLEAR
LCWD	1 1 1		X D3 D2 D1 D0	LOAD CONTROL WORD DATA

(b) FULL INSTRUCTION SET:

INSTRUCTION	OP CODE	ADDRESS	DATA	COMMENTS
LCD	0 X X		D4 D3 D2 D1 D0	LOAD COLUMN DATA
LDA0	1 0 1	X X 0 0 0		LOAD DIGIT ADDRESS 0
LDA1	1 0 1	X X 0 0 1		LOAD DIGIT ADDRESS 1
LDA2	1 0 1	X X 0 1 0		LOAD DIGIT ADDRESS 2
LDA3	1 0 1	X X 0 1 1		LOAD DIGIT ADDRESS 3
LDA4	1 0 1	X X 1 0 0		LOAD DIGIT ADDRESS 4
LDA5	1 0 1	X X 1 0 1		LOAD DIGIT ADDRESS 5
LDA6	1 0 1	X X 1 1 0		LOAD DIGIT ADDRESS 6
LDA7	1 0 1	X X 1 1 1		LOAD DIGIT ADDRESS 7
SCL	1 1 0	0 0 0 0 0		SOFTWARE CLEAR
LCWD	1 1 1		X D3 D2 D1 D0	LOAD CONTROL WORD DATA

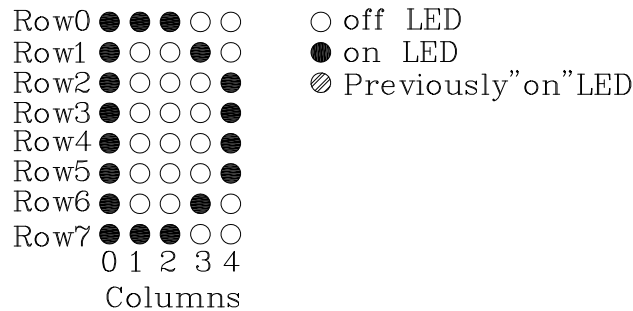
(c) LCD (LOAD COLUMN DATA)

BELOW IS THE GENERAL FORMAT FOR LOADING COLUMN DATA.

DISPLAY COLUMN AND ROW FORMAT

D7	D6	D5	D4	D3	D2	D1	D0
	OP CODE		COLUMN DATA C0	COLUMN DATA C1	COLUMN DATA C2	COLUMN DATA C3	COLUMN DATA C4

Figure 6. Row and Column locations



TO LOAD INTO THE USER RAM YOU MUST LOAD IN AN ADDRESS FOR THE DIGIT YOU WITH TO WRITE TO, THEN LOAD IN THE COLUMN DATA FOR THAT DIGIT. THE USER MUST LOAD ALL SEVEN ROWS OF COLUMN DATA FOR THE CHOSEN DIGIT, STARTING WITH ROW0 AND ENDING WITH ROW6. IF THE USER MAKES A MISTAKE, RELOAD THE DIGIT ADDRESS AND TRY AGAIN. THE SEQUENCE OF INSTRUCTIONS IS SHOWN BELOW.

INSTRUCTION SEQUENCE TO LOAD ONE 5X8 DISPLAY			
INSTRUCTION	OP CODE	COLUMN DATA	COMMENTS
LCD	0 X X	C0 C1 C2 C3 C4	LOAD COLUMN TO ROW 0
LCD	0 X X	C0 C1 C2 C3 C4	LOAD COLUMN TO ROW 1
LCD	0 X X	C0 C1 C2 C3 C4	LOAD COLUMN TO ROW 2
LCD	0 X X	C0 C1 C2 C3 C4	LOAD COLUMN TO ROW 3
LCD	0 X X	C0 C1 C2 C3 C4	LOAD COLUMN TO ROW 4
LCD	0 X X	C0 C1 C2 C3 C4	LOAD COLUMN TO ROW 5
LCD	0 X X	C0 C1 C2 C3 C4	LOAD COLUMN TO ROW 6

(d) LDA (LOAD DIGIT ADDRESS)

THE DIGIT ADDRESS REGISTER IS A 3 BIT WRITE ONLY REGISTER WHICH SELEXTS THE DIGIT THAT THE ROW AND COLUMN DATA WILL BE WRITTEN TO.

BELOW IS THE GENERAL FORMAT OF THE DIGIT ADDRESS REGISTER.

DIGIT ADDRESS RESISTER FORMAT

D7	D6	D5	D4	D3	D2	D1	D0
OP CODE			X	X	A2	A1	A0

BELOW IS THE XOMPLETE DIGIT ADDRESS REGISTER TRUTH TABLE.

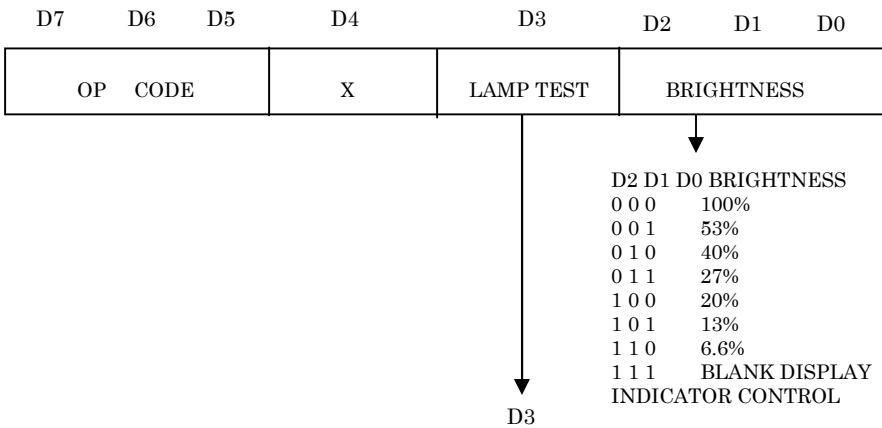
DIGIT ADDRESS RESISTER TRUTH TABLE			
INSTRUCTION	OP CODE	ACCOUNTS	COMMENTS
LAD0	1 0 1	X X 0 0 0	LOAD DIGIT ADDRESS 0
LAD1	1 0 1	X X 0 0 1	LOAD DIGIT ADDRESS 1
LAD2	1 0 1	X X 0 1 0	LOAD DIGIT ADDRESS 2
LAD3	1 0 1	X X 0 1 1	LOAD DIGIT ADDRESS 3

**(e) SCL (SOFTWARE CLEAR)**

THE SCL WILL XLEAR THE ADDRESS REGISTER AND USER RAM. THE DISPLAY WILL BE BLANK.

**(f) LCWD (LOAD CONTROL WORD)**

THE CONTROL WORD IS A 4 BIT WRITE ONLY REGISTER WHICH CONTROLS THE DISPLAY ATTRIBUTES. BELOW ARE THE TRUTH TABLES WHICH DEFINE EACH BIT IN THE CONTROL WORD REGISTER.



THE DISPLAY CAN BE PROGRAMMED TO VARY BETWEEN BLANK, 6.6%, 13%, 20%, 27%, 40%, 53% AND FULL BRIGHTNESS. BITS D0, D1, D2 CONTROL THE BRIGHTNESS OF THE CHARACTERS. WHEN THE BRIGHTNESS IS SET TO 0%, THE DISPLAY WILL BE BLANK. WHILE THE CHIP IS IN THE BLANK DISPLAY MODE, THE RAM CAN BE LOADED WITH DATA.

DISPLAY BRIGHTNESS		
OP CODE	D4 D3 D2 D1 D0	CHARACTER BRIGHTNESS
1 1 1	X 0 0 0 0	100% BRIGHTNESS
1 1 1	X 0 0 0 1	53% BRIGHTNESS
1 1 1	X 0 0 1 0	40% BRIGHTNESS
1 1 1	X 0 0 1 1	27% BRIGHTNESS
1 1 1	X 0 1 0 0	20% BRIGHTNESS
1 1 1	X 0 1 0 1	13% BRIGHTNESS
1 1 1	X 0 1 1 0	6.6% BRIGHTNESS
1 1 1	X 0 1 1 1	BLANK DISPLAY

INDICATORS IN-R AND IN-G FOLLOW THE DISPLAY BRIGHTNESS.

**(g) DEVICE OPERATION**

TO LOAD DATA INTO THE 8-BIT SERIAL SHIFT REGISTER DO THE FOLLOWING:

- 1) POWER UP THE CHIP.
- 2) BRING RST\ LOW, THIS WILL CLEAR THE MULTIPLEX COUNTER, ADDRESS REGISTER, CONTROL WORD REGISTER, USER RAM AND DATA REGISTER. THE DISPLAY WILL ALSO BE BLANK. AFTER 600ns OR MORE BRING HIGH.
- 3) CHECK THE TIMING DIAGRAM FOR THE PROPER RELATIONSHIP BETWEEN DATA, SDCLK, AND LOAD\.
- 4) LOAD THE DIGIT ADDRESS INTO THE SHIFT REGISTER.
- 5) LOAD DISPLAY COLUMN DATA FOR THE ABOVE ADDRESSED DIGIT. THE USER MOST LOAD ALL SEVEN ROWS OF COLUMN DATA FOR THE CHOSEN DIGIT, STARTING WITH ROW0 AND ENDING WITH ROW6. IF THE USER MAKES A MISTAKE, RELOAD THE DIGIT ADDRESS AND TRY AGAIN.
- 6) REPEAT STEP 4 AND 5 FOR EACH DIGIT AND CHARACTER TO BE DISPLAYED.
- 7) LOAD THE CONTROL REGISTER WITH YOUR BRIGHTNESS IF LESS THAN 100% BRIGHTNESS IS REQUIRED.

THE FORMAT FOR EACH OF THE FOUR 8-BIT INSTRUCTIONS IS AS FOLLOWS:

D7	D6	D5	D4	D3	D2	D1	D0
OP CODE				ADDRESS / DATA			

8-BIT SERIAL SHIFT REGISTER.

D0 IS THE LEAST SIGNIFICANT DATA INPUT, AND D7 IS THE MOST SIGNIFICANT DATA INPUT. D0 IS LOADED FIRST AND D7 LOADED LAST. THE DATA BITS ARE BROKEN INTO TWO GROUPS CONSISTING OF BITS D0 TO D4 AND D5 TO D7. BITS D0 TO D4 CAN REPRESENT THE DIGIT ADDRESS, DISPLAY COLUMN DATA, AND CONTROL WORD FUNCTIONS. BITS D5 TO D7 WILL REPRESENT THE OPERATION CODE FOR THE DIGIT ADDRESS, COLUMN DATA CONTROL, CONTROL WORD ADDRESS, OR SOFTWARE CLEAR.

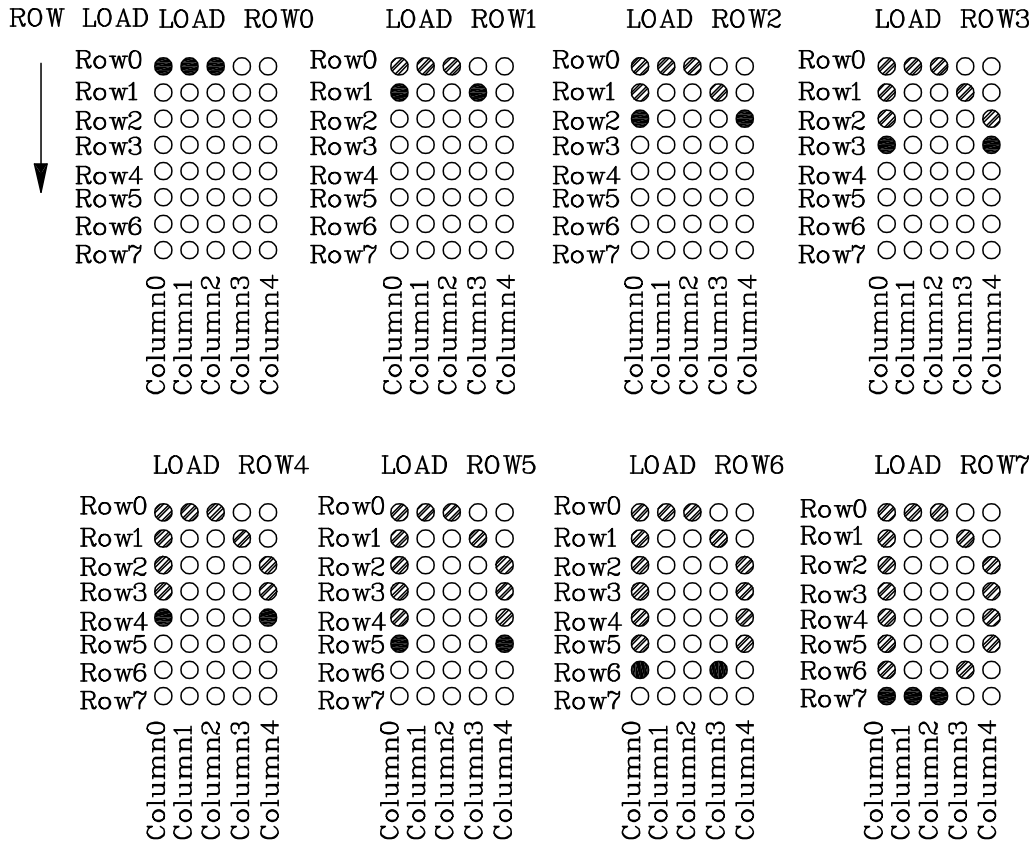
**DATA CONTENTS FOR THE DISPLAY IN A “K”.**

STEP	D7 D6 D5	D4 D3 D2 D1 D0	FUNCTION
A	1 1 0	0 0 0 0 0	CLEAR
B	1 1 1	X 0 X X X	BRIGHTNESS SELECT
ADDRESS(2)	1 0 1	X X 0 X 0	LOAD DIGIT ADDRESS0(2)
1	0 X X	1 0 0 0 1	ROW 0 (K)
2	0 X X	1 0 0 1 0	ROW 1 (K)
3	0 X X	1 0 1 0 0	ROW 2 (K)
4	0 X X	1 1 0 0 0	ROW 3 (K)
ADDRESS1(3)	0 X X	X X 0 X 1	LOAD DIGIT ADDRESS1(3)
5	0 X X	1 1 0 0 0	ROW 4 (K)
6	0 X X	1 0 1 0 0	ROW 5 (K)
7	0 X X	1 0 0 1 0	ROW 6 (K)
8	0 X X	1 0 0 0 1	ROW 7 (K)

Notes:

1. If the display is already reset at Power Up, these is no for Software Clear.
2. X is 0 or 1.

**Figure 7. Row Strobing**



**MULTIPLEXER AND DISPLAY DRIVER**

The character is row multiplexed with RAM resident column data. The strobe rate is established by the internal or external MUX Clock rate. The MUX Clock frequency is divided by a 320 counter chain. This results in a typical strobe rate of 750 Hz. By pulling the CLK connection (pin 3), The maximum external MUX Clock frequency should be limited to 1 MHz.

An asynchronous hardware Reset (pin6) is also provided. Bringing this pin low will clear the Character address Register, Control Word Register, RAM, and blanks the display.

**ELECTRICAL & MECHANICAL CONSIDERATIONS  
INTERCONNECT CONSIDERATIONS**

Optimum product performance can be had when the following electrical and mechanical recommendations are adopted. The MMYK60/IC IC is constructed in a high speed CMOS process consequently high speed noise on the SERIAL DATA, SERIAL DATA CLOCK, LOAD\ and RESET\ lines may cause incorrect data to be written into the serial shift register. Adhere to transmission line termination procedures when using fast line drivers and long cables (>10cm).

Good digital grounds (pin 4) and power supply decoupling (pin 2) will insure that Icc (<400mA peak) switching currents do not generate localized ground bounce. Therefore it is recommended that each display package use a 0.1 uF and 20 uF capacitor between Vcc and ground.

When the internal MUX Clock is being used connect the CLK pin to Vcc. In those applications where RESET\ will not be connected to the system's reset control, it is recommended that this pin be connected to the center node of a series 0.1 uF and 100KΩ RC network. Thus upon initial power up the RESET\ will be held low for 10 ms allowing adequate time for the system power supply to stabilize.

Figure 8. MMYK60/IC Intel 8031 microprocessor( using serial port in mode 0).

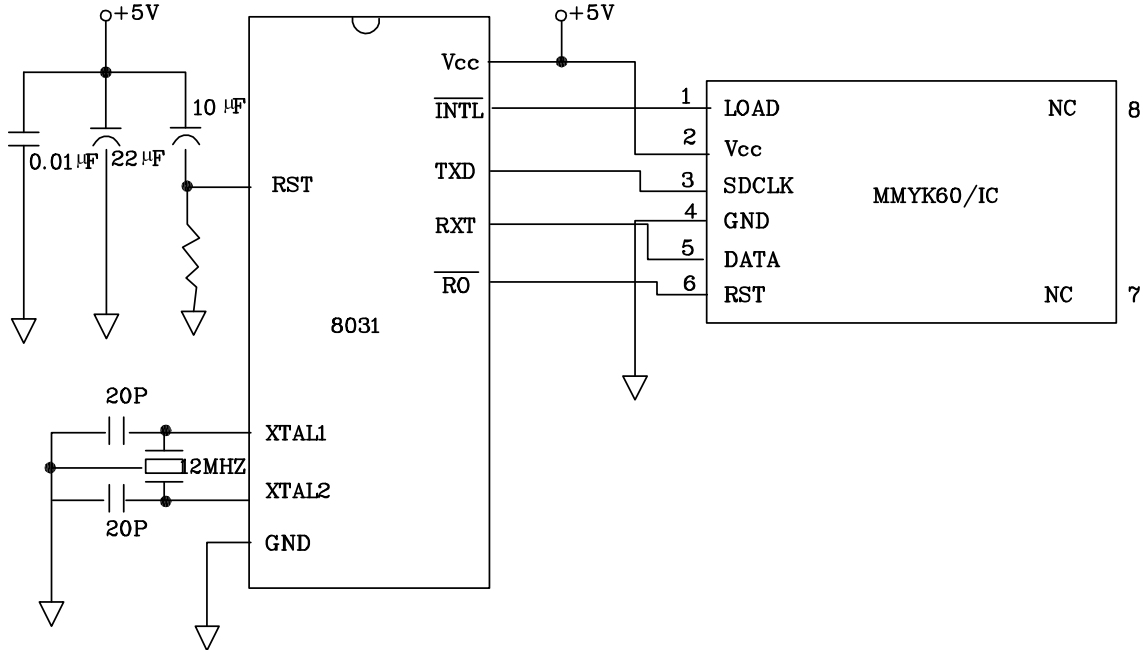
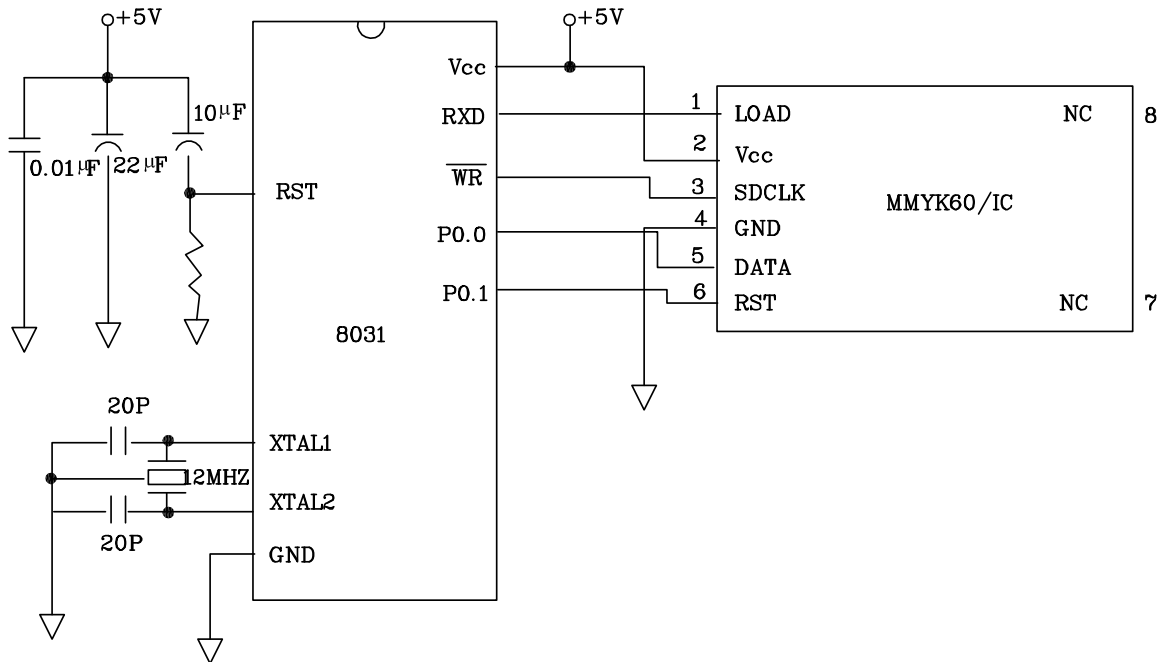


Figure 9. MMYK60/IC interface to Intel 8031 microprocessor  
(Using one of parallel port as serial input).



**MICROPROCESSOR INTERFACE**

The microprocessor interface is through the serial port, SPI port or one out of eight data bit parallel port and also control lines SDCLK and LOAD\.

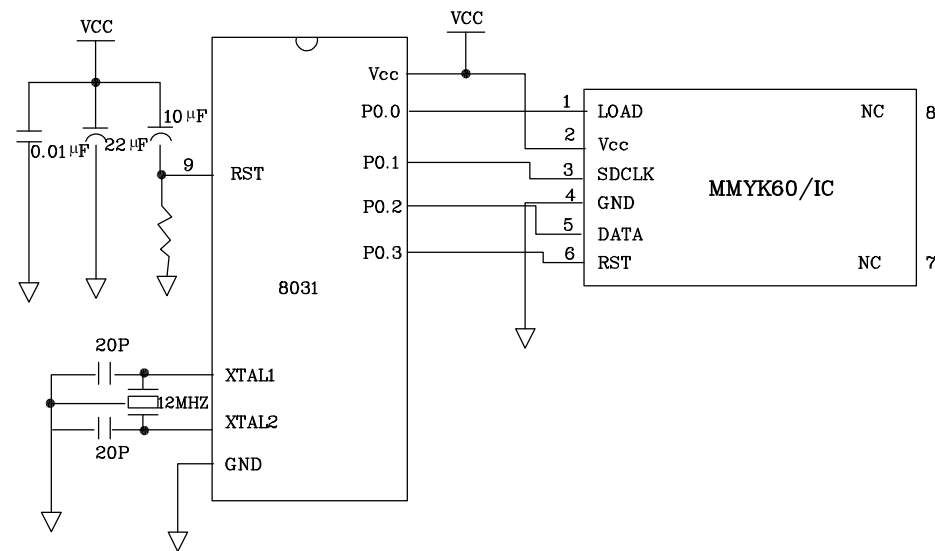
**POWER UP SEQUENCE**

Upon power up display will come on at random. Thus the display should be reset at power-up. User RAM is set to zero (display blank) the Control Word is set to zero (100% brightness with Lamp Test off) and the internal counters are reset.

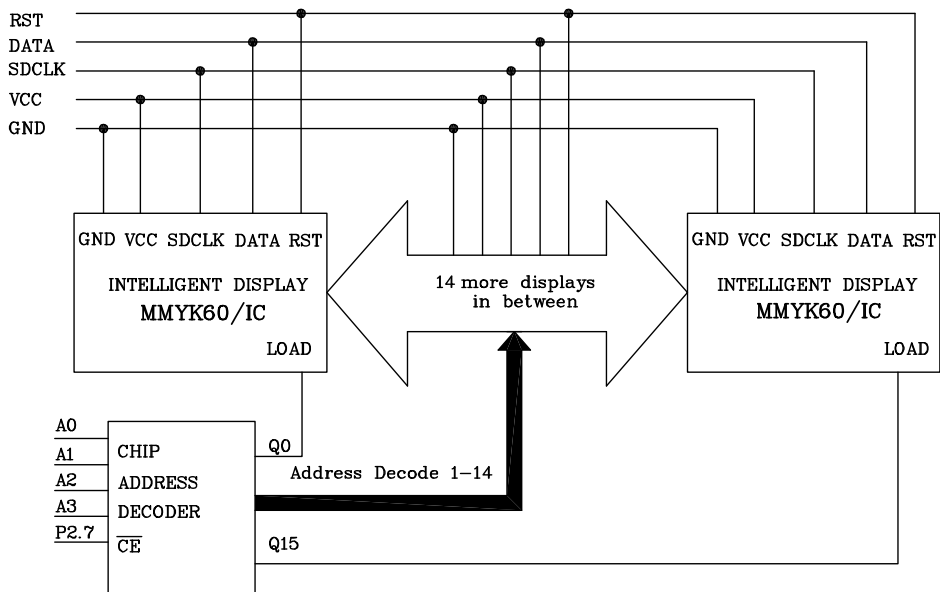
**CASCADING MULTIPLE DISPLAYS**

Multiple displays can be cascaded using the CLK pins as shown below. All Vcc, GND, RST\, SDCLK pins. Use RST\ to synchronize all display counters.

**Figure 10. MMYK60/IC INTERFACE WITH INTEL 8031 MICROPROCESSOR.**



**Figure 11. CASCADING MULTIPLE DISPLAYS**





5X8 DOT MATRIX SERIAL INPUT DOT ADDRESSABLE  
INTELLIGENT DISPLAY DEVICES

User Definable Character Examples

(Upper case alphabets)

HEX CODE	HEX CODE	HEX CODE	HEX CODE	HEX CODE
04H	1EH	06H	1CH	1FH
0AH	11H	09H	12H	10H
11H	11H	10H	11H	10H
11H	1EH	10H	11H	1FH
1FH	11H	10H	11H	10H
11H	11H	10H	11H	10H
11H	11H	09H	12H	10H
11H	1EH	06H	1CH	1FH
1FH	06H	11H	1FH	1FH
10H	09H	11H	04H	04H
10H	10H	11H	04H	04H
1FH	10H	1FH	04H	04H
10H	13H	11H	04H	04H
10H	11H	11H	04H	04H
10H	09H	11H	04H	14H
10H	06H	11H	1FH	08H
11H	10H	11H	11H	0EH
12H	10H	1BH	11H	11H
14H	10H	15H	19H	11H
18H	10H	15H	15H	11H
18H	10H	11H	15H	11H
14H	10H	11H	13H	11H
12H	10H	11H	11H	11H
11H	1FH	11H	11H	0EH
1EH	0EH	1EH	0EH	1FH
11H	11H	11H	11H	04H
11H	11H	11H	10H	04H
1EH	11H	1EH	11H	04H
10H	11H	18H	11H	04H
10H	15H	14H	11H	04H
10H	13H	12H	11H	04H
10H	0DH	11H	0EH	04H
11H	11H	11H	11H	11H
11H	11H	11H	11H	11H
11H	11H	11H	0AH	11H
11H	11H	11H	04H	0AH
11H	11H	15H	0AH	04H
11H	11H	15H	11H	04H
11H	0AH	1BH	11H	04H
0EH	04H	11H	11H	04H
1FH				
01H				
02H				
04H				
08H				
10H				
10H				
1FH				

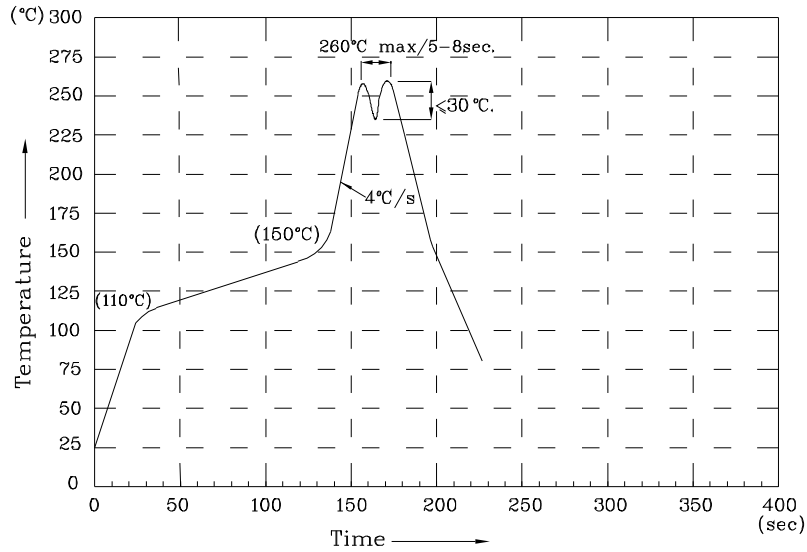


5X8 DOT MATRIX SERIAL INPUT DOT ADDRESSABLE INTELLIGENT DISPLAY DEVICES

User Definable Character Examples\*  
Lower case alphabets

HEX CODE	HEX CODE	HEX CODE	HEX CODE	HEX CODE
00H	10H	00H	01H	00H
00H	10H	00H	01H	00H
0EH	10H	0EH	01H	0EH
12H	1EH	11H	0FH	11H
12H	11H	10H	11H	1EH
12H	11H	10H	11H	10H
12H	11H	11H	11H	11H
0DH	1EH	0EH	0FH	0EH
03H	00H	10H	04H	04H
04H	00H	10H	00H	00H
04H	0EH	10H	04H	04H
1FH	11H	1EH	0CH	0CH
04H	0FH	11H	04H	04H
04H	01H	11H	05H	04H
04H	11H	11H	06H	04H
04H	0EH	11H	04H	18H
10H	08H	00H	00H	00H
10H	08H	00H	00H	00H
1EH	08H	1EH	1EH	0EH
11H	08H	15H	11H	11H
1EH	08H	15H	11H	11H
14H	0AH	15H	11H	11H
12H	0CH	15H	11H	11H
11H	08H	15H	11H	0EH
00H	00H	00H	00H	00H
00H	00H	00H	00H	04H
1EH	0FH	17H	0FH	04H
11H	11H	18H	10H	1FH
1EH	0FH	10H	0EH	04H
10H	01H	10H	01H	04H
10H	01H	10H	11H	05H
10H	01H	10H	0EH	02H
00H	00H	00H	00H	00H
00H	00H	00H	00H	00H
12H	11H	11H	11H	11H
12H	11H	11H	0AH	11H
12H	11H	15H	04H	0FH
12H	11H	15H	0AH	01H
12H	0AH	1BH	11H	01H
0DH	04H	11H	11H	0EH
00H				
00H				
1FH				
02H				
04H				
08H				
10H				
1FH				

Wave Soldering Profile For Lead-free Through-hole LED.



NOTES:

- 1.Recommend the wave temperature 245°C~260°C.The maximum soldering temperature should be less than 260°C.
- 2.Do not apply stress on epoxy resins when temperature is over 85 degree°C.
- 3.The soldering profile apply to the lead free soldering (Sn/Cu/Ag alloy).
- 4.No more than once.

Remarks:

If special sorting is required (e.g. binning based on luminous intensity/ luminous flux , or wavelength), the typical accuracy of the sorting process is as follows:

1. Wavelength: +/-1nm
2. Luminous Intensity/ luminous flux: +/-15%

Note: Accuracy may depend on the sorting parameters.