

ML67Q4050/Q4060 Series

32-Bit ARM®-Based General Purpose Microcontroller

General Purpose

DESCRIPTION

The Oki ML67Q4050/Q4060 Series of microcontrollers have been added to Oki's growing family of ARM based microcontrollers. These devices are the world's smallest packaged ARM processors. They contain a 33.33-MHz, 32-bit ARM7TDMI™ core with either

64KBytes or 128KBytes of 32-bit wide zero-wait state FLASH memory and 16KBytes of SRAM. The devices also contain multiple serial interfaces, like I²C, I²S, SPI, and UARTs (supporting 9-bit communications), along with many other peripheral functions.

Features

- ARM7TDMI™ CPU
 - JTAG debug function
- Internal Memory
 - 64KB or 128KB 32-bit wide FLASH, zero wait state
 - 16KBytes SRAM
 - Boot loader
- External Memory Controller (ML67Q4050/51 only)
 - ROM, RAM and I/O banks
 - 8,16 or 32-bit wide accesses
- Power Supply
 - 2.5V V_{DD_CORE}
 - Selectable 2.5V to 3.3V V_{DD_IO}
- Programmable Timers
 - 16-bit System Timer
 - Six 16-bit Flexible Timers
 - Auto reload, input capture, compare output
- 16-bit Watchdog timer
 - Selectable interrupt or reset
- Two DMAC Channels
- Four 10-bit A/D converter channels
- Two UART channels
 - 16550A-compatible
 - Independent 16-bit Tx and Rx FIFOs
 - Supports 9-bit mode
- I²C
 - Conforms to I²C bus specification
 - Multi-master support
- SIO
 - Full duplex operation with built in baud rate generator
- I²S
 - Conforms to the I²S (the Inter-IC Sound) specification for DAC/ADC IF
 - Supports master/slave modes
 - Channel data length 16/18/20/24-bit (CPU interface is 16 bits)
 - One 256 x 16 shared FIFO
 - Master clock output
- Two SPI channels
 - Selectable master/slave
 - Bus Collision Detection
 - Supports 8-bit and 16-bit transfers
- Clocks
 - Main clock = 33.333 MHz (Max)
 - RTC clock = 32.768 kHz
 - Ring Oscillator
- Power Management
 - Low-power mode
 - Halt mode
 - Stop Mode
 - Clock divider can be dynamically changed during operation
- Packages
 - 64-pin WCSP (the world's smallest package)
 - 64-pin TQFP
 - 84-pin LFBGA
 - 144-pin LQFP (ML67Q4050/51 Only)

Typical Applications

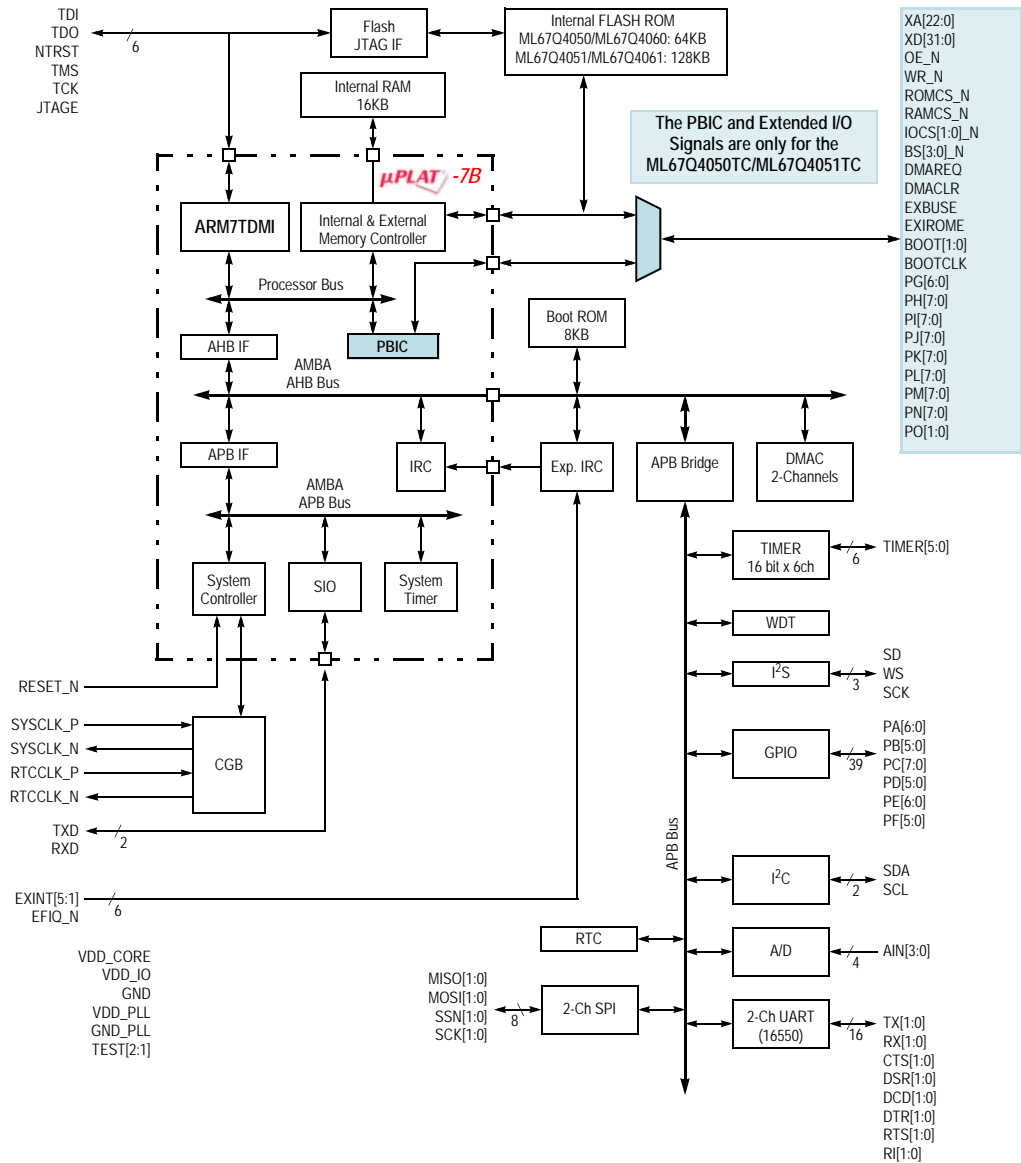
- Consumer, medical, and communications applications where small package size is important.

Product Selector

Part Number	Flash ROM	Package
ML67Q4050TC	64KB	144-Pin LQFP
ML67Q4051TC	128KB	
ML67Q4060TB	64KB	64-Pin TQFP
ML67Q4061TB	128KB	

Part Number	Flash ROM	Package
ML67Q4060LA	64KB	84-Pin LFBGA
ML67Q4061LA	128KB	
ML67Q4060HA	64KB	64-Pin WCSP
ML67Q4061HA	128KB	

Block Diagram



FUNCTIONAL DESCRIPTION

- CPU
 - 32-bit RISC CPU (ARM7TDMI)
 - Little endian byte order
 - Maximum operating frequency: 33.33 MHz
 - Instruction set: Free switching between a highly efficient 32-bit instruction set, and a 16-bit subset offering higher object code density
 - General-purpose registers: 31 32-bit registers
 - Barrel shifter: Simultaneous ALU and barrel shift operations in the same instruction
 - Multiplier (32-bit x 8-bit)
 - JTAG interface for debugging
- Built-in Memory
 - SRAM: 16KBytes (4K x 32 bits), 1-cycle access
 - Built-in Flash ROM: 128KBytes (ML67Q4051, ML67Q4061) or 64KBytes (ML67Q4050, ML67Q4060), 1-cycle access, connected to the processor bus Flash ROM programming cycle count: 100 (max.)
 - Boot ROM: 8KBytes
- External Memory Controller (only for ML67Q4050/51)
 - Programmable access timing setting for each space
 - ROM (Flash) access function
 - Supports 1 bank x 8KBytes ROM space.
 - Supports 16-bit and 32-bit devices
 - Supports flash memories
 - Supports page accessing
 - SRAM access function
 - Supports 1 bank x 8MBytes SRAM space.
 - Supports 16-bit and 32-bit devices.
 - Supports asynchronous SRAM.
 - External I/O access function
 - Supports 2-bank I/O space.
 - Supports 8-bit, 16-bit, and 32-bit devices.
 - Supports asynchronous wait from external devices.
 - Allows address setup in units of single cycles, RE/WE pulse, and data-off timing setting.
- Interrupt Controller
 - One fast interrupt (FIQ) source (external)
 - 31 interrupt (IRQ) sources (40 interrupt sources for ML67Q4050/51)
 - Independent masking for each FIQ and IRQ source
 - Independent interrupt priority level settings for each IRQ source
 - Priority control blocking IRQ requests with priority levels at or below those for interrupt requests currently being processed
- System Timers
 - One 16-bit system timer
- Flexible Timers
 - Six 16-bit flexible timers
 - Auto Reload Timer (ART) / Compare Out (CMO) / Pulse Width Modulation (PWM) / Capture (CAP)
- Watchdog Timer
 - One 16-bit timer
 - Choice of interrupt or reset on overflow
 - Maximum period: 8.94 sec. (at Peripheral clock = 30 MHz)
 - Change watch dog period while running counting
 - Setting of period asserting reset signal (RSTOUT_N)
- SIO
 - Full duplex asynchronous operation
 - Built-in baud-rate generator
- DMA Controller
 - Two channels
 - Selectable DMA request source, source peripheral: I²S, I²C, UART, SPI (External DMA request is available only for ML67Q4050/51)
 - Choice of fixed or round robin mode for channel priority order
 - Choice of cycle-steal or burst mode for requesting bus access
 - Choice of software or external DMA transfer requests
 - Maximum transfer count: 65,535
 - Data transfer sizes: 8-, 16-, and 32-bit
- GPIO
 - Three 20-mA sink pins
 - Individual settings for pin I/O direction
 - Individual settings for pin interrupt requests
 - One 8-bit port, two 7-bit ports, three 6-bit ports
 - For ML67Q4050/51 series:
 - Eight 8-bit ports
 - Three 7-bit ports
 - Three 6-bit ports
 - One 5-bit port
 - For ML67Q4060/61 series:
 - One 8-bit ports
 - Two 7-bit ports
 - Three 6-bit ports
- Analog-to-Digital Converter
 - Four channels of 10-bit resolution, each using consecutive comparison
 - Sample and hold function
 - Choice of scan or select operation
 - Conversion time: 20 μ s (MAX 50k-sample/s)
 - DNL (MAX) = ± 6.0 LSB
 - INL (MAX) = ± 6.0 LSB
 - Zero Scale Error (MAX) = ± 8.0 LSB
 - Full Scale Error (MAX) = ± 8.0 LSB
- UART
 - Two 16550A-compatible asynchronous communications
 - Independent 16-byte FIFOs for transmit and receive operations
 - Full duplex operation
 - Built-in baud-rate generator
 - Supports DMA transfers
- I²C
 - Controller in conformity of I²C bus specification ver2.1
 - Multi Master support
 - Supports fast mode (400 kbps), standard mode (100 kbps)
 - Supports 7-bit, 10-bit address
 - Supports DMA transfers
- I²S Transmitter/Receiver
 - Conforms to I²S (the Inter-IC Sound) specification for DAC/ADC I/F
 - Three-line communication, bit clock (SCK), word clock (WS), serial data (SD)
 - Supports Master/Slave
 - Word Clock: 32fs / 64fs
 - Channel data length: 16/18/20/24-bit (16-bit CPU I/F)
 - Support 1-bit delay, reverse L-Ch and R-Ch
 - Supports DMA
 - One 256 x 16-bit FIFO shared Transmitter/Receiver
 - Master clock output

- SPI
 - Two channels of full duplex serial-parallel Interface.
 - Selectable Master/Slave
 - Independent 16 entry x 16-bit FIFOs
 - Built-in Baud-rate generator
 - Support 8-bit width and 16-bit width transfers
 - Supports DMA operation
- CLOCK
 - Main clock oscillator is 33.33 MHz (Max)
 - RTC clock oscillator is 32.768 kHz Clock
 - Ring Oscillator
- RTC
 - One second generated from 32.768 kHz
 - Built-in 32-bit counter with one second clock
 - Interrupt on 32-bit comparison
- Power Management
 - Low-power mode
 - HALT mode: Stop the clock supply to CPU and other key components
 - STOP mode: Stop the clock supply to CPU and all peripherals except RTC
 - Control the clock supply to each peripherals
 - Clock change is dynamically possible in the division ratio of clock input frequency.
- ML67Q4050/51 Package
 - 144-pin LQFP (LQFP144-P-2020-0.50-ZK)
- ML67Q4060/61 Packages
 - 64-pin WCSP (P-VFBGA64-5.09x4.84-0.50-W)
 - Occupies less than 25 square millimeters
 - 64-pin TQFP (TQFP64-P-1010-0.50-K)
 - 84-pin LFBGA (P-LFBGA84-0909-0.80)

Figure 2. 84-Pin Plastic LFBGA

	A	B	C	D	E	F	G	H	J	K	
10	GND	NC	NC	VDD_IO	PB1/ /RX0	PE4/ SD	PF2/ TIMER2/ CTS1	PF5/ TIMER5/ EXINT5	NC	VDD_CORE	10
9	PB3/ RX1/ EXINT1	NC	VDD_CORE	PB0/ TX0	BOOT0/ PE3/ MCLK	PF1/ TIMER1/ RTS0	PF4/ TIMER4/ EXINT4	GND	GND	NC	9
8	VDD_IO	PB4/ SCL/ TXD	PB5/ SDA/ RXD	GND	PB2/ TX1/ EFIQ_N	PF0/ TIMER0/ CTS0	PF3/ TIMER3/ RTS1	VDD_IO	PC0/ MISO0/ DSR0	BOOTCLK/ PD5	8
7	PE1	PE0	GND	ML67Q4060/61 84-Pin LFBGA (TOP VIEW)				PC1/ MOSI0/ DTR0	PC2/ SCK0/ RIO	VDD_IO	7
6	VDD_IO	GND	PE2					PC4/ MISO1/ DSR1	PC5/ MOSI1/ DTR1	PC3/ SSN0/ DCD0	6
5	PD2/ AIN2	PD0/ AIN0/ EXINT2	PD1/ AIN1/ EXINT3					GND	GND	RESET_N	5
4	TEST2	PD3/ AN3	TEST1					PC6/ SCK1/ RI1	PC7/ SSN1/ DCD1	RSTOUT_N/PA6/ MCLK	4
3	NC	GND	GND_PLL	RTCCLK_N	GND	TCK/ PA0	TDO/ PA3	VDD_IO	PE5/ WS	BS/ PD4	3
2	NC	NC	GND_PLL	VDD_PLL	GND	SYSCLK_N	TDI/ PA2	NTRST/ PA4	VDD_CORE	PE6/ SCK	2
1	VDD_CORE	VDD_IO	VDD_PLL	RTCCLK_P	SYSCLK_P	TMS/ PA1	VDD_IO	JTAGE/ PA5	NC	GND	1
	A	B	C	D	E	F	G	H	J	K	

NOTES:

- For pins that have multiple functions, the signals are noted by their Initial / primary / secondary / tertiary functions. See "Pin Descriptions" Table for details.
- NC balls can be connected to VDD_IO or GND.

Figure 3. 64-Pin WCSP for the ML67Q4060/61

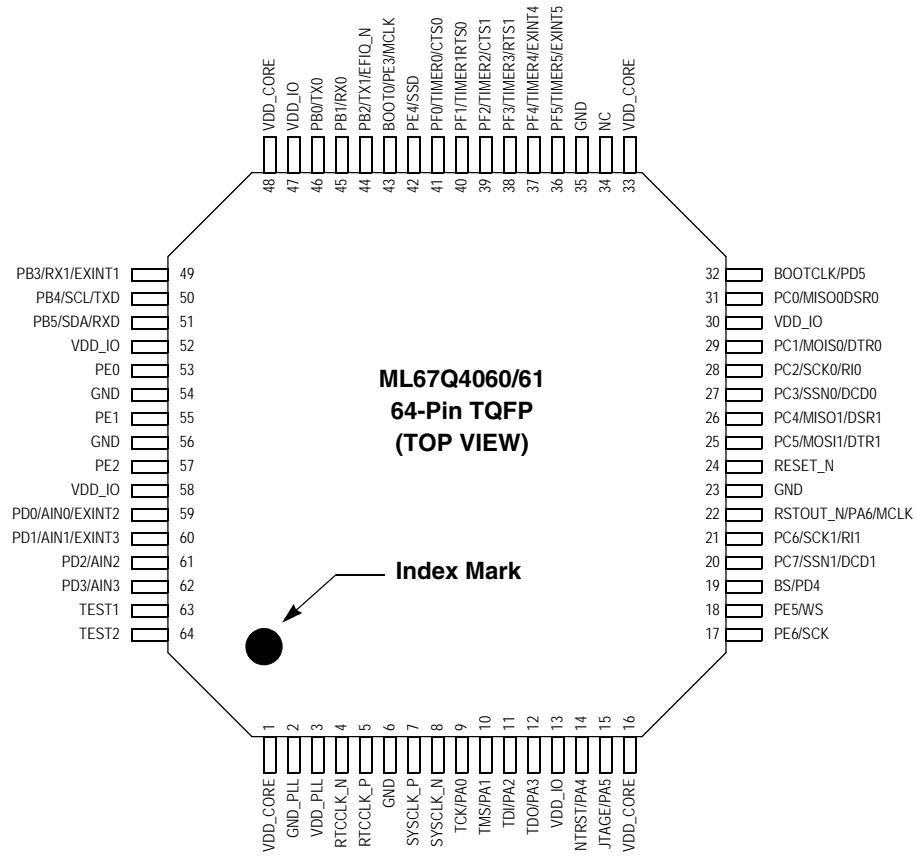
Top View of WCSP Package

	A	B	C	D	E	F	G	H	
8	BOOTCLK/ PD5	NC	PF5/ TIMER5/ EXINT5	PF2/ TIMER2/ CTS1	PE4/ SD	PB0/ TX0	PB4/ SCL/ TXD	PB3/ RX1/ EXINT1	8
7	PC0/ MISO0/ DSR0	GND	PF4/ TIMER4/ EXINT4	PF11/ TIMER1/ RTS0	BOOT0/ PE3/ MCLK	PB5/ SDA/ RXD	PE0	VDD_IO	7
6	PC2/ SCK0/ R10	PC3/ SSN0/ DCD0	PC4/ MISO1/ DSR1	PF3/ TIMER3/ RTS1	PB2/ TX1/ EFIQ_N	PE2	GND	PE1	6
5	PC5/ MOSI1/ DTR1	RESET_N	TDI/ PA2	PC1/ MOSI0/ DTR0	PB1/ /RX0	PD1/ AIN1/ EXINT3	PD0/ AIN0/ EXINT2	VDD_IO	5
4	RSTOUT_N/PA6/ MCLK	PC6/ SCK1/ R11	PC7/ SSN1/ DCD1	TMS/ PA1	PF0/ TIMER0/ CTS0	PD2/ AIN2	PD3/ AN3	TEST1	4
3	BS/ PD4	PE5/ WS	TDO/ PA3	TCK/ PA0	VDD_IO	TEST2	GND	VDD_PLL	3
2	NTRST/ PA4	PE6/ SCK	VDD_CORE	GND	VDD_IO	VDD_CORE	VDD_CORE	GND_PLL	2
1	JTAGE/ PA5	VDD_IO	SYSCLK_N	SYSCLK_P	GND	RTCCLK_P	RTCCLK_N	VDD_CORE	1
	A	B	C	D	E	F	G	H	

NOTES:

1. For pins that have multiple functions, the signals are noted by their Initial / primary / secondary / tertiary functions. See "Pin Descriptions" Table for details.

Figure 4. 64-Pin Plastic TQFP



NOTES:

- For pins that have multiple functions, the signals are noted by their Initial / primary / secondary / tertiary functions. See "Pin Descriptions" Table for details.

Pin Descriptions

The pins of the ML67Q4050/Q4060 Series devices have multiple uses which are shown in detail in [“I/O Functions Share Pin Locations”](#) on page 12. The selection of function used is defined in Chapter 5 the *“ML67Q4050/Q4060 Series User’s Manual”*. The following table

provides the description and function of the pins when they are selected/enabled. The Functions are defined as 1st (primary) / 2nd (secondary) / 3rd (tertiary). The “Initial Function at Reset” overrides other functions and is used until the device is configured.

Pin Descriptions

Symbol	I/O	Description	Function Level		
			1st	2nd	3rd
System					
SYSCLK_P	I	System Clock	✓		
SYSCLK_N	O				
RTCCLK_P	I	32.768 kHz RTC Clock	✓		
RTCCLK_N	O				
RESET_N	I	System Reset input (Active-Low)	✓		
RSTOUT_N	O	Reset output (Active-Low) – shares pin with PA6	✓		
Mode					
TEST1	I	System Test 1	✓		
TEST2	I	System Test 2	✓		
BOOT0	I	Power-up default, selects boot device – shares pin with PE3	Initial Function at Reset		
BOOT1	I	Power-up default, selects boot device – shares pin with PO4			
BOOTCLK	I	Power-up default, Boot Clock – shares pin with PD5			
Debug and Boundary Scan Support					
JTAGE	I	Power-up default, JTAG Test Enable – shares pin with PA5	Initial Function at Reset		
TCK	I	Power-up default, JTAG Clock – shares pin with PA0			
TMS	I	Power-up default, JTAG Mode Select – shares pin with PA1			
NTRST	I	Power-up default, Resets JTAG function (Active Low) – shares pin with PA4			
TDI	I	Power-up default, JTAG Data Input – shares pin with PA2			
TDO	O	Power-up default, JTAG Data Output – shares pin with PA3			
BS	I	Power-up default, boundary scan select – shares pin with PD4			
External Memory Control Signal (ML67Q4050/4051 Only)					
XA [22:0]	O	23-bit Address bus for external devices	✓		
XD [31:0]	I/O	32-bit Data bus for external devices	✓		
EXBUSE	I	Power-up default, memory bus enable – shares pin with PO2	Initial Function at Reset		
EXIROME	I	Power-up default, memory access enable – shares pin with PO3			
OE_N	O	Memory access read enable (Active-Low) – shares pin with PO0	✓		
WR_N	O	Memory access write enable (Active-Low) – shares pin with PO1	✓		
ROMCS_N	O	ROM chip select (Active-Low) – shares pin with PN0	✓		
RAMCS_N	O	RAM chip select (Active-Low) – shares pin with PN1	✓		
BS0/1/2/3_N	O	Four memory byte selects (Active-Low) – shares pin with PN4/5/6/7	✓		
IOCS0_N	O	I/O bank 1, chip select 0 (Active-Low) – shares pin with PN2	✓		
IOCS1_N	O	I/O bank 1, chip select 1 (Active-Low) – shares pin with PN3	✓		
External DMA Control (ML67Q4050/51 Only)					
DMAREQ	I	DMA request – used to request a DMA transfer – shares pin with PI5			✓
DMACLR	O	DMA Clear – signals completion of DMA transfers – shares pin with PI6			✓

Pin Descriptions (Cont.)

Symbol	I/O	Description	Function Level		
			1st	2nd	3rd
General-Purpose I/O Ports					
PA[5:0]	I/O	This is a general-purpose port. – This port shares pins with the startup JTAG function, so it is disabled at power up.	✓		
PA6	I/O			✓	
PB[5:0]	I/O	This is a general-purpose port. – This port shares pins with a secondary function, which can be selected under software control.	✓		
PC[7:0]	I/O	This is a general-purpose port. – This port shares pins with a secondary function, which can be selected under software control.	✓		
PD [5:0]	I/O	This is a general-purpose port. – This port shares pins with a secondary function, which can be selected under software control.	✓		
PE[2:0]	I/O	These pins are dedicated 20 mA I/O pins – no secondary functions	✓		
PE[6:3]	I/O	These pins are either combined with PE[2:0] to form a 7-bit port, or they are programmed to be the I ² S port.	✓		
PF[5:0]	I/O	This is a general-purpose port. – This port shares pins with secondary functions, which can be selected under software control.	✓		
Extended General-Purpose I/O Ports (ML67Q4050/51 Only)					
PG[6:0]	I/O	These are general-purpose ports. – These ports share pins with XA [22:0] and are not available when using external memory		✓	
PH[7:0]	I/O			✓	
PI[7:0]	I/O			✓	
PJ[7:0]	I/O	These are general-purpose ports. – These ports share pins with XD [31:0] are not available when using external memory		✓	
PK[7:0]	I/O			✓	
PL[7:0]	I/O			✓	
PM[7:0]	I/O			✓	
PN[7:0]	I/O	This is a general-purpose port. – This port is not available when using external memory.		✓	
PO[1:0]	I/O	These pins are part of general-purpose ports PO[4:0] – These pins are not available when using external memory functions (OE_N, WR_N)		✓	
PO[4:2]	I/O	These pins are part of general-purpose ports PO[4:0] – They shares pins with the startup external memory function, so it is disabled at power up.	✓		
UART (16550)					
TX[1:0]	O	UART Transmit		✓	
RX[1:0]	I	UART Receive		✓	
CTS[1:0]	I	Clear To Send – Indicates that modem or data set is ready to transfer data.			✓
RTS[1:0]	O	Data Set Ready – Indicates that modem or data set is ready to establish a communications link with UART.			✓
DSR[1:0]	I	Data Set Ready – Indicates that modem or data set is ready to establish a communications link with UART.			✓
DTR[1:0]	O	Data Terminal Ready – Indicates that UART is ready to establish a communications link with the modem or data set.			✓
RI[1:0]	I	Ring Indicator – Indicates that the modem or data set has received a telephone ring indicator.			✓
DCD[1:0]	I	Data Carrier Detect – indicates that the modem has detected a carrier signal			✓
SIO					
RXD	I	SIO asynchronous receive data input			✓
TXD	O	SIO asynchronous transmit data output			✓

Pin Descriptions (Cont.)

Symbol	I/O	Description	Function Level		
			1st	2nd	3rd
External Interrupts					
EFIQ_N	I	Fast Interrupt request (Active-Low)			✓
EXINT[5:1]	I	Interrupt requests			✓
SPI					
MISO[1:0]	I/O	Serial data: Master In – Slave Out		✓	
MOSI[1:0]	I/O	Serial data: Master Out – Slave In		✓	
SSN[1:0]	I/O	Slave select		✓	
SCK[1:0]	I/O	Serial clock		✓	
I²S					
SD	I/O	I ² S serial data		✓	
SCK	I/O	I ² S bit clock		✓	
WS	I/O	I ² S word clock		✓	
MCLK	O	Audio Clock Output		[a]	[b]
I²C					
SDA	I/O	I ² C serial data		✓	
SCL	O	I ² C serial clock		✓	
A/D Converter					
AIN [3:0]	I	A/D inputs (four channels)		✓	
Timer					
TIMER[5:0]	I/O	Timer I/O – Six Channels		✓	
Power Supply					
V _{DD_CORE}		Core logic power supply	—	—	—
V _{DD_IO}		I/O power supply	—	—	—
GND		Core and I/O ground	—	—	—
V _{DD_PLL}		PLL power supply	—	—	—
GND _{PLL}		PLL ground	—	—	—

a. The MCLK can be programmed to be available on the PE3 pin.

b. The MCLK can be programmed to be available on the RSTOUT_N pin.

*I/O Functions Share Pin Locations
(See “Pin Descriptions” on page 9.)*

Primary Function		Secondary Function		Tertiary Function		Initial/Startup Function		Sink Current	Package/Pin Numbers			
Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O		144 LQFP	64 TQFP	84-LF BGA	64 WCSP
RESET_N	I								54	24	K5	B5
SYSCLK_P	I								17	7	E1	D1
SYSCLK_N	O								18	8	F2	C1
RTCCLK_P	I								14	5	D1	F1
RTCCLK_N	O								13	4	D3	G1
TEST1	I								137	63	C4	H4
TEST2	I								141	64	A4	F3
PA0	I/O					TCK	I	3 mA	20	9	F3	D3
PA1	I/O					TMS	I	3 mA	21	10	F1	D4
PA2	I/O					TDI	I	3 mA	22	11	G2	C5
PA3	I/O					TDO	O	3 mA	23	12	G3	C3
PA4	I/O					NTRST	I	3 mA	26	14	H2	A2
PA5	I/O					JTAGE	I	3 mA	30	15	H1	A1
RSTOUT_N	O	PA6	I/O	MCLK	O			3 mA	51	22	K4	A4
PB0	I/O	TX0	O					3 mA	96	46	D9	F8
PB1	I/O	RX0	I					3 mA	95	45	E10	E5
PB2	I/O	TX1	O	EFIQ_N	I			3 mA	94	44	E8	E6
PB3	I/O	RX1	I	EXINT1	I			3 mA	112	49	A9	H8
PB4	I/O	SCL	I/O	TXD	O			3 mA	116	50	B8	G8
PB5	I/O	SDA	I/O	RXD	I			3 mA	121	51	C8	F7
PC0	I/O	MISO0	I/O	DSR0	I			3 mA	66	31	J8	A7
PC1	I/O	MOSI0	I/O	DTR0	O			3 mA	60	29	H7	D5
PC2	I/O	SCK0	I/O	RI0	I			3 mA	59	28	J7	A6
PC3	I/O	SSN0	I/O	DCD0	I			3 mA	58	27	K6	B6
PC4	I/O	MISO1	I/O	DSR1	I			3 mA	57	26	H6	C6
PC5	I/O	MOSI1	I/O	DSR1	I			3 mA	56	25	J6	A5
PC6	I/O	SCK1	I/O	RI1	I			3 mA	50	21	H4	B4
PC7	I/O	SSN1	I/O	DCD1	I			3 mA	49	20	J4	C4
PD0	I/O	AIN0	I	EXINT2	I			3 mA	129	59	B5	G5
PD1	I/O	AIN1	I	EXINT3	I			3 mA	130	60	C5	F5
PD2	I/O	AIN2	I					3 mA	131	61	A5	F4
PD3	I/O	AIN3	I					3 mA	132	62	B4	G4
PD4	I/O					BS	I	3 mA	48	19	K3	A3
PD5	I/O					BOOTCLK	I	3 mA	70	32	K8	A8
PE0	I/O							20 mA	123	53	B7	G7
PE1	I/O							20 mA	125	55	A7	H6
PE2	I/O							20 mA	127	57	C6	F6
PE3	I/O	MCLK	O			BOOT0	I	3 mA	93	43	E9	E7

*I/O Functions Share Pin Locations
(See “Pin Descriptions” on page 9.)*

Primary Function		Secondary Function		Tertiary Function		Initial/Startup Function		Sink Current	Package/Pin Numbers			
Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O		144 LQFP	64 TQFP	84-LF BGA	64 WCSP
PE4	I/O	SD	I/O					3 mA	92	42	F10	E8
PE5	I/O	WS	I/O					3 mA	43	18	J3	B3
PE6	I/O	SCK	I/O					3 mA	39	17	K2	B2
PF0	I/O	TIMER0	I/O	CTS0	I			3 mA	91	41	F8	E4
PF1	I/O	TIMER1	I/O	RTS0	O			3 mA	90	40	F9	D7
PF2	I/O	TIMER2	I/O	CTS1	I			3 mA	89	39	G10	D8
PF3	I/O	TIMER3	I/O	RTS1	O			3 mA	88	38	G8	D6
PF4	I/O	TIMER4	I/O	EXINT4	I			3 mA	87	37	G9	C7
PF5	I/O	TIMER5	I/O	EXINT5	I			3 mA	86	36	H10	C8
XA0	O	PI7	I/O					5 mA	24			
XA1	O	PG0	I/O					5 mA	114			
XA2	O	PG1	I/O					5 mA	115			
XA3	O	PG2	I/O					5 mA	117			
XA4	O	PG3	I/O					5 mA	118			
XA5	O	PG4	I/O					5 mA	119			
XA6	O	PG5	I/O					5 mA	120			
XA7	O	PG6	I/O					5 mA	133			
XA8	O	PH0	I/O					5 mA	134			
XA9	O	PH1	I/O					5 mA	135			
XA10	O	PH2	I/O					5 mA	136			
XA11	O	PH3	I/O					5 mA	138			
XA12	O	PH4	I/O					5 mA	139			
XA13	O	PH5	I/O					5 mA	140			
XA14	O	PH6	I/O					5 mA	142			
XA15	O	PH7	I/O					5 mA	144			
XA16	O	PI0	I/O					5 mA	1			
XA17	O	PI1	I/O					5 mA	2			
XA18	O	PI2	I/O					5 mA	4			
XA19	O	PI3	I/O					5 mA	6			
XA20	O	PI4	I/O					5 mA	9			
XA21	O	PI5	I/O	DMAREQ	I			5 mA	12			
XA22	O	PI6	I/O	DMACLR	O			5 mA	19			
XD0	I/O	PJ0	I/O					5 mA	84			
XD1	I/O	PJ1	I/O					5 mA	83			
XD2	I/O	PJ2	I/O					5 mA	79			
XD3	I/O	PJ3	I/O					5 mA	78			
XD4	I/O	PJ4	I/O					5 mA	77			
XD5	I/O	PJ5	I/O					5 mA	76			
XD6	I/O	PJ6	I/O					5 mA	74			

*I/O Functions Share Pin Locations
(See “Pin Descriptions” on page 9.)*

Primary Function		Secondary Function		Tertiary Function		Initial/Startup Function		Sink Current	Package/Pin Numbers			
Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O		144 LQFP	64 TQFP	84-LF BGA	64 WCSP
XD7	I/O	PJ7	I/O					5 mA	73			
XD8	I/O	PK0	I/O					5 mA	72			
XD9	I/O	PK1	I/O					5 mA	69			
XD10	I/O	PK2	I/O					5 mA	68			
XD11	I/O	PK3	I/O					5 mA	67			
XD12	I/O	PK4	I/O					5 mA	65			
XD13	I/O	PK5	I/O					5 mA	64			
XD14	I/O	PK6	I/O					5 mA	62			
XD15	I/O	PK7	I/O					5 mA	61			
XD16	I/O	PL0	I/O					5 mA	55			
XD17	I/O	PL1	I/O					5 mA	47			
XD18	I/O	PL2	I/O					5 mA	45			
XD19	I/O	PL3	I/O					5 mA	44			
XD20	I/O	PL4	I/O					5 mA	42			
XD21	I/O	PL5	I/O					5 mA	41			
XD22	I/O	PL6	I/O					5 mA	40			
XD23	I/O	PL7	I/O					5 mA	37			
XD24	I/O	PM0	I/O					5 mA	36			
XD25	I/O	PM1	I/O					5 mA	35			
XD26	I/O	PM2	I/O					5 mA	33			
XD27	I/O	PM3	I/O					5 mA	32			
XD28	I/O	PM4	I/O					5 mA	31			
XD29	I/O	PM5	I/O					5 mA	29			
XD30	I/O	PM6	I/O					5 mA	28			
XD31	I/O	PM7	I/O					5 mA	27			
ROMCS_N	O	PN0	I/O					5 mA	107			
RAMCS_N	O	PN1	I/O					5 mA	105			
IOCS0_N	O	PN2	I/O					5 mA	104			
IOCS1_N	O	PN3	I/O					5 mA	103			
BS0_N	O	PN4	I/O					5 mA	97			
BS1_N	O	PN5	I/O					5 mA	109			
BS2_N	O	PN6	I/O					5 mA	111			
BS3_N	O	PN7	I/O					5 mA	113			
OE_N	O	PO0	I/O					5 mA	108			
WR_N	O	PO1	I/O					5 mA	98			
PO2	I/O					EXBUS	I	3 mA	82			
PO3	I/O					EXIROME	I	3 mA	100			
PO4	I/O					BOOT1	I	3 mA	102			

Power and Ground Pin Locations

Symbol	144 LQFP	64 TQFP	84-LF BGA	64 WCSP
V _{DD_IO}	5,25,46,63,85,101,122,128	13,30,47,52,58	A6,A8,B1,D10,G1, H3,H8,K7	B1,E2,E3,H5,H7
V _{DD_CORE}	3,34,75,106	1,16,33,48	A1,C9,J2,K10	C2,G2,H1,F2
GND	15,16,38,52,53,71,81,99,110,124, 126,143	6,23,35,54,56	A10,B3,B6,C7,D8,E2, E3,J5,J9,K1,H5,H9	B7,D2,E1,G3,G6
V _{DD_PLL}	10,11	3	C1,D2	H3
GND _{PLL}	7,8	2	C2,C3	H2
NC (No Connect)	80	34	A2,A3,B2,B9,B10,C10, J1,J10,K9	B8

Electrical Characteristics**Absolute Maximum Ratings***(Exceeding these maximum ratings could cause damage or lead to permanent deterioration of the device)*

Parameter	Symbol	Conditions	Rating	Unit
Digital power supply voltage (core)	V_{DD_CORE}	GND = 0V $T_A = 25^\circ\text{C}$	-0.3 to +3.6	V
Digital power supply voltage (I/O)	V_{DD_IO}		-0.3 to +4.6	
PLL power supply voltage	V_{DD_PLL}		-0.3 to +3.6	
Input Voltage	V_I		-0.3 to $V_{DD_IO} + 0.3$	
Output Voltage	V_O		-0.3 to $V_{DD_IO} + 0.3$	mA
Input Current	I_I		-10 to +10	
Output High current	I_{OH}		10	
Output Low current	I_{OL}		20	
Power dissipation	P_D	$T_A = 85^\circ\text{C}$ Per Package	530	mW
Storage temperature	T_{STG}	144-pin LQFP, 64-pin QFP, 64-pin WCSP	-50 to +150	$^\circ\text{C}$
		84-pin LFBGA	-50 to +125	$^\circ\text{C}$

Recommended Operating Conditions (GND = 0 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Digital power supply voltage (core)	V_{DD_CORE}		2.25	2.5	2.75	V
Digital power supply voltage (I/O)	V_{DD_IO}	When external Memory Bus is not used	V_{DD_CORE}	3.3	3.6	
		When external Memory Bus is used	3.0	3.3	3.6	
PLL power supply voltage	V_{DD_PLL}		2.25	2.5	2.75	
Memory retention voltage (SRAM) [a]	VDDH	fOSC = 0 Hz	—	—	2.75	
CPU operating frequency	f_{OSC}	$V_{DD_IO} = V_{DD_CORE}$ to 3.6V $V_{DD_CORE} = 2.25\text{V}$ to 2.75V	0.032	—	33.333	MHz
Ambient Temperature	T_A		-40	25	85	$^\circ\text{C}$

a. Memory retention voltage is the minimum voltage required to retain the contents of internal SRAM.

DC Characteristics ($V_{DD_CORE} = 2.25$ to 2.75 V, $V_{DD_IO} = 3.0$ to 3.6 V, $T_A = -40$ to $+85^\circ\text{C}$)

Parameter		Symbol	Conditions	Min.	Typ.	Max.	Unit
Input High voltage		V_{IH}	—	2.0	—	$V_{DD_IO} + 0.3$	V
Input Low voltage		V_{IL}		-0.3	—	0.8	
Schmitt trigger input threshold voltage		V_{T+}		—	—	$V_{DD_IO} \times 0.7$	
		V_{T-}		$V_{DD_IO} \times 0.2$	—	—	
Schmitt trigger hysteresis		V_{HYS}		$V_{DD_IO} \times 0.1$	—	—	
Output High voltage	3-mA buffer [a]	V_{OH}	$I_{OH} = -3$ mA	—	—	—	V
	5-mA buffer [a]		$I_{OH} = -5$ mA				
	20-mA buffer [b]		$I_{OH} = -20$ mA				
Output Low voltage	3-mA buffer [a]	V_{OL}	$I_{OL} = 3$ mA	—	—	0.40	V
	5-mA buffer [a]		$I_{OL} = 5$ mA	—	—	0.40	
	20-mA buffer [b]		$I_{OL} = 20$ mA	—	—	0.45	
Input leakage current [c]		I_{IH}/I_{IL}	$V_I = 0$ V / V_{DD_IO}	-10	—	10	μA
			$V_I = 0$ V, Pull-up resistance of 50 k Ω	—	—	200	
Output leakage current		I_{LO}	$V_O = 0$ V / V_{DD_IO}	-10	—	10	μA

a. Pins other than 20-mA SINK pins

b. 20-mA SINK pins

c. The absolute value of leakage current into the device is shown as (+) and current out of the device is shown as (-).

DC Characteristics ($V_{DD_CORE} = 2.25$ to 2.75 V, $V_{DD_IO} = V_{DD_CORE}$ to 2.75 V, $T_A = -40$ to $+85^\circ\text{C}$)

Parameter		Symbol	Conditions	Min.	Typ.	Max.	Unit
Input High voltage		V_{IH}	—	1.7	—	$V_{DD_IO} + 0.3$	V
Input Low voltage		V_{IL}		-0.3	—	0.7	
Schmitt trigger input threshold voltage		V_{T+}		—	—	$V_{DD_IO} \times 0.7$	
		V_{T-}		$V_{DD_IO} \times 0.2$	—	—	
Schmitt trigger hysteresis		V_{HYS}		$V_{DD_IO} \times 0.1$	—	—	
Output High voltage	3-mA buffer [a]	V_{OH}	$I_{OH} = -1$ mA	—	—	—	V
	5-mA buffer [a]						
	20-mA buffer [b]						
Output Low voltage	3-mA buffer [a]	V_{OL}	$I_{OL} = 1$ mA	—	—	0.40	V
	5-mA buffer [a]		$I_{OL} = 1$ mA	—	—	0.40	
	20-mA buffer [b]		$I_{OL} = 20$ mA	—	—	0.50	
Input leakage current [c]		I_{IH}/I_{IL}	$V_I = 0$ V / V_{DD_IO}	-10	—	10	μA
			$V_I = 0$ V, Pull-up resistance of 50 k Ω	—	—	150	
Output leakage current		I_{LO}	$V_O = 0$ V / V_{DD_IO}	-10	—	10	μA

a. Pins other than 20-mA SINK pins

b. 20-mA SINK pins

c. The absolute value of leakage current into the device is shown as (+) and current out of the device is shown as (-).

DC Characteristics ($V_{DD_CORE} = 2.25$ to 2.75 V, $V_{DD_IO} = 2.75$ to 3.00 V, $T_A = -40$ to $+85^\circ\text{C}$)

Parameter		Symbol	Conditions	Min.	Typ.	Max.	Unit
Input High voltage		V_{IH}	—	2.0	—	$V_{DD_IO} + 0.3$	V
Input Low voltage		V_{IL}		-0.3	—	0.8	
Schmitt trigger input threshold voltage		V_{T+}		—	—	$V_{DD_IO} \times 0.7$	
		V_{T-}		$V_{DD_IO} \times 0.2$	—	—	
Schmitt trigger hysteresis		V_{HYS}		$V_{DD_IO} \times 0.1$	—	—	
Output High voltage	3-mA buffer [a]	V_{OH}	$I_{OH} = -1$ mA	—	—	—	V
	5-mA buffer [a]						
	20-mA buffer [b]						
Output Low voltage	3-mA buffer [a]	V_{OL}	$I_{OL} = 1$ mA	—	—	0.40	V
	5-mA buffer [a]		$I_{OL} = 1$ mA	—	—	0.40	
	20-mA buffer [b]		$I_{OL} = 20$ mA	—	—	0.45	
Input leakage current [c]		I_{IH}/I_{IL}	$V_I = 0$ V / V_{DD_IO}	-10	—	10	μA
			$V_I = 0$ V, Pull-up resistance of 50 k Ω	—	—	175	
Output leakage current		I_{LO}	$V_O = 0$ V / V_{DD_IO}	-10	—	10	μA

a. Pins other than 20-mA SINK pins

b. 20-mA SINK pins

c. The absolute value of leakage current into the device is shown as (+) and current out of the device is shown as (-).

AC/DC Characteristics ($V_{DD_CORE} = 2.25$ to 2.75 V, $V_{DD_IO} = V_{DD_CORE}$ to 3.6 V, $T_A = -40$ to $+85^\circ\text{C}$)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Pin Capacitance [a]	C_1	—	—	5	—	pF
Pin Capacitance [b]	C_2	—	—	9	—	
Pin Capacitance [c]	C_3	—	—	18	—	
Current consumption (STOP)	I_{DDS_CORE}	$T_A = 85^\circ\text{C}$, $V_{DD_CORE} = 2.75$ V	—	—	485	μA
		$T_A = 25^\circ\text{C}$, $V_{DD_CORE} = 2.5$ V	—	10.131	—	
	I_{DDS_IO} [d]	$T_A = 85^\circ\text{C}$, $V_{DD_IO} = 3.6$ V	—	—	10	
		$T_A = 25^\circ\text{C}$, $V_{DD_IO} = 3.3$ V	—	0.062	—	
	I_{DDS_PLL}	$T_A = 85^\circ\text{C}$, $V_{DD_PLL} = 2.75$ V	—	—	5	
$T_A = 25^\circ\text{C}$, $V_{DD_PLL} = 2.5$ V		—	0.027	—		
Current consumption (HALT)	I_{DDH_CORE}	ML67Q4050/51 $f_{OSC} = 33.333$ MHz No load	—	25	30	mA
	I_{DDH_IO}		—	13.78	16	
	I_{DDH_PLL}		—	6.56	14	
	I_{DDH_CORE}	ML67Q4060/61 $f_{OSC} = 33.333$ MHz No load	—	25	30	
	I_{DDH_IO}		—	8.49	16	
	I_{DDH_PLL}		—	6.56	14	

AC/DC Characteristics ($V_{DD_CORE} = 2.25$ to 2.75 V, $V_{DD_IO} = V_{DD_CORE}$ to 3.6 V, $T_A = -40$ to $+85^\circ\text{C}$) (Cont.)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Current consumption (Dynamic)	I_{DDO_CORE}	ML67Q4050/51 $f_{OSC} = 33.333$ MHz No load	—	49.9	76	mA
	I_{DDO_IO}		—	13.78	30	
	I_{DDO_PLL}		—	6.56	14	
	I_{DDO_CORE}	ML67Q4060/61 $f_{OSC} = 33.333$ MHz No load	—	49.9	76	
	I_{DDO_IO}		—	13.78	30	
	I_{DDO_PLL}		—	6.56	14	

- a. Pin other than the AIN pin and 20mA SINK pins
 b. AIN pins
 c. 20-mA SINK pins
 d. Input ports = V_{DD_IO} or 0 V; other ports = no load

Note: Reference Power Consumption Characteristics:

The following power data is measured on Oki MCU boards during operation. These values should be used as reference only. The measured values on user systems may be different, if operating conditions are changed.

IDD0 Operating Power at 33.333 MHz

TYP: ($V_{DD_IO} = 3.3$ V, $V_{DD_CORE} = 2.5$ V, $V_{DD_PLL} = 2.5$ V, $T_A = 25^\circ\text{C}$)

MAX: ($V_{DD_IO} = 3.6$ V, $V_{DD_CORE} = 2.75$ V, $V_{DD_PLL} = 2.75$ V, $T_A = -40^\circ\text{C}$)

IDD0 Operating Power Limits	ML67Q4050/51		ML67Q4060/61	
	Typ. (mA)	Max. (mA)	Typ. (mA)	Max. (mA)
I_{DD_CORE}	49.90	76.00	49.90	76.00
I_{DD_IO}	13.78	30.00	8.49	30.00
I_{DD_PLL}	6.56	13.00	6.56	13.00

ML67Q4050/51

Typical Operating Power as a Function of Frequency ($V_{DD_IO} = 3.3$ V, $V_{DD_CORE} = V_{DD_PLL} = 2.5$ V, $T_A = 25^\circ\text{C}$)

f_{OSC} (MHz)	8	12	16	20	24	28	33.333
I_{DD_CORE} (mA)	21.80	26.19	30.59	34.98	39.38	43.78	49.90
I_{DD_IO} (mA)	4.69	6.23	7.76	9.30	10.83	12.37	13.78
I_{DD_PLL} (mA)	3.29	3.64	4.00	4.50	5.15	5.80	6.56

ML67Q4060/61

Typical Operating Power as a Function of Frequency ($V_{DD_IO} = 3.3$ V, $V_{DD_CORE} = V_{DD_PLL} = 2.5$ V, $T_A = 25^\circ\text{C}$)

f_{OSC} (MHz)	8	12	16	20	24	28	33.333
I_{DD_CORE} (mA)	21.80	26.19	30.59	34.98	39.38	43.78	49.90
I_{DD_IO} (mA)	2.89	3.84	4.78	5.73	6.67	7.62	8.49
I_{DD_PLL} (mA)	3.29	3.64	4.00	4.50	5.15	5.80	6.56

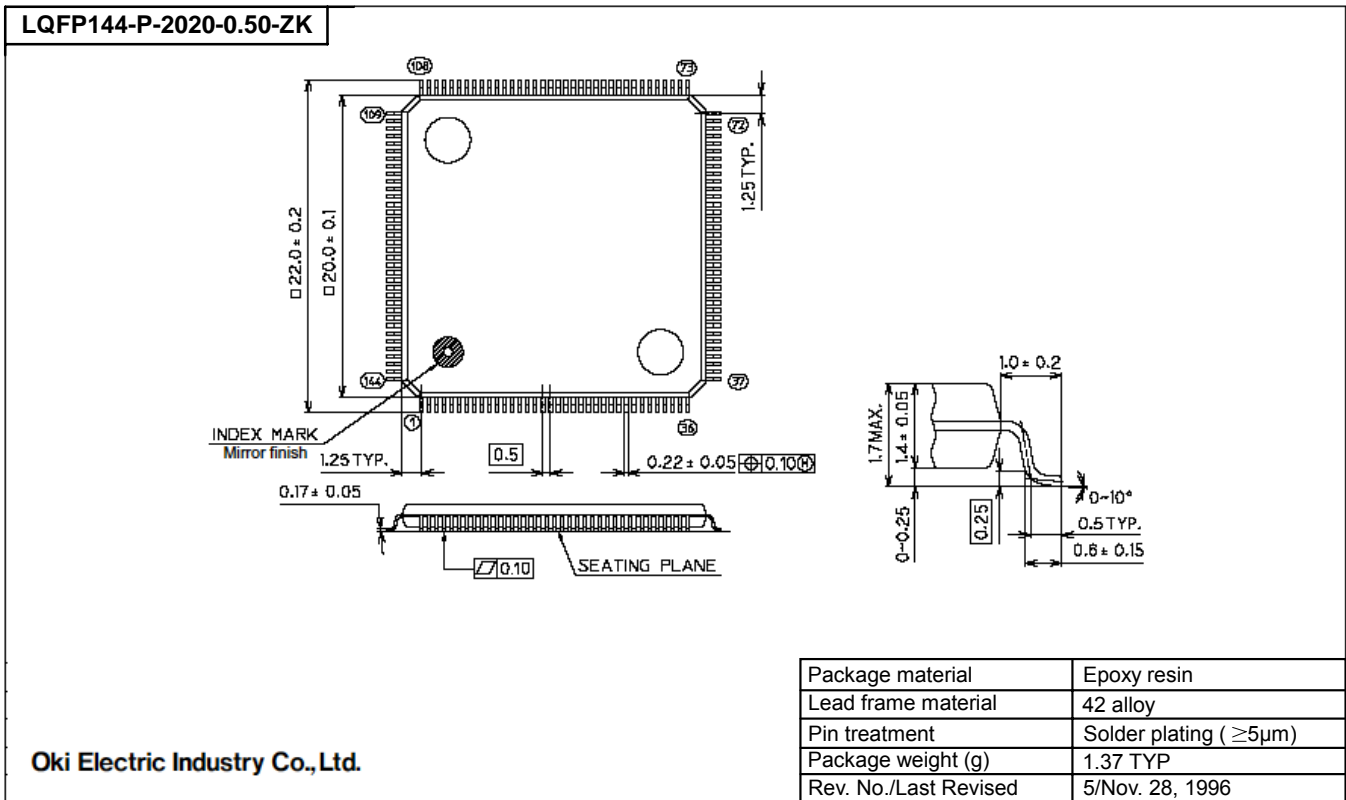
ADC Converter Characteristics

($V_{DD_CORE} = 2.25$ to 2.75 V, $V_{DD_IO} = V_{DD_CORE}$ to 3.6 V, $T_A = -40$ to $+85^\circ\text{C}$)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Resolution	n	—		—	—	10	bit
Linearity error	INL	Sampling Frequency = 50 kHz	Analog input source impedance $R_i \leq 5 \text{ k}\Omega$ $2.25\text{V} \leq V_{DD_IO} \leq 2.75\text{V}$	—	± 4.0	± 6.0	LSB
Zero-scale error	E_{ZS}			—	± 4.0	± 8.0	
Full-scale error	E_{FS}			—	± 4.0	± 8.0	
Linearity error	INL	Sampling Frequency = 100 kHz	Analog input source impedance $R_i \leq 5 \text{ k}\Omega$ $2.75\text{V} \leq V_{DD_IO} \leq 3.6\text{V}$	—	± 3.0	± 6.0	
Zero-scale error	E_{ZS}			—	± 4.0	± 8.0	
Full-scale error	E_{FS}			—	± 4.0	± 8.0	

PACKAGE DIMENSIONS

144-Pin LQFP (LQFP144-P-2020-0.50-ZK)

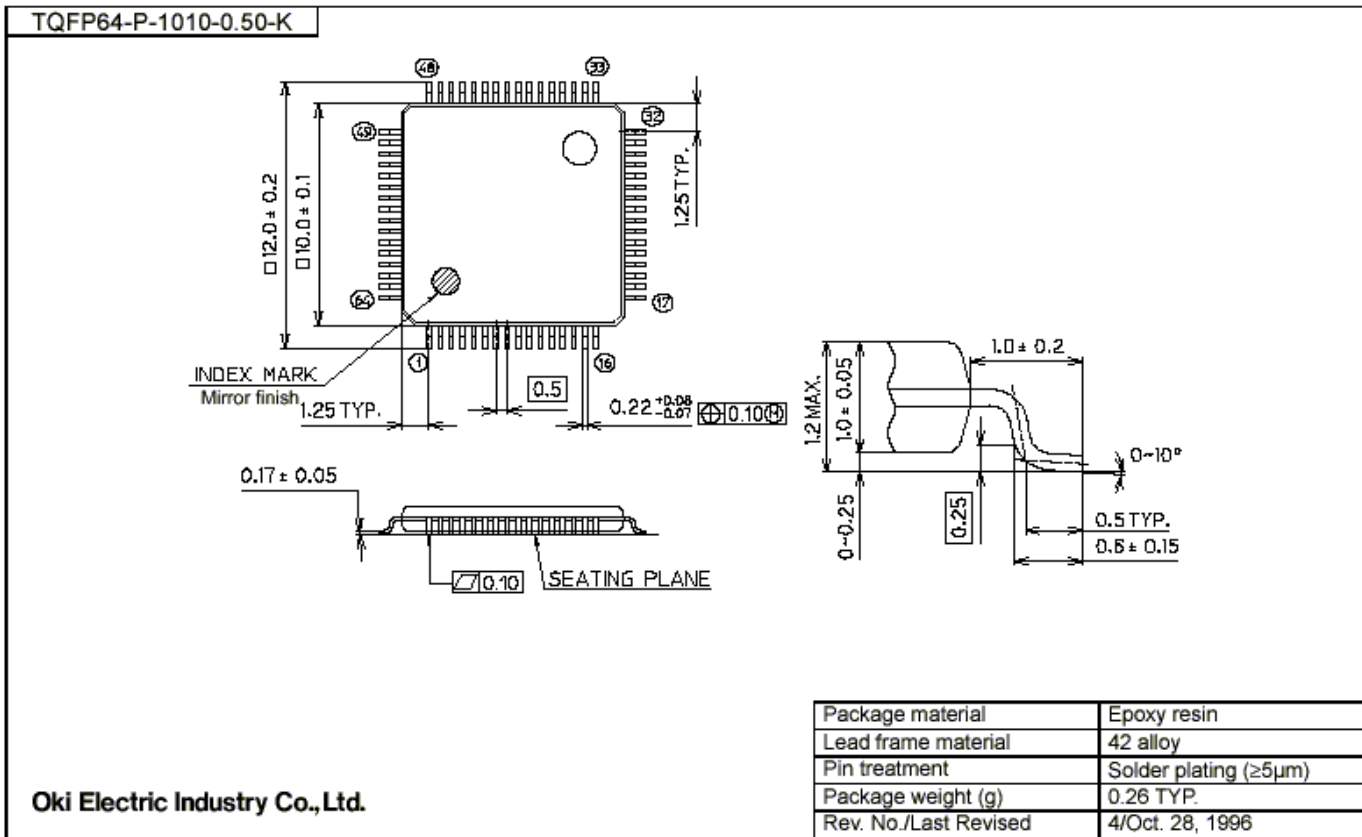


Notes for Mounting the Surface Mount Type Package:

The surface mount type packages are very susceptible to heat in re-flow mounting and humidity absorbed in storage. Therefore, before you perform re-flow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (re-flow method, temperature and times).

64-Pin QFP (TQFP64-P-1010-0.50-K)

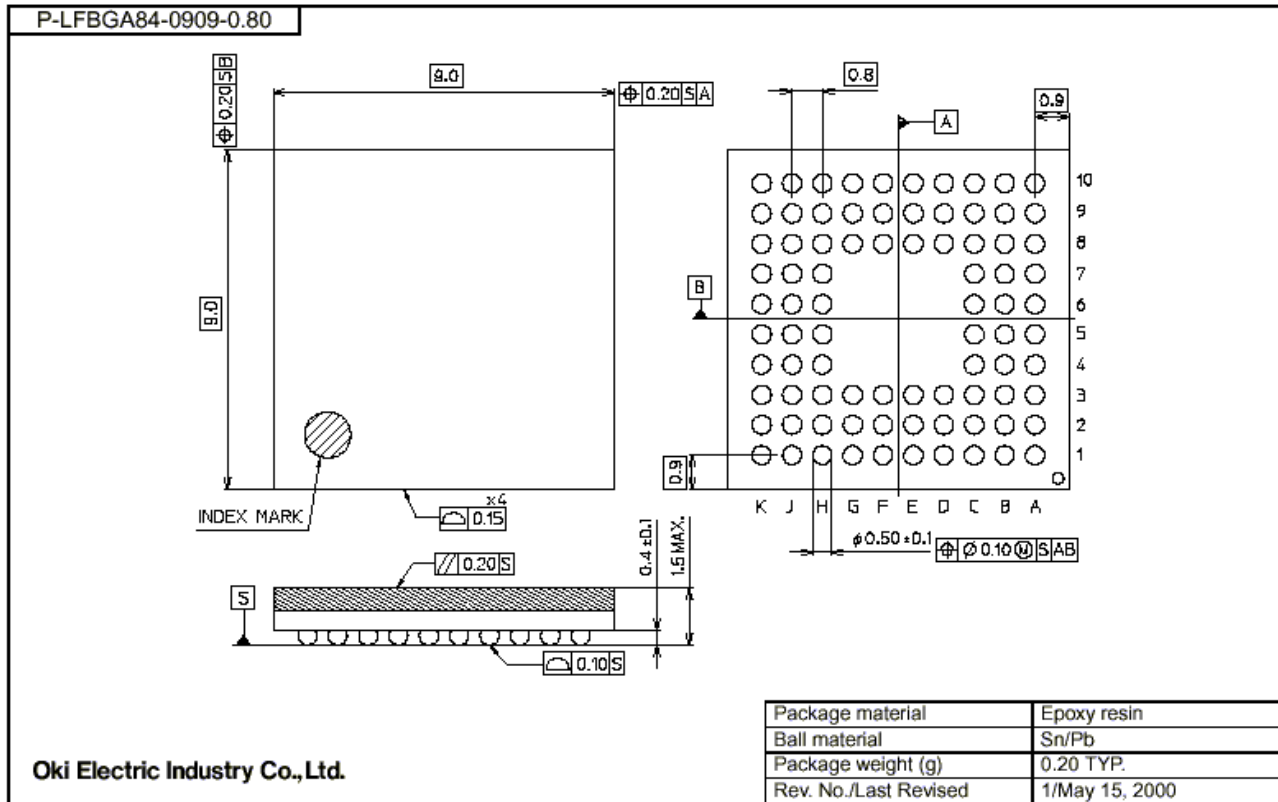
(Unit: mm)



Notes for Mounting the Surface Mount Type Package:

The surface mount type packages are very susceptible to heat in re-flow mounting and humidity absorbed in storage. Therefore, before you perform re-flow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (re-flow method, temperature and times).

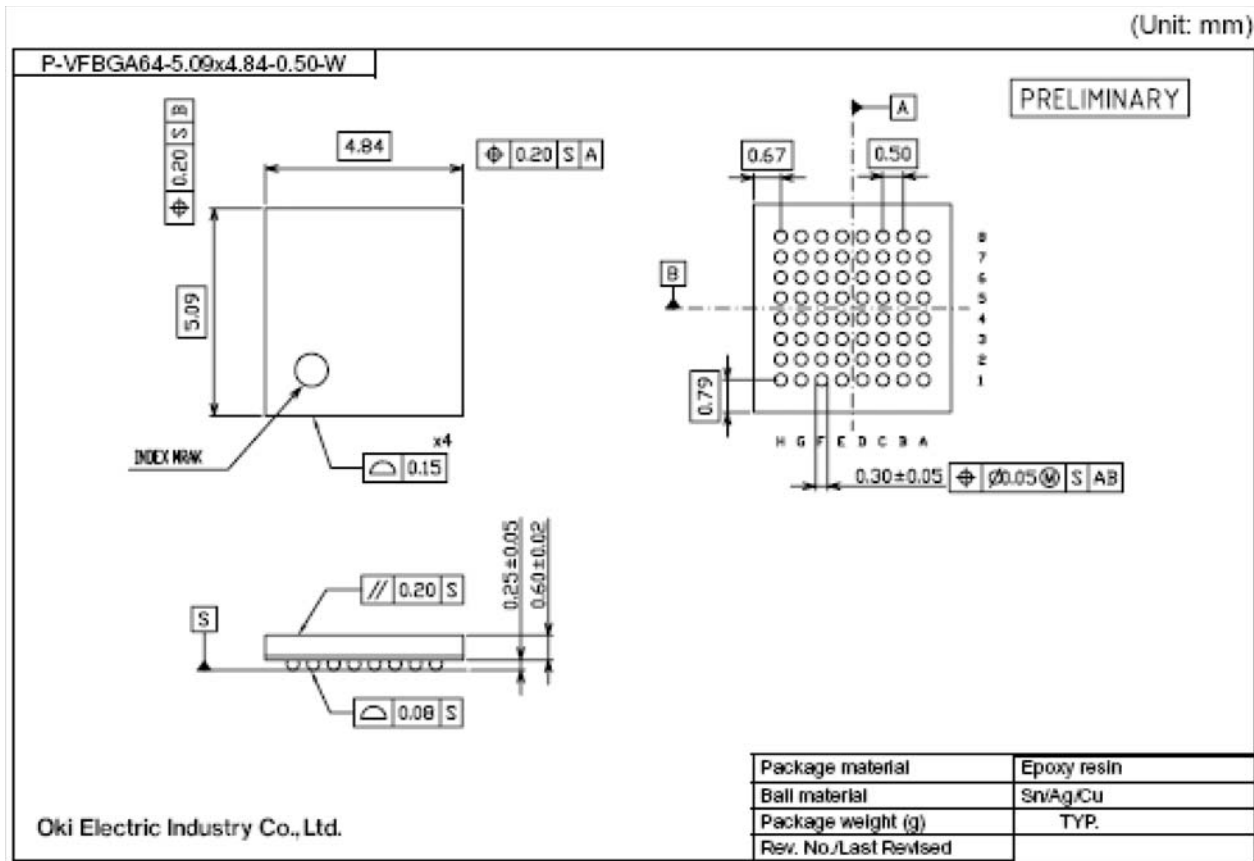
84-Pin LFBGA (P-LFBGA-0909-0.80)



Notes for Mounting the Surface Mount Type Package:

The surface mount type packages are very susceptible to heat in re-flow mounting and humidity absorbed in storage. Therefore, before you perform re-flow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (re-flow method, temperature and times).

64-Pin WCSP (P-VFBGA64-5.09x4.84-0.50-W)



Notes for Mounting the Surface Mount Type Package:

The surface mount type packages are very susceptible to heat in re-flow mounting and humidity absorbed in storage. Therefore, before you perform re-flow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (re-flow method, temperature and times).

Related Oki Documents for the ML67Q4050/Q4060 Series

Document	Date
ML67Q4050/Q4060 Series User's Manual	March, 2005

Related ARM Documents for the ML67Q4050/Q4060 Series

Document
ARM7TDMI™ Technical Reference Manual

Revision History

Revision Number	Date	Changes from Previous Revision
Revision 1.0	March, 2005	Initial release of this document
Revision 1.1	May, 2005	Modified Logic Diagram, rotated package diagrams for LFBGA and WCSP, and edited pin names. Clarified external memories supported.
Revision 1.2	June, 2006	Electrical Characteristics: Revised some DC values and added power limits.

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Please make sure before using the product that the information you are referring to is up-to-date.

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