MN4700, MN4700K, and MN4700F

1,048,576-bit Video Memory

■ General Description

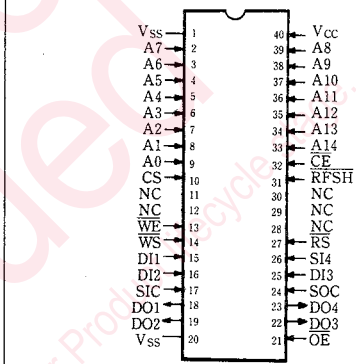
MN4700 is a 1M bits (256K words × 4 bits) N-channel MOS dynamic RAM, and is equipped with 8-bit serial shift registers to enable shift operation of data input and output at the minimum clock rate of 30ns. The large capacity and low power dissipation have been realized by adoption of a single transistor type dynamic memory cell and dynamic peripheral circuits. The serial shift registers respectively covering the data input and output independently of the memory assure easy constitution of a video memory, high speed data transfer, data read, and data write.

■ Features

- Equipped with 8-bit serial/parallel conversion circuit
- Memory constitution: 262,144 words (32,768 addresses × 8 bits serial) × 4 bits
- Serial access time: max. 20ns
- Serial cycle time: min. 30ns
- Address cycle time: min. 240ns (at read modify write time)
- Power consumption: max. 825mW (150mA) at operating time max. 110mW (20mA) at stand-by time
- Source voltage: +5V±10%
- Refresh cycle: 512 cycles/2ms
- Package: 40-pin DIL (item No. MN4700), 40-pin SDIL (item No. MN4700K), and 64-pin QFP (item No. MN4700F)
- Input/output: TTL compatible
- Internally equipped with refresh circuit

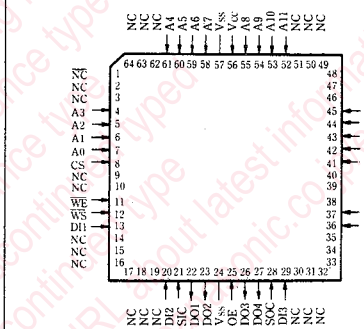
■ Pin Configurations

MN4700, MN4700K



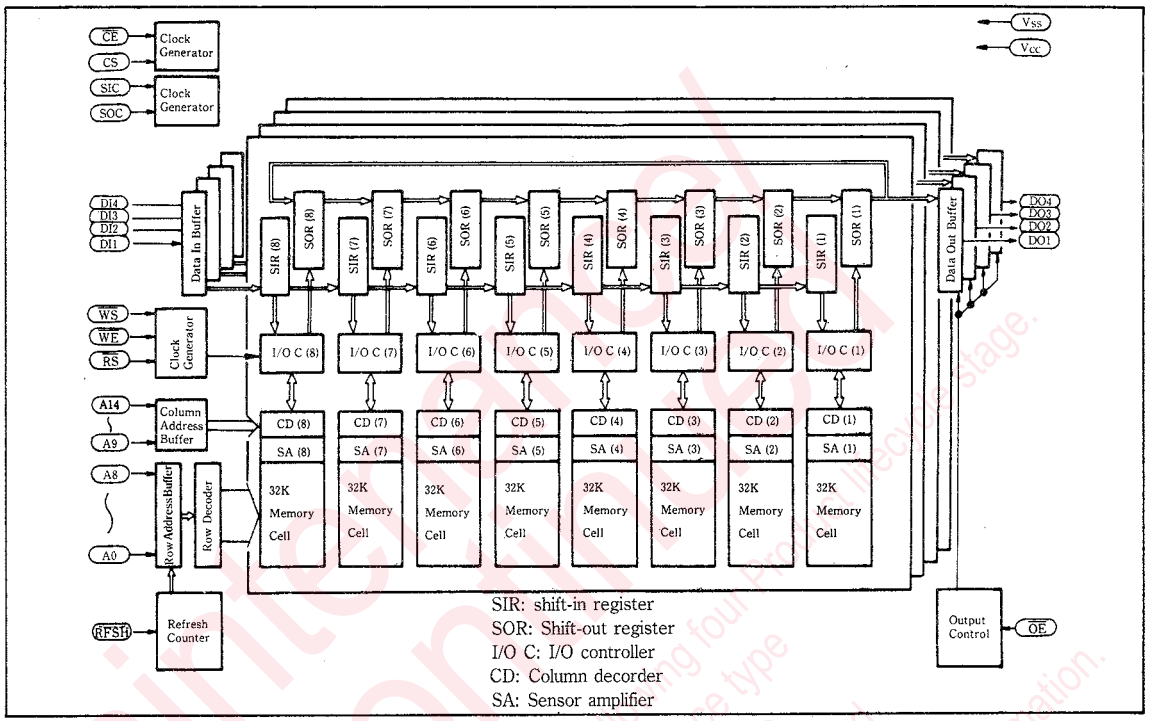
㉒ 40-DIP(b) ㉔ 40-SDIP

MN4700F



㉝ 64-QFP(a)

■ Block Diagram



■ Absolute Maximum Ratings (V_{SS} standard, Ta=25°C)

Item	Symbol	Rating	Unit
Source voltage	V_{CC} (max.)	−1.0~+7.0	V
Input voltage	V_{IN} (max.)	−1.0~+7.0	V
Output voltage	V_{OUT} (max.)	−1.0~+7.0	V
Power dissipation	P_d	1.5	W
Output short circuit current	I_{os}	50	mA
Operating ambient temperature	T_{opr}	0~+70	°C
Storage temperature	T_{stg}	−55~+125	°C

■ Operating Conditions (Ta=0~+70°C, V_{SS} standard, V_{SS}=0V)

Item	Symbol	Condition	min.	typ.	max.	Unit
Source voltage	V_{CC}		4.5	5.0	5.5	V
Input voltage high level (total input)	V_{IH}		2.4		V_{CC}+1.0	V
Input voltage low level (total input)	V_{IL}		−1.0		0.8	V

■ Pin Capacitance (V_{CC}=5V±10%, Ta=25°C, f=1MHz)

Item	Symbol	Condition	min.	typ.	max.	Unit
Input capacitance $\overline{CE}$, $\overline{RS}$, $\overline{WS}$, $\overline{OE}$, $\overline{RFSH}$, SIC, SOC)	C_{I1}				10	pF
Input capacitance (A0~A14)	C_{I2}				10	pF
Input capacitance (DI1~DI4)	C_{I3}				10	pF
Input capacitance (DO~DO4)	C_O				10	pF

■ DC Electrical Characteristics (V_{CC}=5V±10%, Ta=0~+70°C)

Item	Symbol	Condition	min.	typ.	max.	Unit
Operating current (mean supply current)	I_{CC1}	$\overline{CE}$, SIC, SOC cycling; t_c, t_{SIC}, t_{SOC}=min. Note 1)			150	mA
Stand-by current (mean supply current)	I_{CC2}	$\overline{CE}$=$\overline{OE}$=V_{IH}, SIC=SOC=V_{IL}			20	mA
Refresh current (mean supply current)	I_{CC3}	$\overline{RFSH}$ cycling; SIC=SOC=V_{IL}; t_{CR}=min. Note 1)			120	mA
Input leak current (0V<V_{IN}<5.5V)	I_{LI}	Other than measuring pin: 0V	−10	0.1	10	μA
Output leak current	I_{LO}	0V<V_{OUT}<5.5V	−10	0.1	10	μA
Output voltage low level	V_{OL}	I_{OL}=4.2mA			0.4	V
Output voltage high level	V_{OH}	I_{OH}=−5mA	2.4			V

Note 1) The respective value of I_{CC1} and I_{CC3} varies with the cycle rate and the output load condition. The specified values of them denote those at the maximum cycle time under the no-load state.

■ AC Electrical Characteristics (V_{CC}=5V±10%, Ta=0~+70°C) Note 1), Note 2), Note 5)

Item	Symbol	Note	min.	typ.	max.	Unit
Refresh cycle	t_{REF}				2	ms
$\overline{OE}$ access time	t_{OEA}				25	ns
SOC access time	t_{SOA}				20	ns
Output disable time	t_{OEZ}				25	ns
Read/write cycle frequency	t_C		200			ns
Read modify write cycle frequency	t_{RWC}		240			ns
Rise/fall time	t_T	Note 3)	3		50	ns
$\overline{CE}$ precharge time	t_P		80			ns
$\overline{CE}$ pulse width	t_{CE}		110		1010	ns
$\overline{CE}$ hold time from $\overline{RS}$	t_{CRL}		10			ns
$\overline{CE}$ hold time from $\overline{WE}$	t_{CWL}		40			ns
Address setup time	t_{ASC}		0			ns
Address hold time	t_{AHC}		50			ns
$\overline{CE}$·$\overline{RS}$ delay time	t_{CRD}		85			ns
$\overline{RS}$ pulsle width	t_{RS}		20		1000	ns
$\overline{RS}$ precharge time	t_{RSP}		30			ns
$\overline{RS}$ hold time from SOC	t_{RSL}		0			ns
$\overline{WE}$ pulse width	t_{WP}		20		1000	ns
$\overline{WE}$ read cycle setup time	t_{RCS}		0			ns
$\overline{WE}$ read cycle hold time	t_{RCH}		20			ns
$\overline{WE}$ delay time from $\overline{RS}$	t_{RWD}		0			ns
$\overline{CE}$·$\overline{WE}$ delay time (read modify write cycle)	t_{CWD}		90			ns
$\overline{WE}$ hold time from $\overline{CE}$	t_{WHC}		70			ns
$\overline{WS}$ precharge time	t_{WSP}		30			ns
$\overline{WS}$ pulse width	t_{WS}		20		1000	ns
$\overline{WS}$ inhibition time	t_{WIH}		50			ns
$\overline{WS}$ setup time	t_{SWE}		20			ns
$\overline{OE}$ precharge time	t_{OEP}		30			ns
$\overline{OE}$ pulse width	t_{OE}		30			ns

■ AC Electrical Characteristics (Cont.) (V_{CC}=5V±10%, Ta=0~+70°C)[Note 1), Note 2), Note 5)]

Item	Symbol	Note	min.	typ.	max.	Unit
CS setup time	t_{ASC}	Note 4)	0			ns
CS hold time	t_{AHC}	Note 4)	50			ns
SOC setup time	t_{SOS}		0			ns
SOC valid time	t_{SOV}		15			ns
SOC prcharge time	t_{SOP}		10		1000	ns
SOC pulse width	t_{SO}		10			ns
Serial out cycle frequency	t_{SOC}		30			ns
Output data hold time	t_{SOH}		5			ns
SIC valid time	t_{SIV}		5			ns
SIC hold time	t_{SIH}		10			ns
SIC precharge time	t_{SIP}		10		1000	ns
SIC pulse width	t_{SI}		10			ns
Serial cycle frequency	t_{SIC}		30			ns
Data input setup time	t_{DS}		5			ns
Data input hold time	t_{DH}		5			ns
$\overline{CE}$ precharge start-$\overline{RFSH}$ delay time	t_{CSR}		80			ns
Refresh reset time	t_{FR}		80			ns
$\overline{RFSH}$ prcharge time	t_{FP}		80			ns
$\overline{RFSH}$ pulse width	t_{RDI}		110			ns
$\overline{RFSH}$ refresh cycle	t_{CR}		200			ns

Note 1) Set the wait time of 500μs before the memory operation start after the powr input. Also insert the 8 or more dummy cycles by the $\overline{CE}$, SIC, and SOC. The wait time of 500μ may include the cycles of the $\overline{CE}$, SIC, and SOC. The dummy cycle insertion is also necessary after the state of $\overline{CE}$=V_{IH} and SIC=SOC=V_{IL} continued for 2ms or more.

Note 2) The condition of emasurement is t_T=5.0ns.

Note 3) The timing measurement, rise time, and fall time are based on V_{IH} and V_{IL}

Note 4) The CS is fetched at the same timing as of the address input.

Note 5) The output pin load is measured at 50pF+2TTL.

■ Explanation of Pins

Symbol	Pin name	I/O	Explanatio of terminal
A0~A14	Address inptu pin	I	MN4700 requires 15-bit address input to select one address from among the 32,768 addresses. The row address and the column address are simultaneously fetched at the fall of the $\overline{CE}$ because MN4700 has adopted no address multiplexing system.
$\overline{CE}$	Chip enable input pin	I	MN4700 fetches the addresses (row address and column address together) at the fall of the $\overline{CE}$, and after selecting the concerned word line and activating the sensor amplifier, selects the corresponding 8-word (32-bit) memory cell when the CS level is "H".
$\overline{OE}$	Output enable input pin	I	The output enable input is a clock to control the output impedance. Whe the ouptut enable signal was input, the $\overline{OE}$ level becomes "H", and after the lapse of t_{OES}, the DO1~DO4 become Hi-Z. Then the $\overline{OE}$ level becomes "L", and after the lapse of t_{OEA}, the DO1~DO4 output is enabled. The $\overline{OE}$ exerts no influence on the SOC clock shift-out register control.
$\overline{WE}$	Write enable input pin	I	The write enable input activates the $\overline{CE}$ clock and the $\overline{WE}$ to write the data of the I/O controller inot the selected 8-word (32-bit) memory cell.
$\overline{WS}$	Write strobe input pin	I	When the $\overline{WE}$ was activate by the write strobe input, the data of the shift-in register is transferred to the I/O controller and latched.
$\overline{RS}$	Read strobe input pin	I	When the $\overline{CE}$ clock and the $\overline{RS}$ were activated by the read strobe input, the selected 8-word (32-bit) memory data is transferred to the I/O controller and latched, and thereafter transferred to the shift-out register.
CS	Chip select input pin	I	This is the input pin for chip selection. To the chip intended for read/write, the level must be put into "H". The CS is fetched together with the address at the fall of the $\overline{CE}$.
SIC	Shift-in clock input pin	I	This is the input pin of the shift-in clock. By the rise or this clock, data is sequentially fetched into the shift-in register.
SOC	Shift-out clock input pin	I	This is the input pin of the shift-out clock. By the rise of this clock, 1 word (4 bits) of the serial data is sequentially output. This output data is held until the rise of the next shift-out clock.
DI1~DI4	Data input pin	I	This is the serial data input pin.
DO1~DO4	Data output pin	O	This is the serial data output pin.
$\overline{RFSH}$	Refresh input pin	I	This is the input pin of the refresh signal. When this clock signal was nput, the concerning memory is refreshed.
V_{CC}	Power supply pin (+5V)	—	
V_{SS}	Power supply pin (0V)	—	
NC	Non-connection	—	

■ Explanation of Operation

• Data processing method

The four data inputs (DI1~DI4) and the four data outputs (DO1~DO4) are respectively processed in the 8-bit serial data form.

The input data is fetched at the rise edge of the SIC, and sequentially transferred to the internal 8-bit shift-in register. At the fall edge of the $\overline{WS}$, the 8-bit data in the shift-in register is transferred to the I/O controller block. The input data latched in the I/O controller block is written into the concerning memory cell in the memory write cycle. The data to be written into the memory cell, therefore, corresponds to the input data stored during the SIC 8 cycles before the fall of the $\overline{WS}$.

The 8-bit data read from the memory block in the memory read cycle is latched int eh I/O controller block at the fall edge of the $\overline{RS}$, and the read data is simultaneously transferred to the shift-out register. The data transferred to the shift-out register is synchronized with the SOC and sequentially output at the rise of the SOC immediately after the fall of the $\overline{RS}$. The shift-out register outputs the same 8-bit data repeatedly until the data transfer start by the next $\overline{RS}$ since it is a circulating shift register.

• Memory read/write cycle

If the $\overline{CE}$ fell when the CS level is "H" (chip selection), the memory read cycle or the memory write cycle starts. The read operation and the write operation are selected by the $\overline{WE}$. Namely when the $\overline{WE}$ level is "H", the read cycle is selected, and when "L", the write cycle is selected. The address of the memory cell to be selected is fetched at the fall edge of the $\overline{CE}$.

In the read cycle, the $\overline{RS}$ clock input is disabled until the memory cell data read is completed. (t_{ORD}) The read data transferred to the shift-out register is sequentially output by the rise of the SOC clock when the $\overline{OE}$ level is "L".

The write cycle starts at the later fall of either the $\overline{WE}$ or the $\overline{CE}$. Therefroe, the data transfer to the I/O controller by the $\overline{WS}$ clock must be completed (to be set by t_{SWE}) before the write cycle starts. It is also necessary to secure the time space of t_{WIH} to be left before the next rise of the $\overline{WS}$ clock.

• Read modify write cycle

It is necessary to wait for the fall of the $\overline{RS}$ and the $\overline{WE}$ in the same $\overline{CE}$ cycle for execution of the read modify write to the memory cell of the same address. The address of the memory cell to be selected for that purpose is latched at the fall of the $\overline{CE}$.

• $\overline{CE}$ only refresh cycle

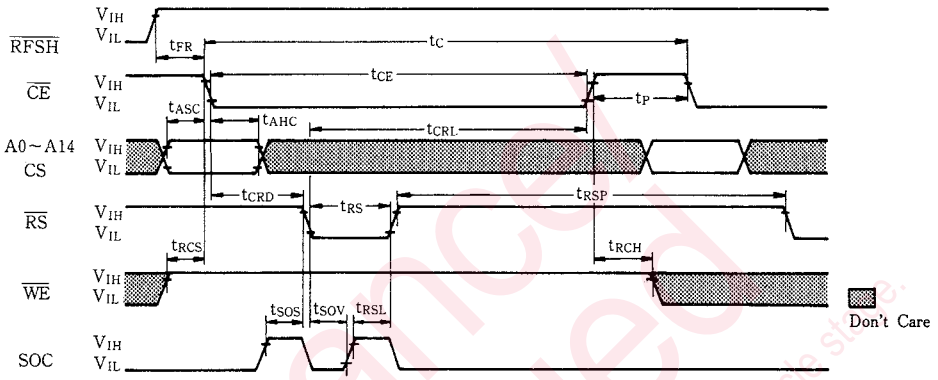
The $\overline{CE}$ only refresh and the $\overline{RFSH}$ refresh are available in MN4700, and the refresh cycle time is 512 cycles/2ms. In the $\overline{CE}$ only refresh cycle, one row address is selected from among the 512 row addresses specified by the lower 9 bits (A0~A8) of the concerning address, and the data of 2048 bits per 1 row is amplified by the sensor amplifier and rewritten into the memory cell. In other words, all the row addresses 1~511 specified by the lower 9 bits are supposed to the selected within 2ms. So, some systems of the display memory and others in which the address is always incremented or decremented for the memory may not require new refresh cycle insertion. It is possible, on the other hand, to execute the $\overline{CE}$ only refresh even if the CS level is "L" (non-selection).

• $\overline{RFSH}$ refresh cycle

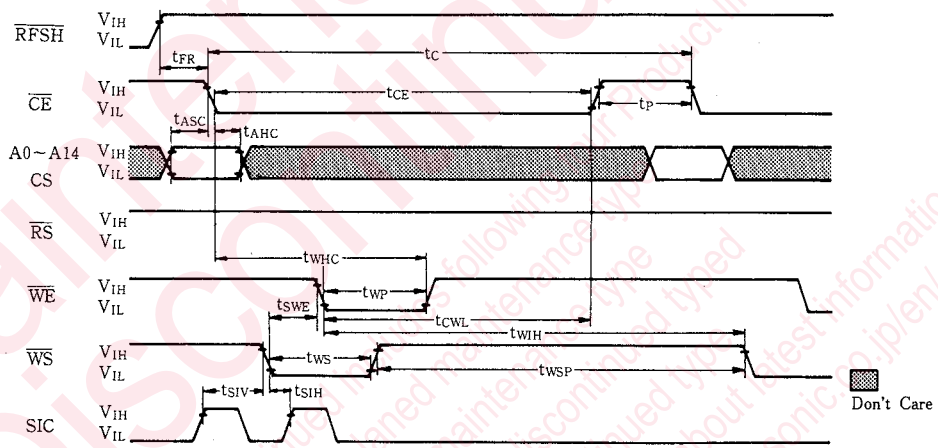
In the $\overline{RFSH}$ refresh cycle, the internal refresh is executed by the $\overline{RFSH}$ clock while the $\overline{CE}$ is kept in the "H" level state. This refresh cycle starts at the fall of the $\overline{RFSH}$ clock. The $\overline{RFSH}$ refresh requires no extra address input since MN4700 is internally equipped with an address counter. The address counter is counted up per $\overline{RFSH}$ pulse input, and all the memory cells are refreshed in 512 cycles so long as the $\overline{RFSH}$ clock is repeatedly input 512 times within 2ms.

■ Timing Charts

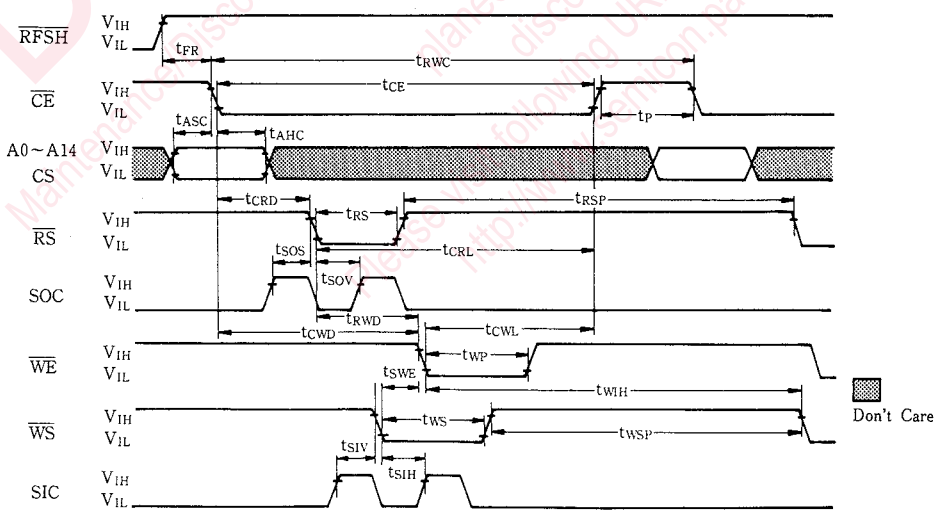
• Memory read cycle



• Memory write cycle

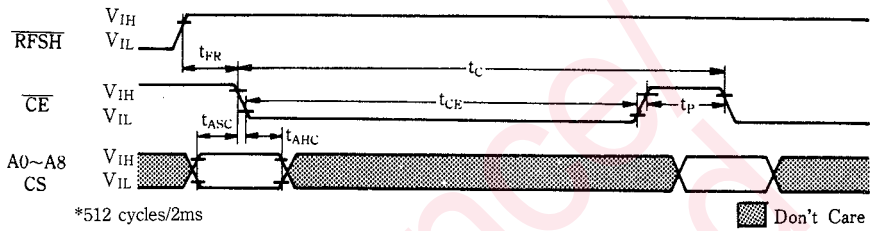


• Memory read modify cycle

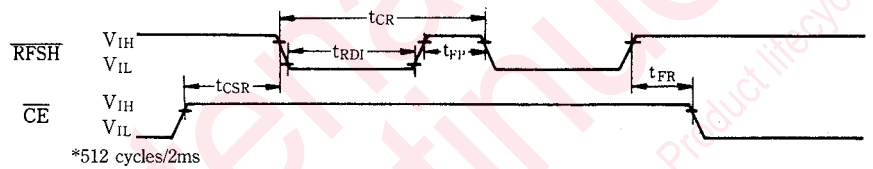


■ Timing Charts (Cont.)

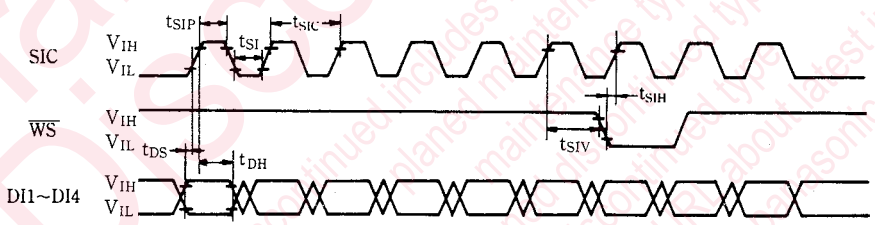
- $\overline{CE}$ only refresh cycle



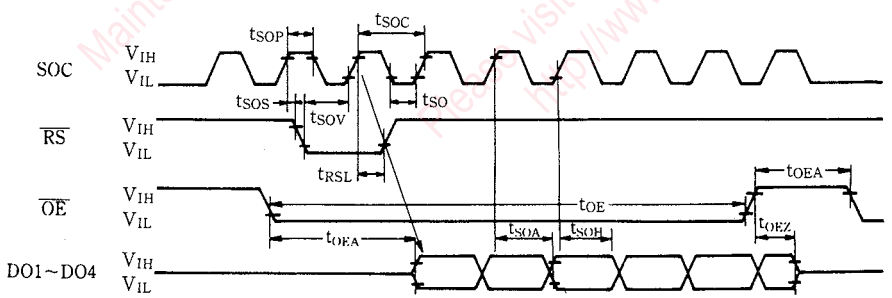
- $\overline{RFSH}$ refresh cycle



- Shift-in cycle



- Shift-out cycle

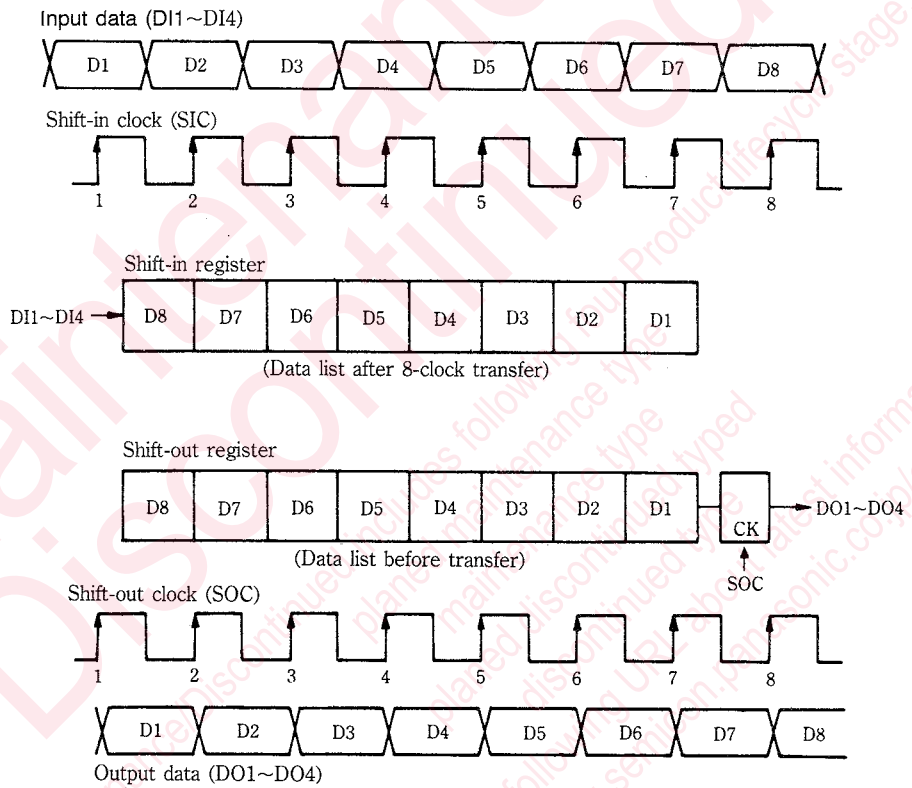


■ Relation of Input Data and Output Data

The input data is fetched through the input pins of DI0~DI4 by the shift-in clock (SIC) sequentially from D1, and after completion of the 8 shift-in clock input, the fetched data is arrayed in the shift-in register as shown in the sketch below. The data is written in the 8-bit parallel format during the memory write cycle.

The output data, on the other hand, is read in the memory read cycle, and transferred to the shift-out register in the 8-bit parallel form by the $\overline{RS}$. At that time, the transferred data is arrayed as shown in the sketch below, and output through the output pins of DO1~DO4 sequentially from D1 by the shift-out clock (SOC) in the same order as of their input.

(Conceptual Diagram)



■ Explanation of Data Input/Output Timing

MN4700 has a shift-in register and a shift-out register independent of each other. So, the data input and the data output by different clocks are possible as is clear from the examples shown in Fig. 1~Fig. 3 on the following pages.

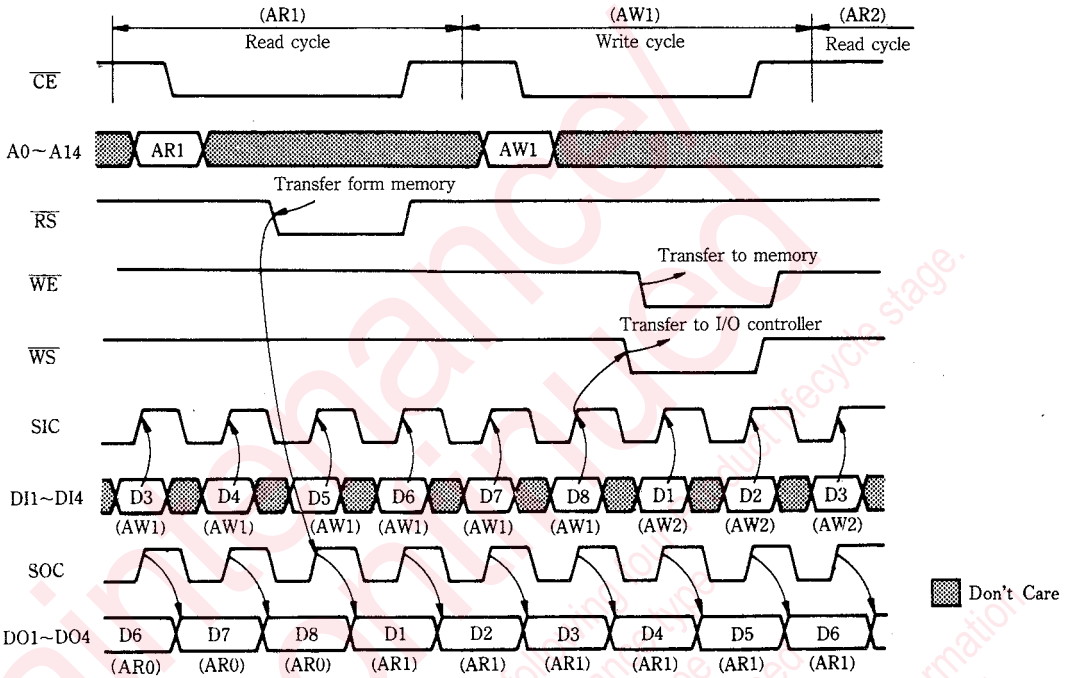
In the example shown in Fig. 1, the random write and the random read are repeated per 1 cycle of the $\overline{CE}$. Eight shift-in cycles and shift-out cycles are executed in two cycles of the $\overline{SE}$.

In the example shown in Fig. 2, the data transfer from the memory to the shift-out register is executed twice and the data transfer from the shift-in register to the memory once in one $\overline{CE}$ cycle. Namaly, 8 shift-in cycles and 16 shift-out cycles are covered by 4 cycles of the $\overline{OE}$.

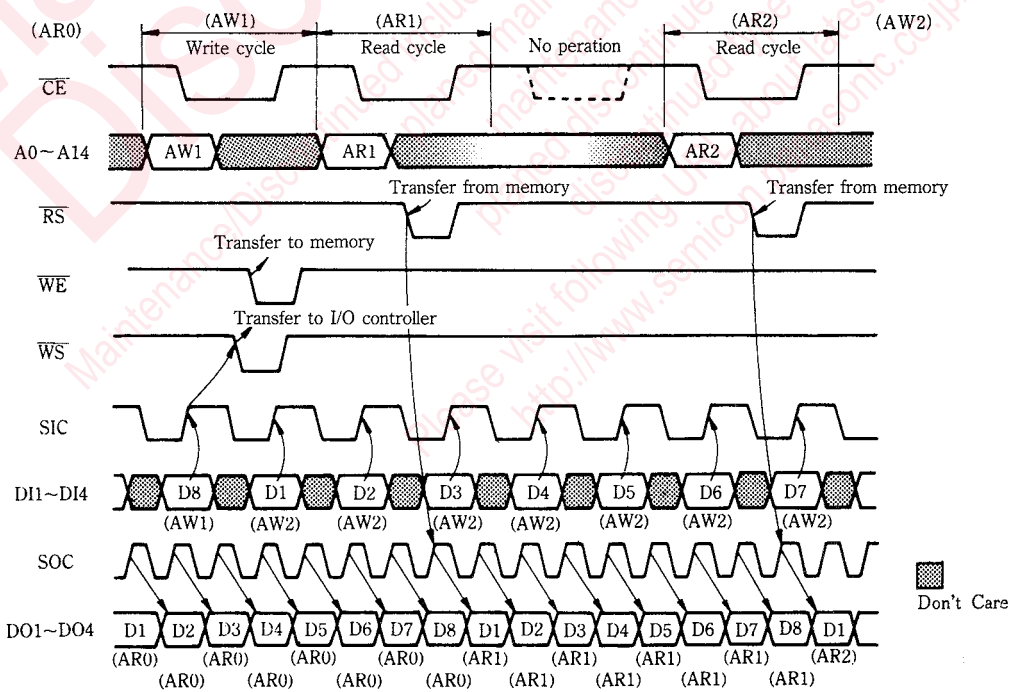
In the example shown in Fig. 3, the read modify write cycle is repeated in one of the two $\overline{CE}$ cycles and the read cycle is repeated in the other one of the $\overline{CE}$ cycles. In other words, two cycles of the $\overline{CE}$ cover 8 shift-in cycles and 16 shift-out cycles.

■ Explanation of Data Input/Output Timing (Cont.)

- Random read/write (Fig. 1)

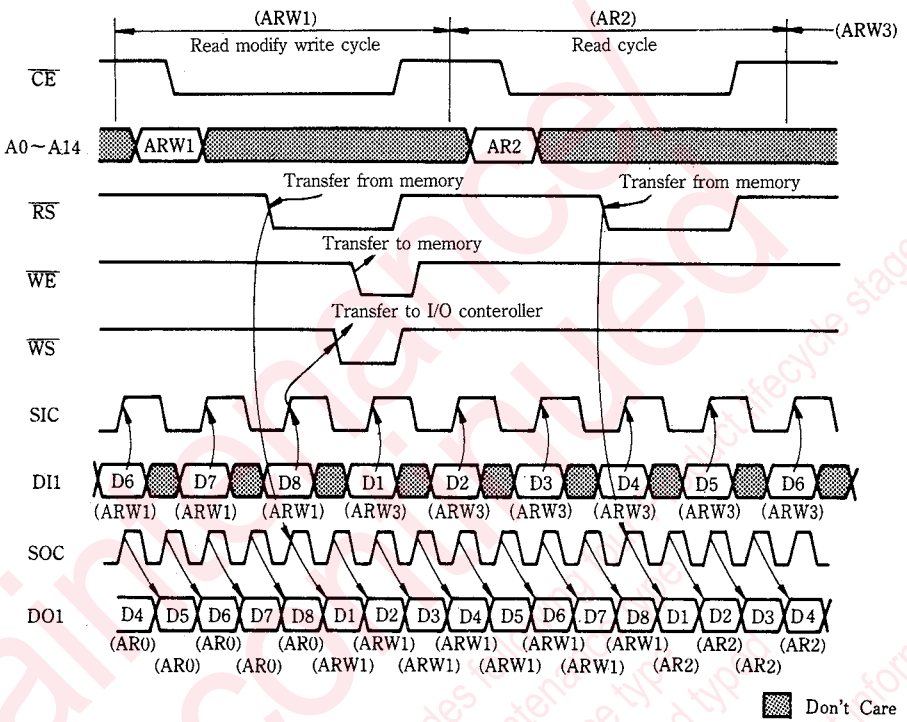


- Random access write and random access double speed read (Fig. 2)



■ Explanation of Data Input/Output Timing (Cont.)

● Read modify write and random access double speed read (Fig. 3)



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