

## CMOS BINARY UP/DOWN COUNTER

### FEATURES

- ◆ Internally Synchronous for High Speed
- ◆ Asynchronous Preset Enable
- ◆ Asynchronous Reset
- ◆ Logic Edge-Clocked Design
- ◆ 6MHz Counting Rate @ 10Vdc
- ◆ Carry Output for Cascading Stages

### DESCRIPTION

The 4516B consists of a four-stage Up/Down Counter with provisions for "look-ahead" carry in both counting modes. The inputs consist of a single Clock, Carry-in (Clock Enable), Reset, Up/Down, Preset Enable, and four individual Jam signals. Four separate buffered Q signals and a Carry-out signal are provided as outputs.

A high Preset Enable signal allows information on the Jam inputs to preset the counter to any state asynchronously with the Clock. A high on the Reset line resets all stages to the "zero" state. The counter is advanced one count at the positive transition of the Clock when the Carry-in and Preset Enable signals are low. Advancement is inhibited when the Carry-in or Preset Enable signals are high. The Carry-out signal is normally high and goes low when the counter reaches its maximum count in the Up mode or the minimum count in the Down mode, provided the Carry-in signal is low. The Carry-in signal in the low state can thus be considered a "Clock Enable." The Carry-in terminal must be connected to  $V_{SS}$  when not in use.

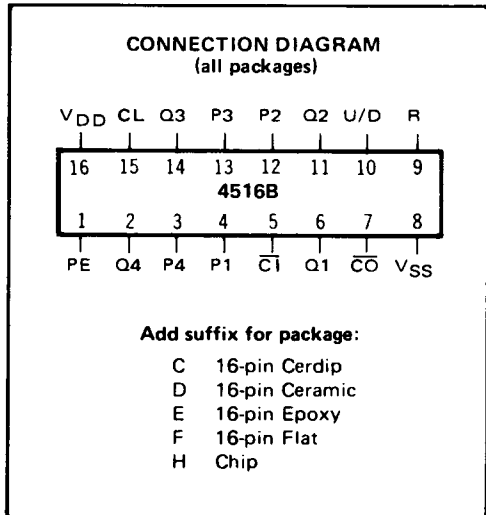
The counter counts Up when the Up/Down input is high, and Down when the Up/Down input is low. Multiple packages can be connected in either a parallel-clocking or a ripple-clocking arrangement. Parallel clocking provides synchronous control and hence faster response from all counting outputs. Ripple-clocking allows for longer clock input rise and fall times.

This counter finds primary use in up/down and differential counting and frequency synthesizer applications. It is also useful in A/D and D/A conversion and for magnitude and sign generation.

**TRUTH TABLE**

CARRY IN	UP/DOWN	PRESET ENABLE	RESET	ACTION
1	X	0	0	No Count
0	1	0	0	Count Up
0	0	0	0	Count Down
X	X	1	0	Preset
X	X	X	1	Reset

X = Don't Care

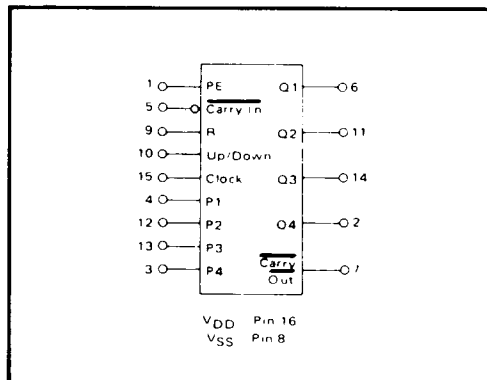


### RECOMMENDED OPERATING CONDITIONS

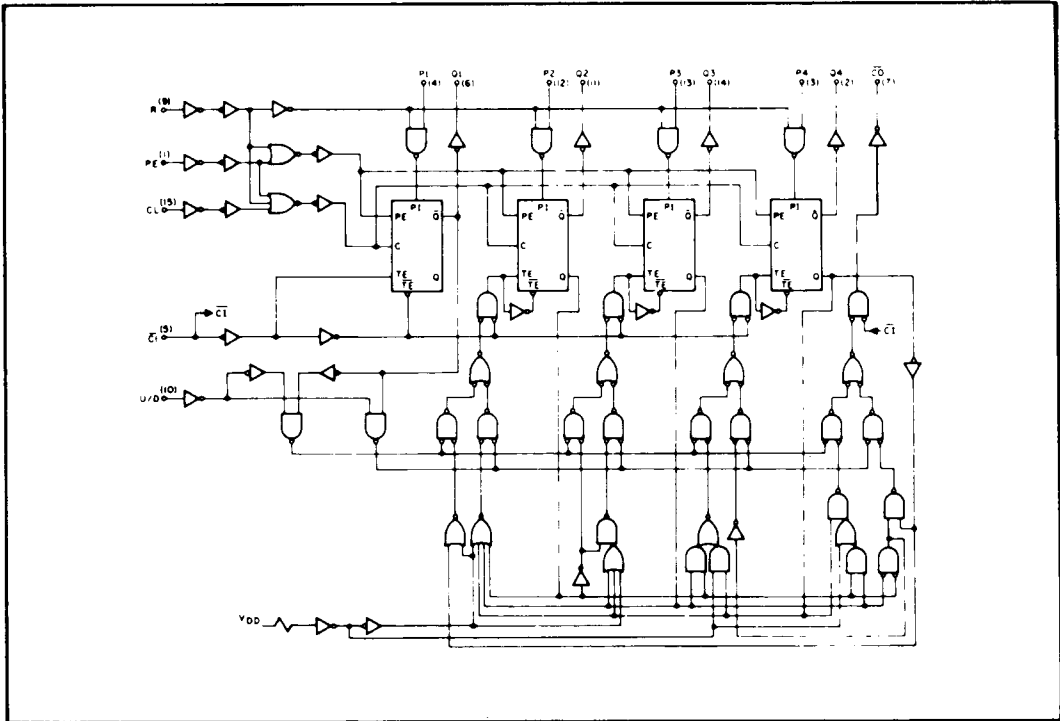
For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	$T_A$		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

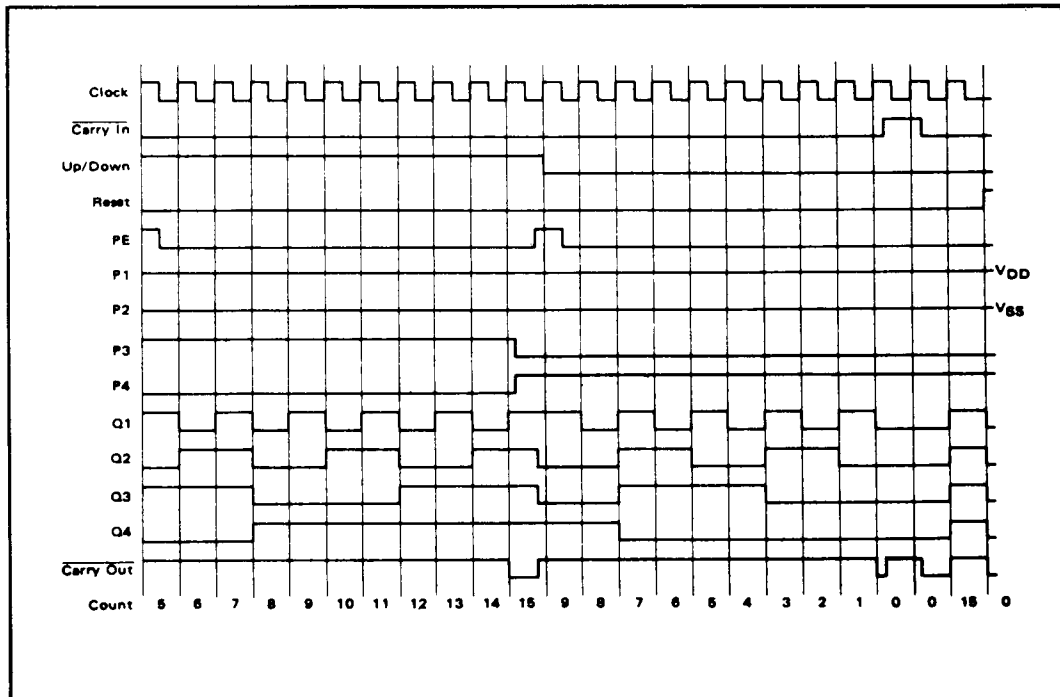
**BLOCK DIAGRAM**



LOGIC DIAGRAM



TIMING DIAGRAM



## ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS<sup>1</sup>

PARAMETER	V <sub>DD</sub> (Vdc)	CONDITIONS	T <sub>LOW</sub> <sup>2</sup>		+25°C			T <sub>HIGH</sub> <sup>2</sup>		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT I <sub>DD</sub>	5	V <sub>IN</sub> = V <sub>SS</sub> or V <sub>DD</sub> All valid input combinations	—	5	—	0.05	5	—	150	μAdc
	10		—	10	—	0.1	10	—	300	
	15		—	20	—	0.2	20	—	600	

NOTES: <sup>1</sup> Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".

<sup>2</sup> T<sub>LOW</sub> = -55°C for C, D, F, H device.

= -40°C for E device.

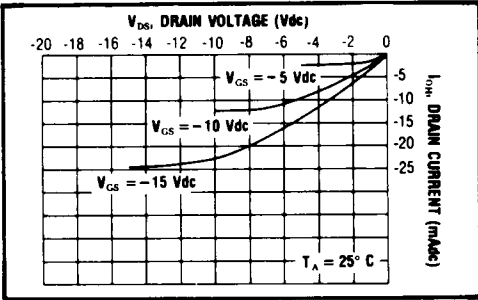
T<sub>HIGH</sub> = +125°C for C, D, F, H device.

= + 85°C for E device.

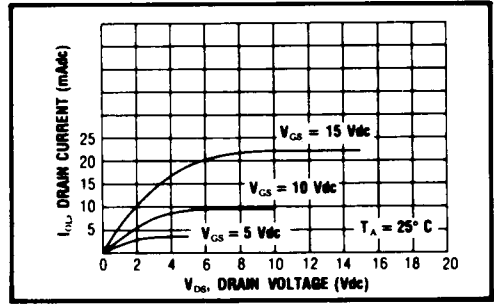
DYNAMIC CHARACTERISTICS (C<sub>L</sub> = 50pF, T<sub>A</sub> = 25°C)

PARAMETER	V <sub>DD</sub> (Vdc)	Min.	Typ.	Max.	Units		
<b>CLOCKED OPERATION</b>							
PROPAGATION DELAY TIME Clock to Q  Clock to $\overline{\text{Carry Out}}$  $\overline{\text{Carry In}}$ to $\overline{\text{Carry Out}}$	t <sub>PLH</sub> , t <sub>PHL</sub>	5	—	200	400	ns	
		10	—	100	200		
		15	—	75	150		
			5	—	210	420	ns
			10	—	120	240	
			15	—	90	180	
			5	—	125	250	ns
			10	—	60	120	
			15	—	50	100	
OUTPUT TRANSITION TIME	t <sub>TLH</sub> , t <sub>THL</sub>	5	—	100	200	ns	
		10	—	50	100		
		15	—	40	80		
MINIMUM CLOCK PULSE WIDTH	PW <sub>CL</sub>	5	—	170	340	ns	
		10	—	85	170		
		15	—	70	140		
MAXIMUM CLOCK FREQUENCY	f <sub>CL</sub>	5	2.0	4.0	—	MHz	
		10	4.0	8.0	—		
		15	5.5	11.0	—		
MAXIMUM CLOCK RISE AND FALL TIME <sup>1</sup>	t <sub>rCL</sub> , t <sub>fCL</sub>	5	15	—	—	μs	
		10	15	—	—		
		15	15	—	—		
MINIMUM SETUP TIME Carry In	t <sub>setup</sub>	5	—	130	260	ns	
		10	—	65	130		
		15	—	50	100		
Up/Down		5	—	250	500	ns	
		10	—	100	200		
		15	—	75	150		
<b>PRESET OR RESET OPERATION</b>							
PROPAGATION DELAY TIME Preset Enable or Reset to Q  Preset Enable or Reset to $\overline{\text{Carry Out}}$	t <sub>PLH</sub> , t <sub>PHL</sub>	5	—	210	420	ns	
		10	—	105	210		
		15	—	90	180		
			5	—	320	640	ns
			10	—	160	320	
			15	—	125	250	
MINIMUM PRESET ENABLE OR RESET PULSE WIDTH	PW <sub>PE</sub> , PW <sub>R</sub>	5	—	100	200	ns	
		10	—	50	100		
		15	—	40	80		
PRESET ENABLE OR RESET REMOVAL TIME	t <sub>rem</sub>	5	—	325	650	ns	
		10	—	110	220		
		15	—	90	180		

<sup>1</sup> When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.

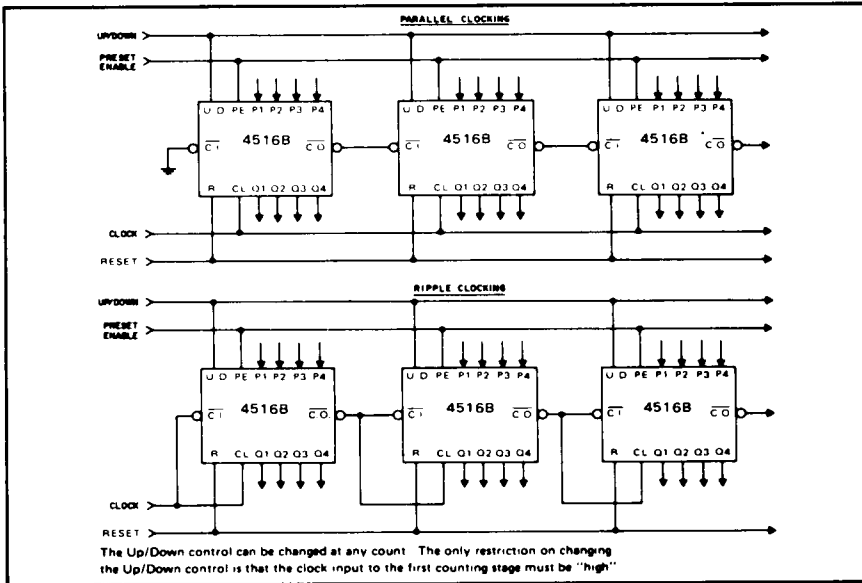


Typical P-Channel Source Current Characteristics



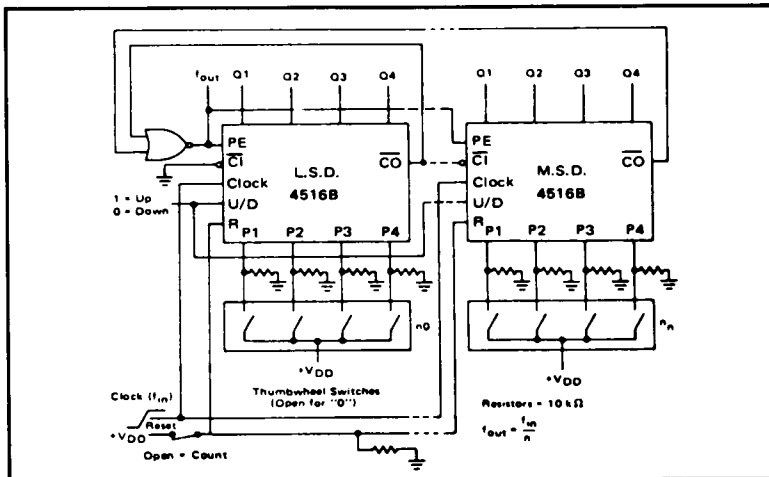
Typical N-Channel Sink Current Characteristics

APPLICATIONS INFORMATION  
CASCADING COUNTERS



The Up/Down control can be changed at any count. The only restriction on changing the Up/Down control is that the clock input to the first counting stage must be "high"

Cascading counter packages.



Programmable Cascaded Frequency Divider