1M ×4 Bit CMOS Dynamic RAM with Static Column Mode

FEATURES

• **Performance range:**

	tRAC	tCAC	tRC
KM44C1002C-5	50ns	13ns	90ns
KM44C1002C-6	60ns	15ns	110ns
KM44C1002C-7	70ns	20ns	130ns
KM44C1002C-8	80ns	20ns	150ns

- **Static Column Mode operation**
- **$\overline{CS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Fast parallel test mode Capability**
- **TTL compatible inputs and outputs**
- **Early Write or Output Enable Controlled Write**
- **Single +5V±10% power supply**
- **1024 cycles/16ms refresh**
- **JEDEC standard pinout**
- **Available in plastic DIP, SOJ, ZIP and TSOP(II) Packages**

GENERAL DESCRIPTION

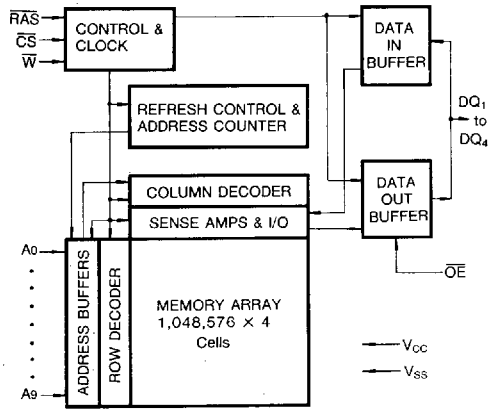
The Samsung KM44C1002C is a CMOS high speed 1, 048,576×4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

Static Column Mode Operation allows high sepeed random or sequential access within a row. The KM44C1002C offers high performance while relaxing many critical system timing requirements for fast usable speed.

$\overline{CS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM44C1002C is fabricated using Samsung's advanced CMOS process.

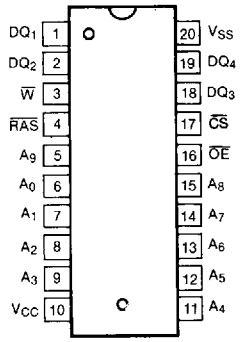
FUNCTIONAL BLOCK DIAGRAM



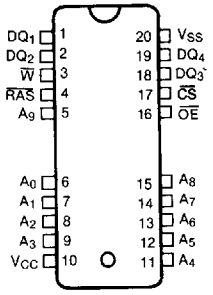
SAMSUNG ELECTRONICS

PIN CONFIGURATION (Top Views)

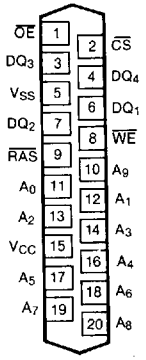
• KM44C1002CP



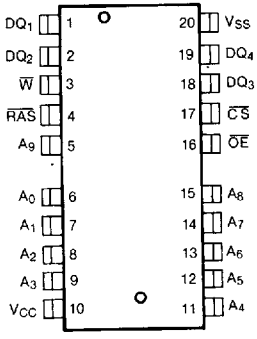
• KM44C1002CJ



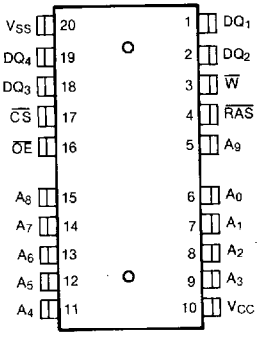
• KM44C1002CZ



• KM44C1002CT



• KM44C1002CTR



Pin Names	Pin Function
A_0-A_9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select Input
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
DQ_1/DQ_4	Data In/Data Out
V_{CC}	Power (+5V)
V_{SS}	Ground

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ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-1 to + 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-1 to + 7.0	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} + 1	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CS}$ Cycling @t_{RC}=min.)	KM44C1002C-5	I_{CC1}	-	85	mA
	KM44C1002C-6		-	75	mA
	KM44C1002C-7		-	65	mA
	KM44C1002C-8		-	55	mA
Standby Current ($\overline{RAS}$=$\overline{CS}$=$\overline{W}$=V_{IH})		I_{CC2}	-	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CS}$=V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC}=min.)	KM44C1002C-5	I_{CC3}	-	85	mA
	KM44C1002C-6		-	75	mA
	KM44C1002C-7		-	65	mA
	KM44C1002C-8		-	55	mA
Standby Column Mode Current* ($\overline{RAS}$=$\overline{CS}$=V_{IL} Address Cycling @t_{PC}=min.)	KM44C1002C-5	I_{CC4}	-	65	mA
	KM44C1002C-6		-	55	mA
	KM44C1002C-7		-	45	mA
	KM44C1002C-8		-	35	mA
Standby Current ($\overline{RAS}$=$\overline{CS}$=$\overline{W}$=V_{CC}-0.2V)		I_{CC5}	-	1	mA
$\overline{CS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CS}$ Cycling @t_{RC}=min.)	KM44C1002C-5	I_{CC6}	-	85	mA
	KM44C1002C-6		-	75	mA
	KM44C1002C-7		-	65	mA
	KM44C1002C-8		-	55	mA
Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}+0.5V, all other pins not under test=0 volts.)		$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤V_{CC})		$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-5mA)		V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. I_{CC1}, I_{CC3}, I_{CC6} Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once during a static column mode cycle.

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_9)	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Input Capacitance (DQ1~DQ4)	C_{OUT}	-	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	133		155		185		205		ns	
Static column mode cycle time	t_{SC}	30		35		40		45		ns	
Static column mode read-write cycle time	t_{SRWC}	80		85		100		110		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60		70		80	ns	3,4,11
Access time from $\overline{CS}$	t_{CAC}		13		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		25		30		35		40	ns	3,11
Access time from last write	t_{ALW}		50		55		65		75	ns	3
$\overline{CS}$ to output in Low-Z	t_{CLZ}	0		0		0		0		ns	7
Output buffer turn-off delay	t_{OFF}	0	13	0	15	0	20	0	20	ns	
Output data hold time from column address	t_{AOH}	5		5		5		5		ns	
Output data enable time from $\overline{W}$	t_{OW}		35		40		45		55	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3		3		ns	
$\overline{RAS}$ precharge time	t_{RP}	30		40		50	50	60	50	ns	2
$\overline{RAS}$ pulse width	t_{RAS}	50	10,000	60	10,000	70		80		ns	
$\overline{RAS}$ pulse width(static column mode)	t_{RASC}	50	100,000	60	100,000	70	10,000	80	10,000	ns	
$\overline{CS}$ to $\overline{RAS}$ hold time	t_{RSH}	13		15		20	100,000	20	100,000	ns	
$\overline{RAS}$ to $\overline{CS}$ hold time	t_{CSH}	50		60		70		80		ns	
$\overline{CS}$ pulse width	t_{CS}	13	10,000	15	10,000	20		20		ns	
$\overline{CS}$ pulse width (static column mode)	t_{CSC}	13	100,000	15	100,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	20	37	20	45	20	100,000	20	100,000	ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	15	50	15	60	ns	4
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5	35	5	40	ns	11
$\overline{CS}$ precharge time (static column mode)	t_{CP}	10		10		10		10		ns	
Row address set-up time	t_{ASR}	0		0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		0		ns	
Column address hold	t_{CAH}	10		10		15		15		ns	
Write address hold time referenced to $\overline{RAS}$	t_{AWR}	40		45		55		60		ns	6
Column address hold time referenced to $\overline{RAS}$	t_{AR}	60		70		80		90		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		35		40		ns	
Column address hold time referenced to $\overline{RAS}$ rise	t_{AH}	5		5		5		5		ns	
Last Write to column address to delay time	t_{LWAD}	20	25	20	25	25	35	25	40	ns	12
Last write to column address hold time	t_{AHLW}	50		60		70		80		ns	
Read command set-up time	t_{RCS}	0		0		0		0		ns	
Read command hold time referenced to $\overline{CS}$	t_{RCH}	0		0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		0		ns	9
Write command hold time	t_{WCH}	10		15		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	40		50		55		60		ns	6
Write command pulse width	t_{WP}	10		15		15		15		ns	
Write command inactive time	t_{WI}	10		10		10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		20		20		ns	
Write command to $\overline{CS}$ lead time	t_{CWL}	13		15		20		20		ns	
Data-in set-up time	t_{DS}	0		0		0		0		ns	10
Data-in hold time	t_{DH}	10		15		15		15		ns	10
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	40		50		55		60		ns	6
Refresh period (1024 cycles)	t_{REF}		16		16		16		16	ms	
Write command set-up time	t_{WCS}	0		0		0		0		ms	8
$\overline{CS}$ to $\overline{W}$ delay time	t_{CWD}	36		40		50		50		ms	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	73		85		100		110		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	48		55		65		70		ns	8
$\overline{CS}$ setup time ($\overline{CS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		10		ns	
$\overline{CS}$ hold time ($\overline{CS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		10		10		ns	
$\overline{RAS}$ to $\overline{CS}$ hold time	t_{RPC}	5		5		5		5		ns	
$\overline{CS}$ precharge time($\overline{CS}$-before-$\overline{RAS}$ counter test cycle)	t_{CPT}	20		20		25		30		ns	
$\overline{OE}$ access time	t_{OEA}		13		15		20		20	ns	
$\overline{OE}$ to data delay	t_{OED}	13		15		20		20		ns	
Output buffer trun off delay time from $\overline{OE}$	t_{OEZ}	0	13	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	t_{OEH}	13		15		15		15		ns	

TEST MODE CYCLE

(Note.13)

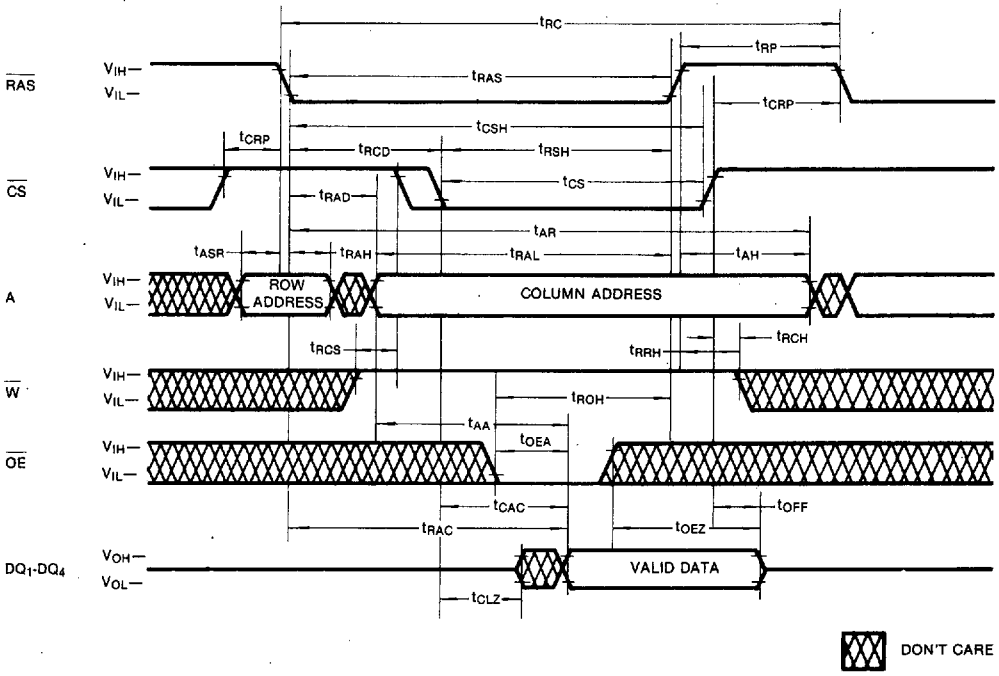
Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	95		115		135		155		ns	
Read-modify-write cycle time	t_{RWC}	138		160		190		210		ns	
Access time from $\overline{RAS}$	t_{RAC}		55		65		75		85	ns	3,4,11
Access time from $\overline{CS}$	t_{CAC}		18		20		25		25	ns	3,4,5
Access time from column address	t_{AA}		30		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	t_{RAS}	55	10,000	65	10,000	75	10,000	85	10,000	ns	
$\overline{CS}$ pulse width	t_{CS}	18	10,000	20	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		20		25		25		ns	
$\overline{CS}$ hold time	t_{CSH}	55		65		75		85		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		45		ns	
$\overline{CS}$ to $\overline{W}$ delay time	t_{CWD}	41		45		55		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	78		90		105		115		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	53		60		70		75		ns	8
Static column mode cycle time	t_{SC}	35		40		45		50		ns	
Static column mode read-modefy-write	t_{SRWC}	85		90		105		115		ns	
$\overline{RAS}$ pulse width (Static column mode)	t_{RASC}	55	100,000	65	100,000	75	100,000	85	100,000	ns	
Access time from last write	t_{ALW}		55		60		70		80	ns	3,12
$\overline{CS}$ pulse width (static column mode)	t_{CSC}	18	100,000	20	100,000	25	100,000	25	100,000	ns	
$\overline{OE}$ access time	t_{OEA}		18		25		25		30		
$\overline{OE}$ to data delay	t_{OED}	18		20		25		25			
$\overline{OE}$ command hold time	t_{OEH}	18		20		25		25			

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{CBR}$ or $\overline{ROR}$ cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AWR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$
7. This parameter defines the time at which the output achieves the open circuit condition and is not refernced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. Operation within the $t_{LWAD(max)}$ limit insures that $t_{ALW(max)}$ can be met. $t_{LWAD(max)}$ is specified as a reference point only. t_{LWAD} is greater than the specified $t_{LWAD(max)}$ limit, then access time is controlled by t_{AA}.
13. These specifications are applied in the test mode.

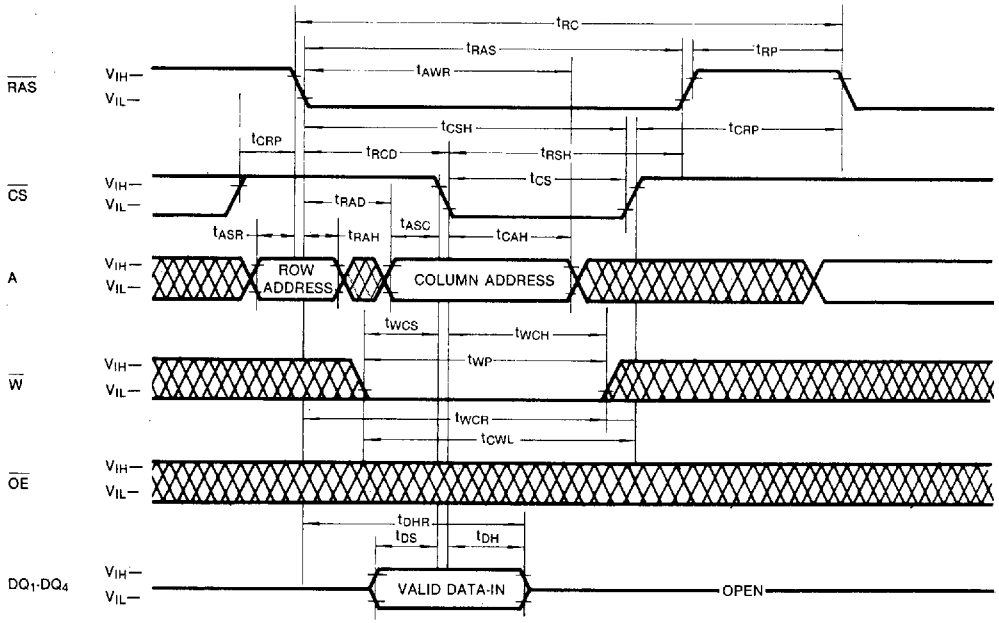
TIMING DIAGRAMS

READ CYCLE

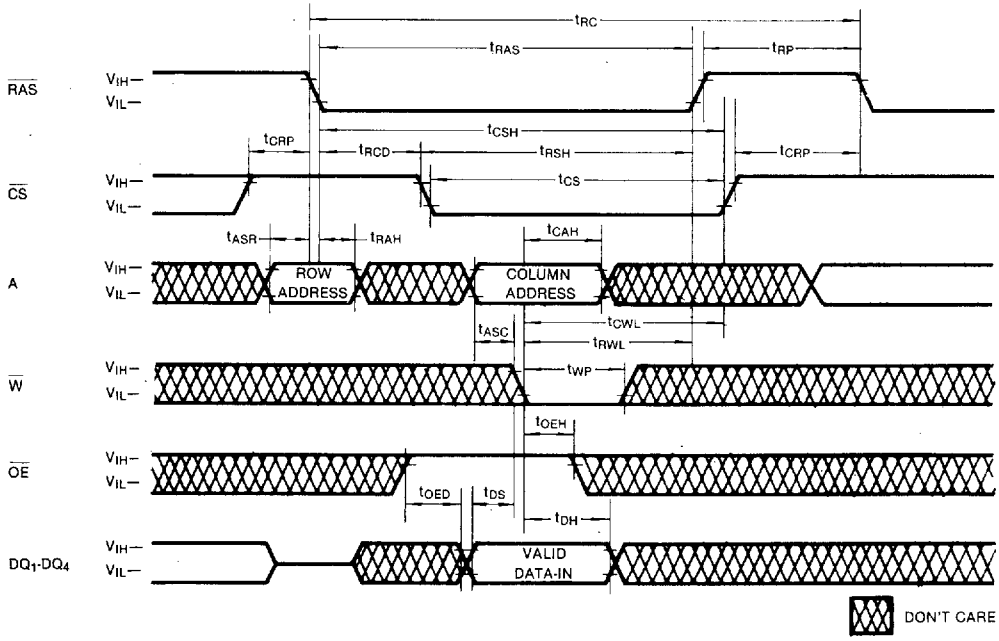


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)



WRITE CYCLE (OE CONTROLLED WRITE)



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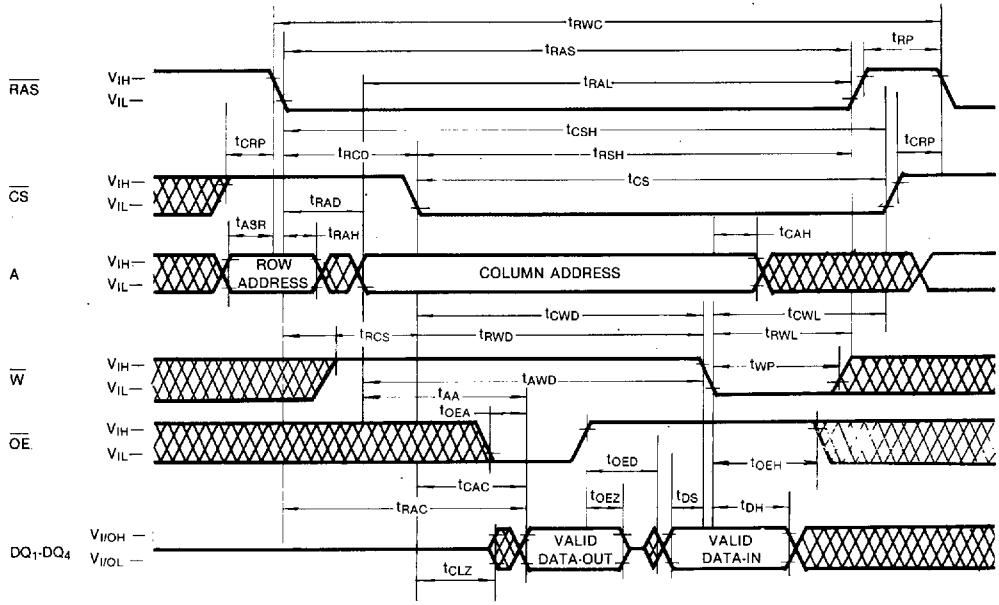
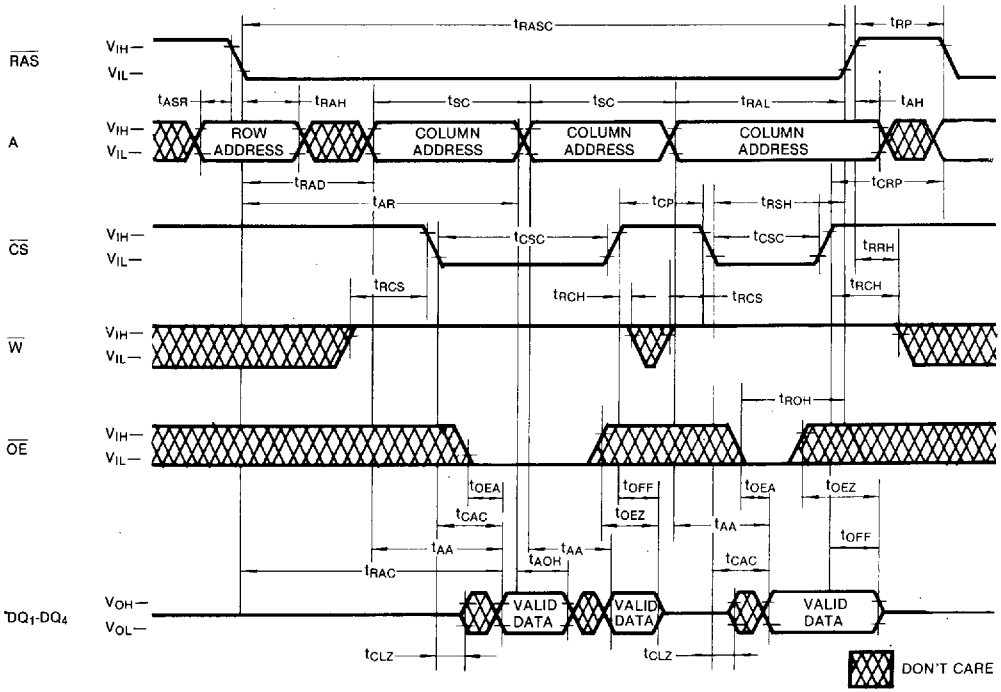
TIMING DIAGRAMS (Continued)

READ-WRITE/READ-MODIFY-WRITE CYCLE

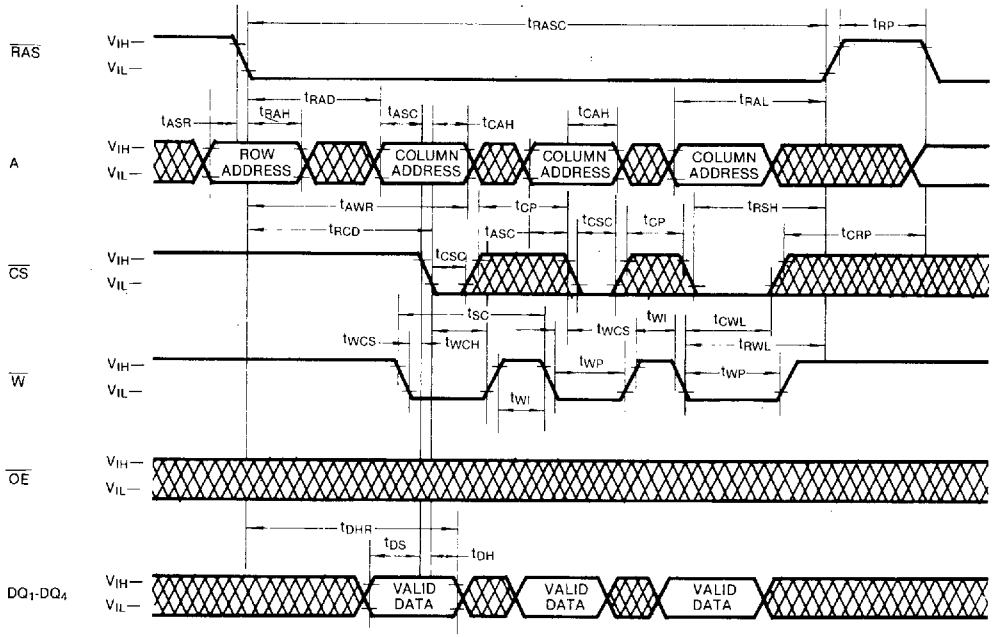


STATIC COLUMN MODE READ CYCLE

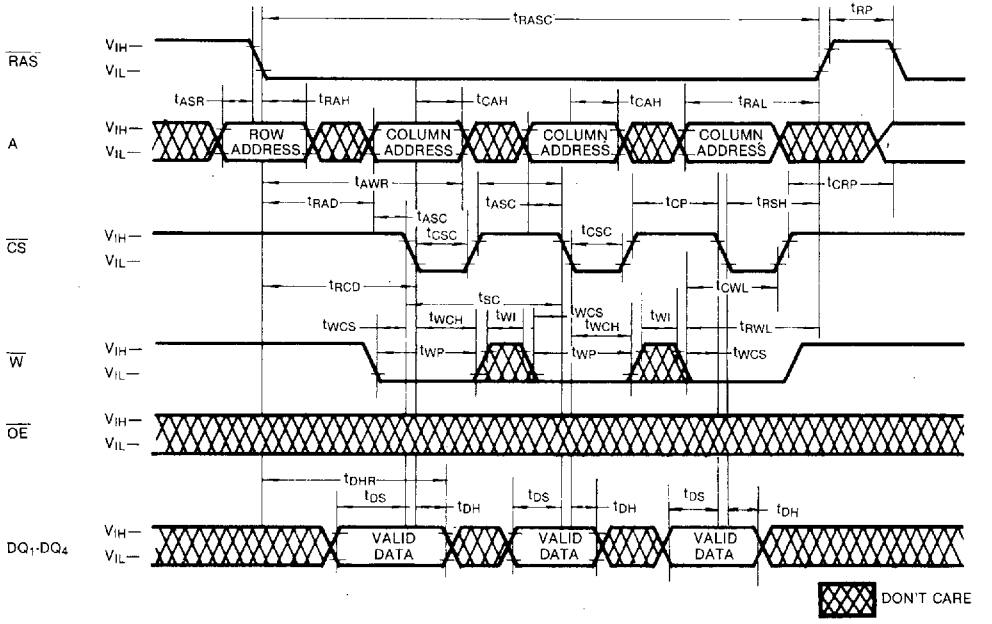


TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE WRITE CYCLE ($\overline{W}$ controlled early write)

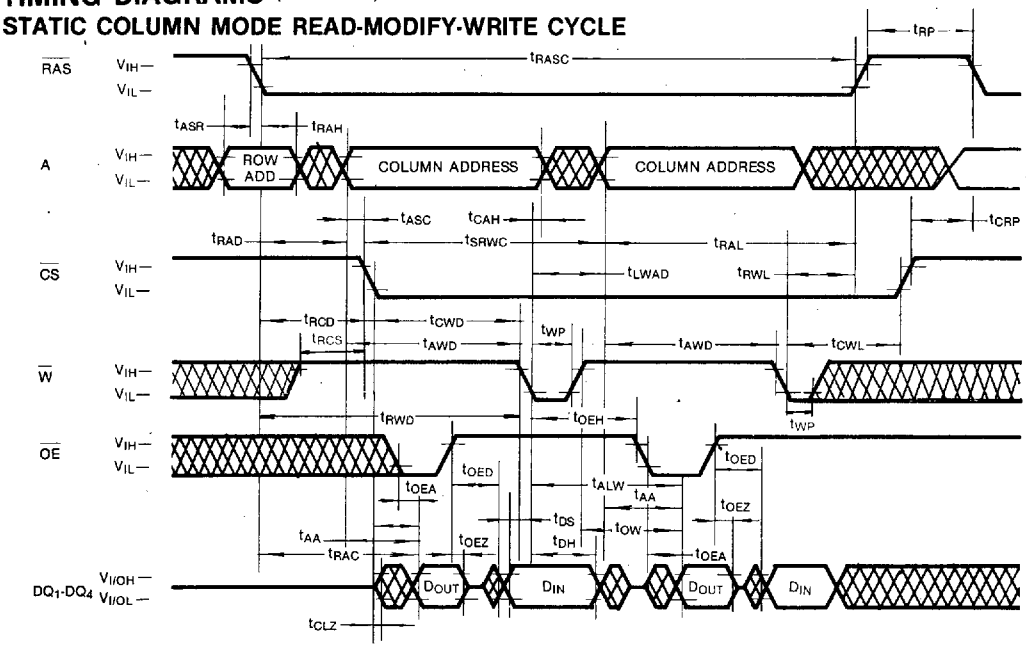


STATIC COLUMN MODE WRITE CYCLE ($\overline{CS}$ controlled early write)

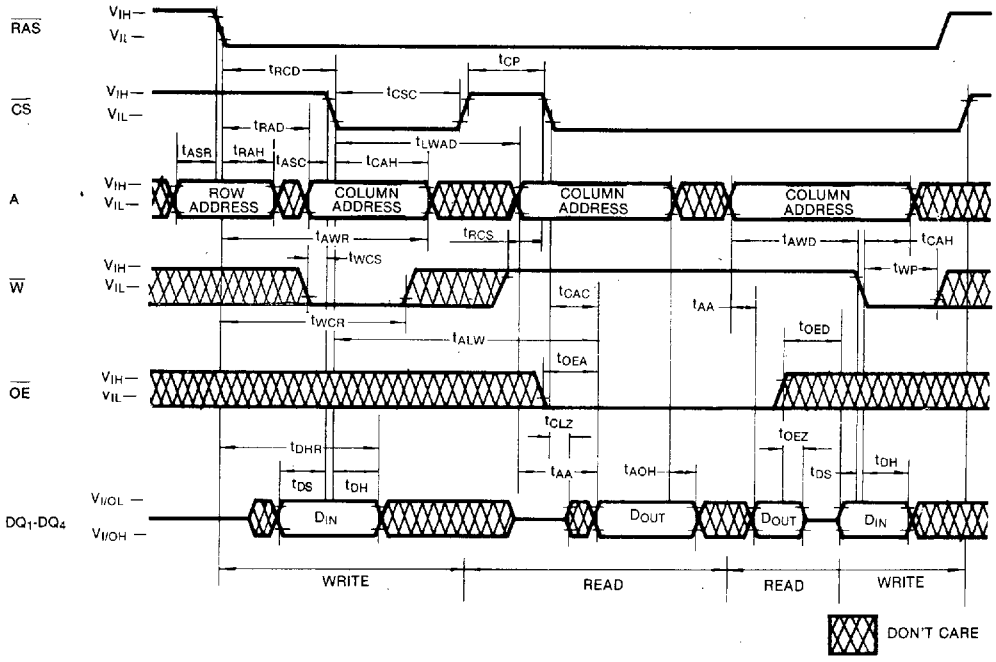


TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE READ-MODIFY-WRITE CYCLE



STATIC COLUMN MODE MIXED CYCLE



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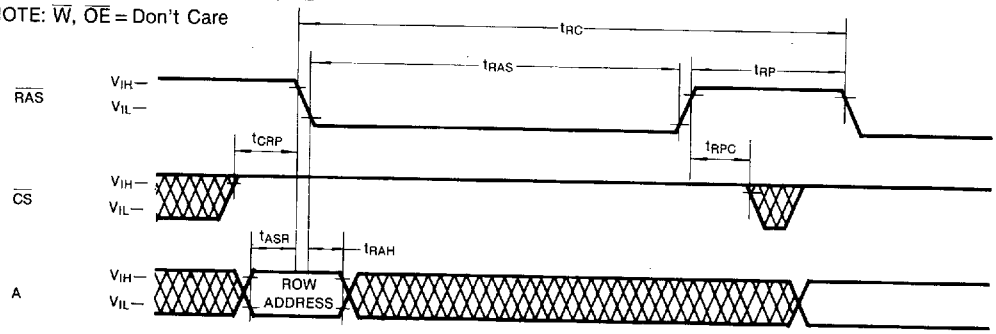
TIMING DIAGRAMS (Continued)

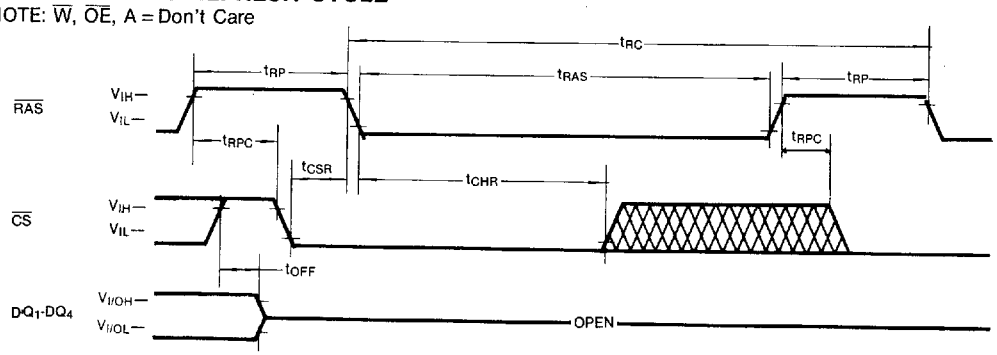
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE: $\overline{W}$, $\overline{OE}$ = Don't Care



$\overline{CS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: $\overline{W}$, $\overline{OE}$, A = Don't Care

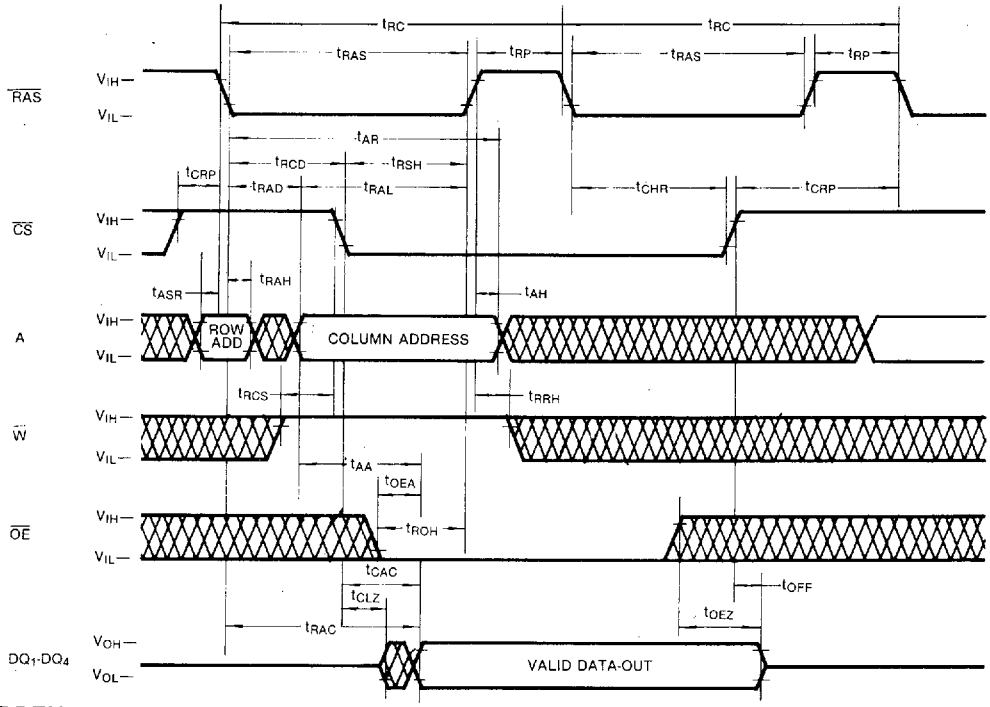


DON'T CARE

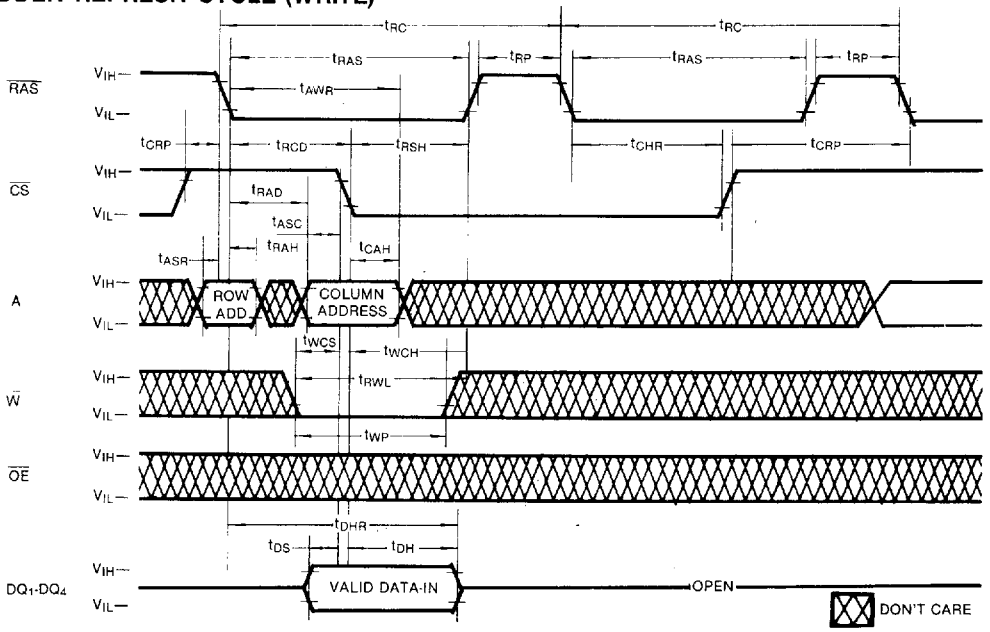
3

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



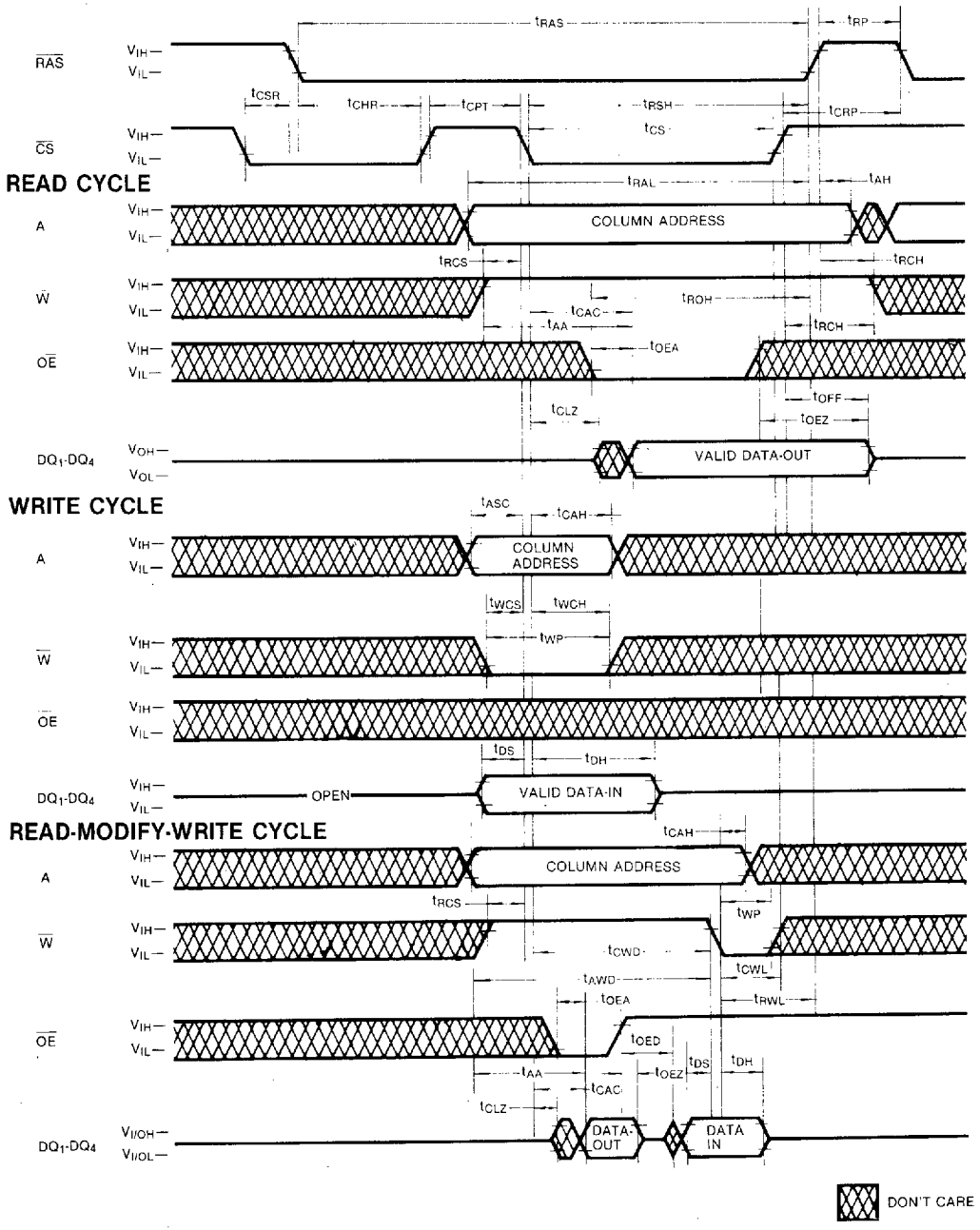
HIDDEN REFRESH CYCLE (WRITE)



SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

$\overline{CS}$-BEFORE-RAS REFRESH COUNTER TEST CYCLE



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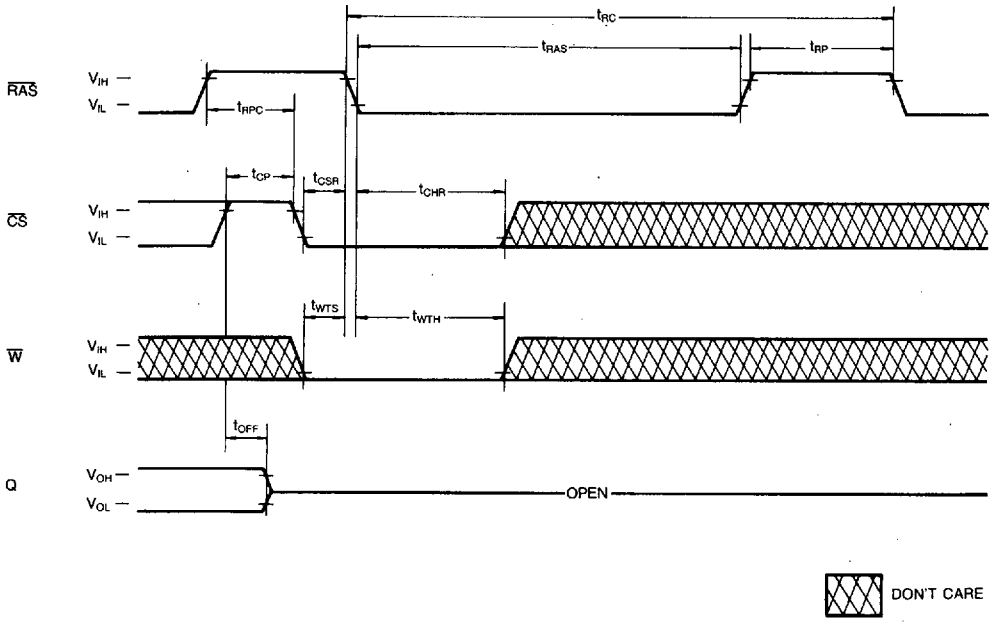
TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

NOTE: D, Address=Don't Care



TEST MODE DESCRIPTION

The KM44C1002C is the RAM organized 1,048,576 words by 4 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. Column address bit A_0 is not used. If, upon reading, two bits on one I/O pin are equal (all "1"s or "0"s), the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In "Test Mode", the 1M×4 DRAM can be tested as if it were a 512K×4 DRAM. $\overline{W}$, $\overline{CS}$ Before $\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CS}$-Before-$\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/2 in cases of N test pattern).

DEVICE OPERATION

Device Operation

The KM44C1002C contains 4,194,304 memory locations. organized as 1,048,576 four-bit words. TwentytWo address bits are required to address a particular 4-bit word in the memory array. Since the KM44C1002C has only 10 address input pins, time multiplexed addressing is used to input 10 row and 10 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe $\overline{CS}$ and the valid row and column address inputs.

Operation of the KM44C1002C begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CS}$ remains high. Then the address on the 10 address input pins is changed from a row address to a column address and is strobed in by $\overline{CS}$. This is the beginning of any KM44C1002C cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CS}$ pulse widths are specified by t_{RAS}(min) and t_{CS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM44C1002C bigin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the addess time also depends on the falling edge of $\overline{CS}$ and on the valid column address transition.

If $\overline{CS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAD}(max) then the access time to valid data is specified by t_{RAC}(min). However, if $\overline{CS}$ goes low after t_{RCD}(max) or if the column address becomes valid after t_{RAD}(max), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to meet both t_{RCD}(max) and t_{RAD}(max).

The KM44C1002C has common data I/O pins. For this reason and output enable control input ($\overline{OE}$) has been provided so the output buffer can be precisely controlled. For data to appear at the outputs. $\overline{OE}$ must be low for the period of time defined by t_{OEA} and t_{OEZ}.

Write

The KM44C1002C can perform early write, late write and read-modify-write cycles. The differece between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$ and $\overline{CS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CS}$. The 4-bit wide data at the data input pins is written into the addressed memory cells. Throughout the early write cycle the output remain in the Hi-Z state. In the early write cycle the output buffers remain in the Hi-Z state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the daaressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CS}$ and meeting the data sheet read-modify-write cycle timing requirements. The output enable input ($\overline{OE}$) must be low during the time defined by t_{OEA} and t_{OEZ} for data to apear at the outputs If t_{CWD} and t_{RWD} are not to the $\overline{OE}$ timing requirements prevents bus contention on the KM44C1002C's DQ pins.

Data Output

The KM44C1002C has a three-state output buffer which is controlled by $\overline{CS}$and $\overline{OE}$. Whenever $\overline{CS}$ or $\overline{OE}$ is high(V_{IH}) the output are in the high impedance(Hi-Z) state. In any cycle in which valid data appears at the output, the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing paraneters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM44C1002C operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Static Column Mode Read, Static Column Mode Read-Modify-Write.

DEVICE OPERATION (Continued)

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Static Column Mode Write, $\overline{CS}$-before-$\overline{RAS}$ Refresh, $\overline{CS}$-only cycle.

Indeterminate Output State: Delayed Write (t_{CWD} or t_{RWD})

Refresh

The data in the KM44C1002C is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 16ms. Either a burst refresh or distributed refresh may be used. There are several ways to accomplish this.

$\overline{RAS}$-Only-Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CS}$ remains high. This cycle must be repeated for each for each of the 1024 rw address. (A_0~A_9).

$\overline{CS}$-before-$\overline{RAS}$ Refresh: The KM44C1002C has $\overline{CS}$-Before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CS}$ active time and cycling $\overline{RAS}$. The KM44C1002C hidden refresh cycle is actually $\overline{CS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM44C1002C by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantateous to perform refresh in this mammer but in gheneral $\overline{RAS}$-only or $\overline{CS}$-before-$\overline{RAS}$ refresh is the preferred method.

Power-up

If $\overline{RAS}$= V_{SS} during power-up, the KM44C1002C might begin an active cycle. This coundition results in higher than necessary current demands from the power supplu during power-up. It is recommended that $\overline{RAS}$ and $\overline{CS}$ rrack with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.

An initial pause of 200μsec is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 8 msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM44C1002C inputs act like unterminated transmission lines resulting in significant overshoot and undershoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short sa possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM44C1002C input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

A high frequency 0.1μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each KM44C1002C using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM44C1002C and they supply much of the current used by the KM44C1002C during cycling.

DEVICE OPERATION (Continued)

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Address and control lines should be as short as possible to avoid skew. In boards with may DRAMs these lines should fan out from a central point like a fork or comb rather than being connected in a serpentine pattern. Also the control logic should be centrally located on the memory boards to facilitate the shortest possible address and control lines to all the DRAMs.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the V_{CC} to V_{SS} voltage (measured at the device pins) should not exceed 500mV.

A high frequency 0.1μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of eachKM44C1002Busing the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM44C1002Band they supply much of the current used by theKM44C1002Bduring cycling.

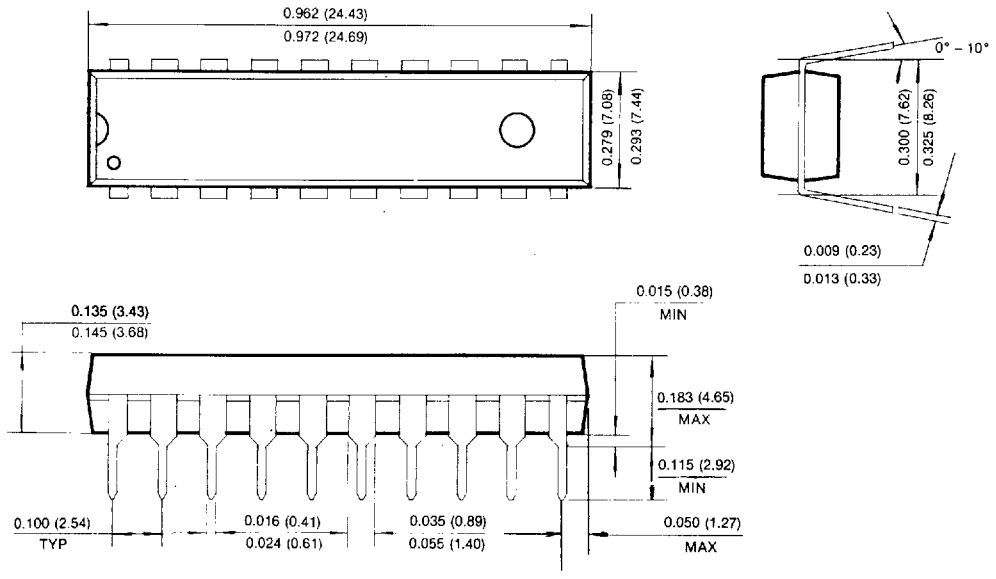
In addition, a large tantalum capacitor with a value of 47μF to 100μF should be used for bulk decoupling to recharge the 0.1μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

3

PACKAGE DIMENSIONS

20-LEAD PLASTIC DUAL IN-LINE PACKAGE

Units: Inches (millimeters)



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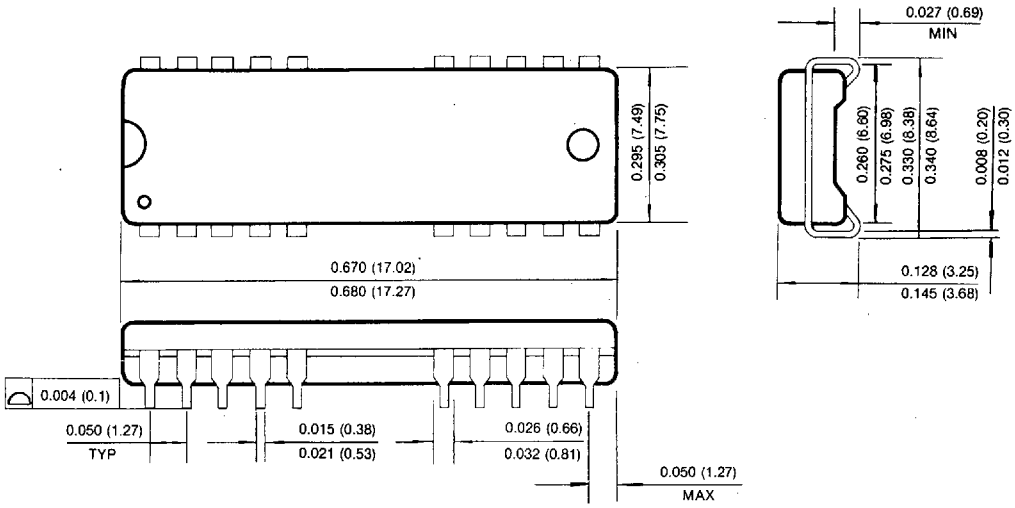
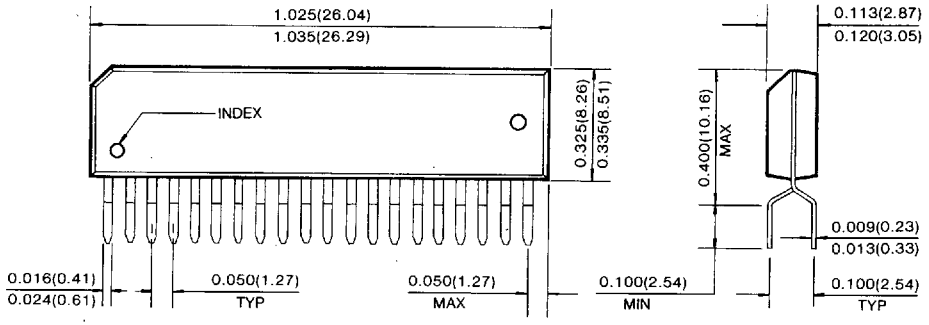
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE



PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II) (Forward and Reverse Type)

Units: Inches (millimeters)