NEC

MOS INTEGRATED CIRCUIT

Phase-out/Discontinued

μPD98412

1.5G ATM SWITCH LSI

DESCRIPTION

The μPD98412 (NEASCOT-X15) is an LSI integrating ATM switch functions on a single chip. It has UTOPIA Level2 interfaces and can switch 30 × 30 circuits by connecting multiple PHY devices. This LSI employs a shared buffer non-blocking type switch and realizes a switch capacity of 1.5G bps by using an externally connected SRAM for buffering cells.

For a detailed description of the functions of the controller, refer to the following User's Manual:
μPD98412 User's Manual: S14169E

FEATURES

- Conforms to ATM FORUM UNI Version 3.1 & Traffic Management 4.0
- Realizes all switch functions with a single chip
- Non-blocking type with switch capacity of 1.5G bps
- UTOPIA Level2 interface allowing you to select bit widths
  (4 ports × 8 bits, 2 ports × 8 bits + 1 port × 16 bits, 2 ports × 16 bits)
- Various polling modes for UTOPIA Level2 interface
- Can switch 30 logical ports
- Multi-speed (622M bps, 155M bps, 52M bps, 25M bps, etc.)
- Microprocessor connecting port can be set for signaling processing and OAM cell processing
- Supports 16K/32K/64K uni-cast VP/VC and 1K/2K/4K multi-cast VP/VC
- Shared buffer architecture using standard SRAM
- Cell buffer capacity: 12.8K/25.6K/51.2K cells
- Supports four QOS classes (CBR, VBR, ABR, UBR)
- ABR traffic control (binary mode)
- Supports EPD (Early Packet Discard) and PPD (Partial Packet Discard)
- +3.3-V single power source (directly connectable with +5-V TTL level signals)
- Test function: Supports JTAG (IEEE 1149.1)

Remark Active low pins are indicated as ×××_B (symbol_B after pin names) in this document.

ORDERING INFORMATION

Part Number	Package
μPD98412N7-H6	576-pin tape BGA (40 × 40)

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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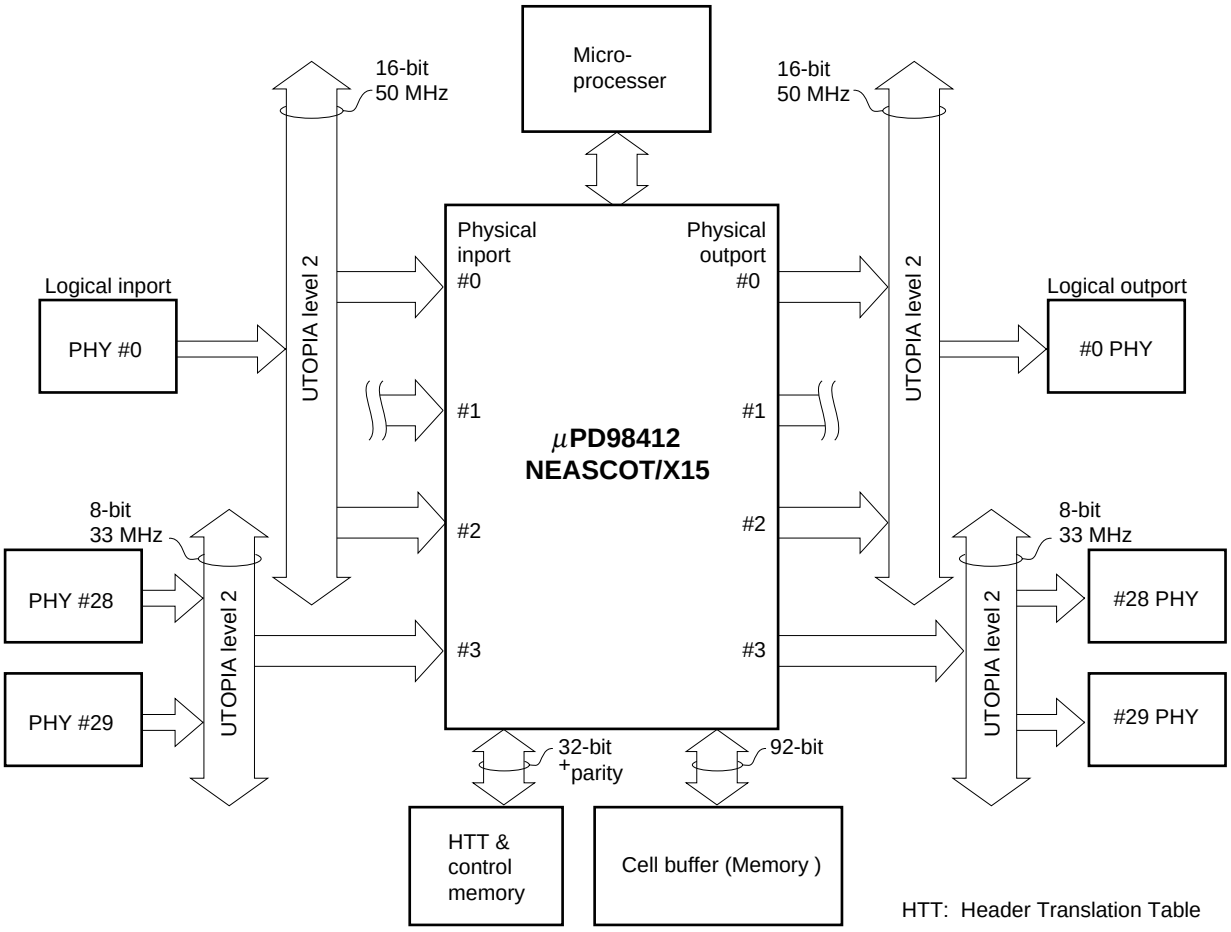
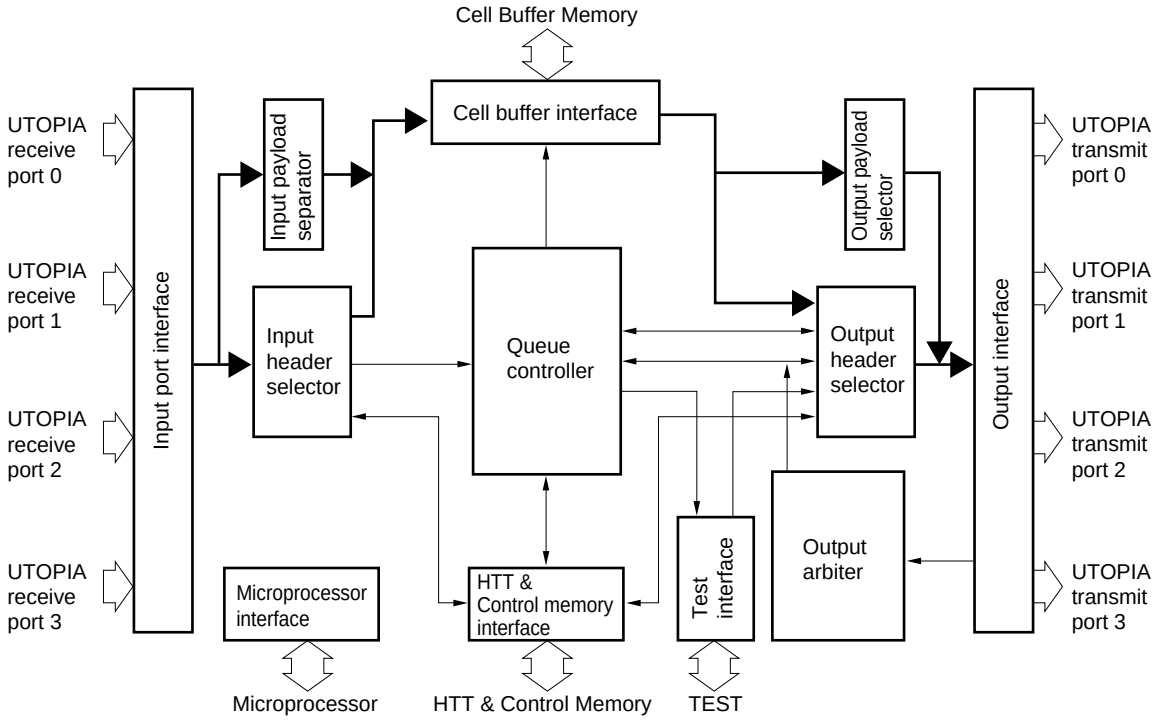
The mark ★ shows major revised points.

EXAMPLE OF SYSTEM CONFIGURATION (APPLICATION)

The μPD98412 can be used to realize an ATM layer cell switching function by connecting it to a microprocessor, SRAM for use as a cell buffer, and a header translation table (HTT)/SRAM for storing control information as shown below.

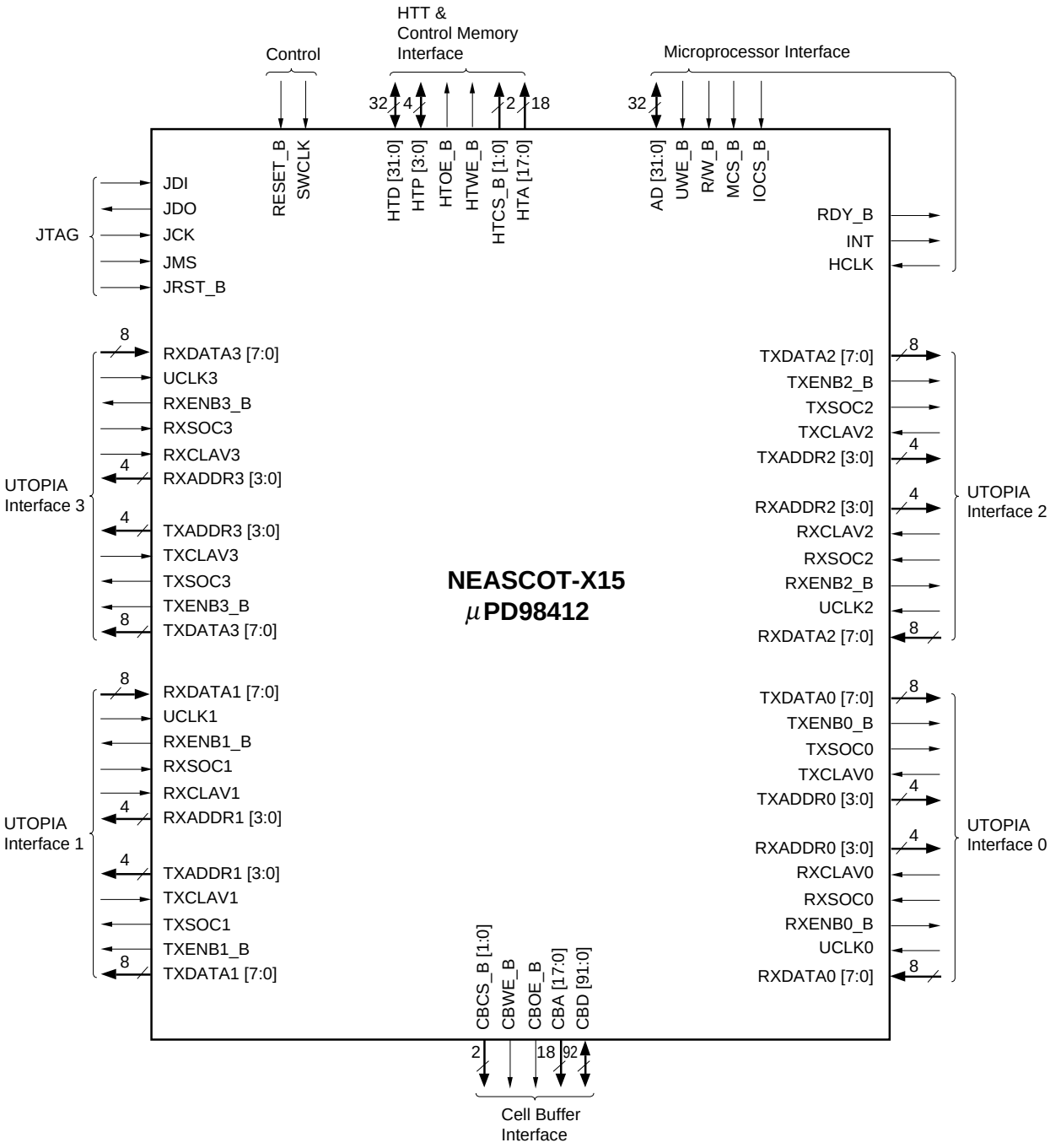


BLOCK DIAGRAM

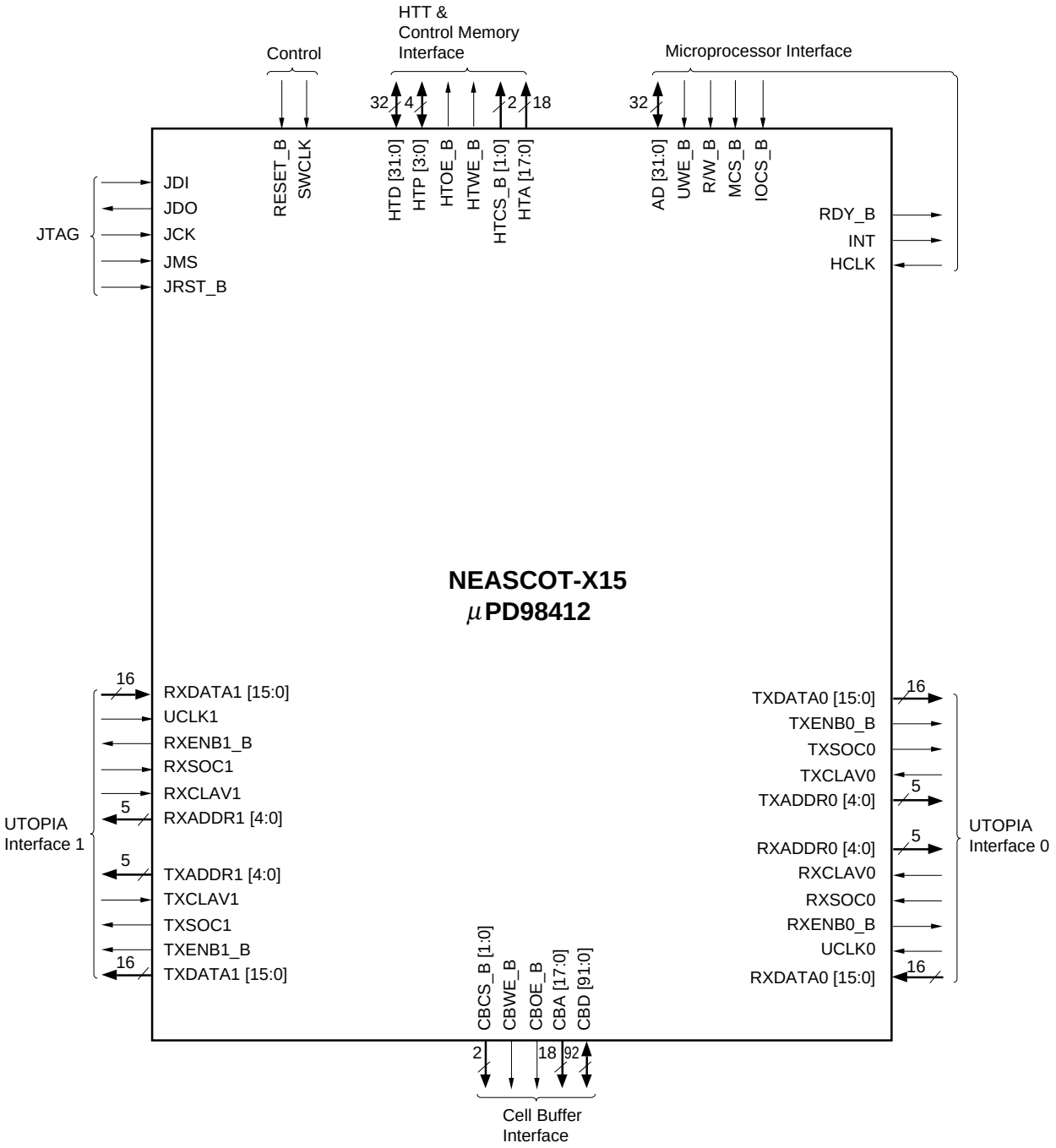


PIN CONFIGURATION

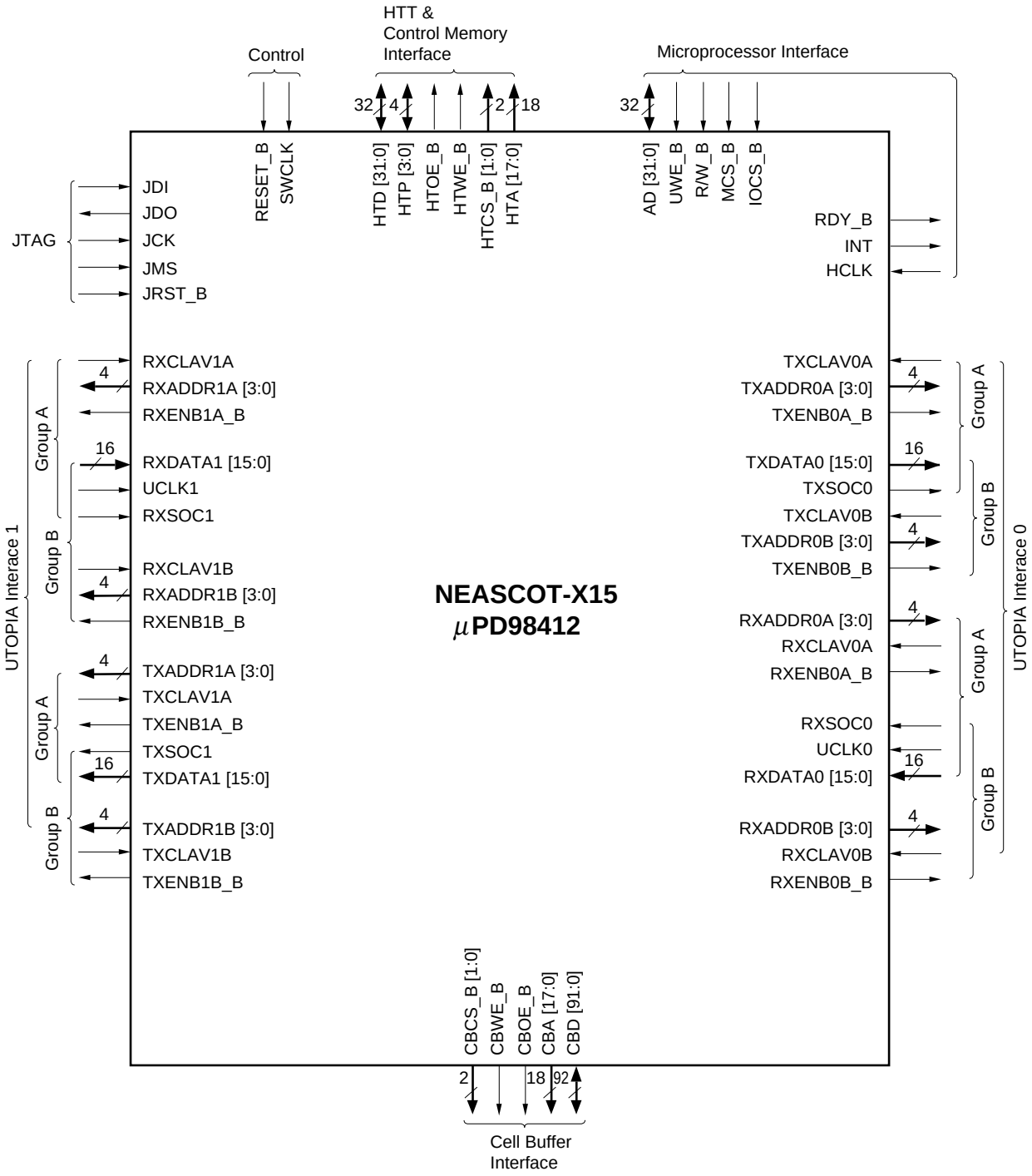
(1) 8-bit 12-PHY polling mode/15-PHY polling mode



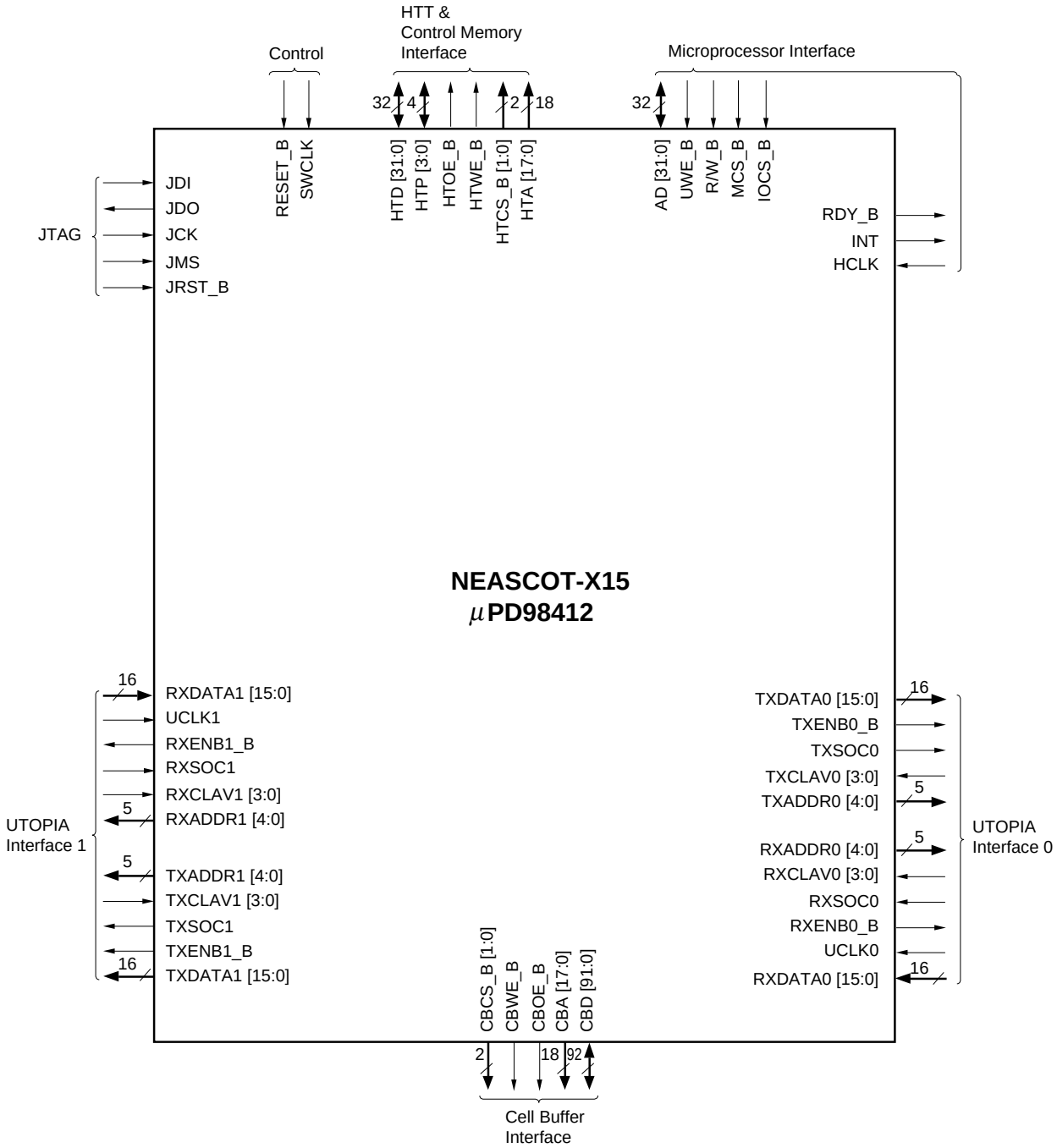
(2) 16-bit multiplexed status polling mode



(3) 16-bit 2-group weighted polling mode

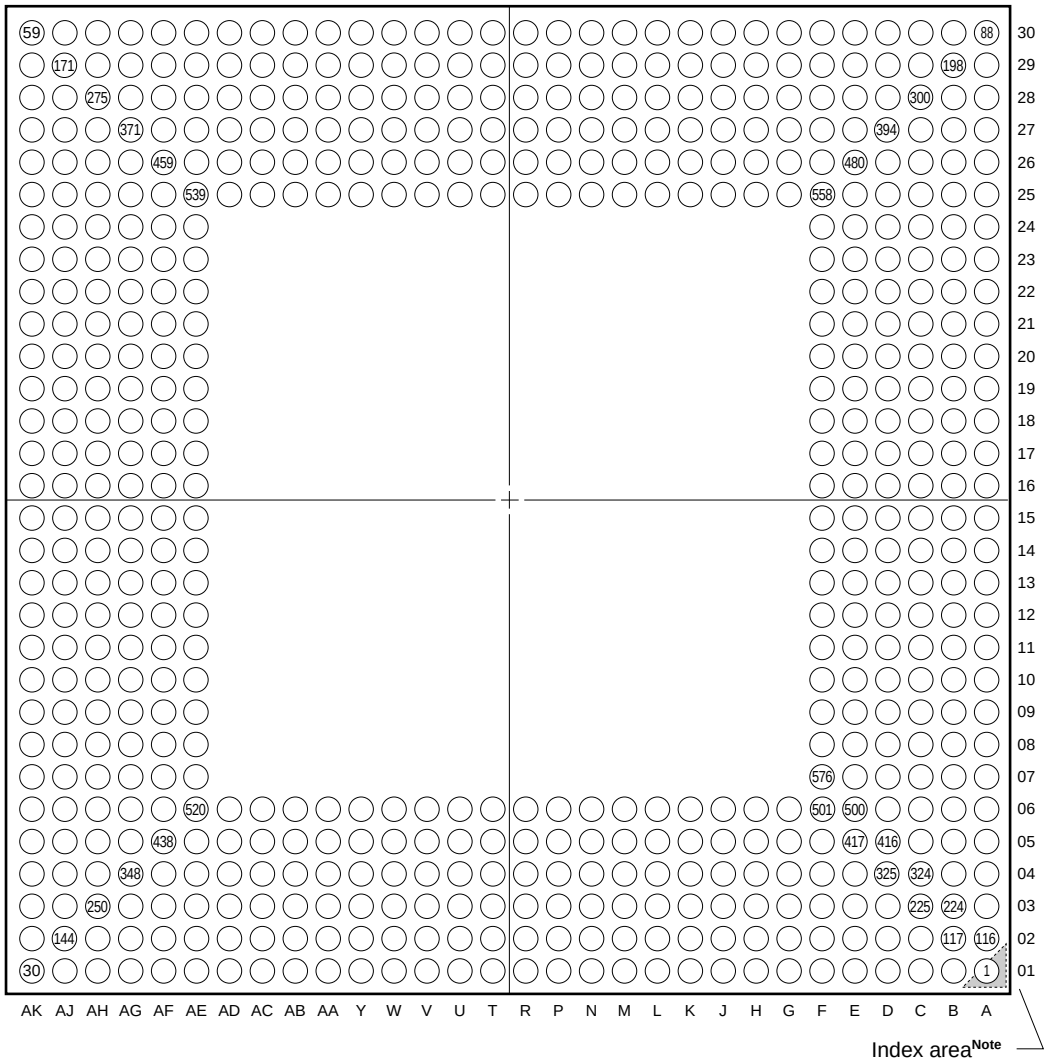


(4) 16-bit 1-group weighted polling mode



PIN CONFIGURATION (BOTTOM VIEW)

- **576-pin tape BGA (40 × 40)**
  μPD98412N7-H6



Note The index area is shown in Top View.

PIN NAME

1. Power

V_{DD} : Supply Voltage
GND : Ground

2. Memory Interface

HTA17 - HTA0	: HTT Memory Address
HTD31 - HTD0	: HTT Memory Data Bus
HTP3 - HTP0	: HTT Memory Data Bus Parity
HTCS1_B, HTCS0_B	: HTT Memory Chip Select
HTWE_B	: HTT Memory Write Enable
HTOE_B	: HTT Memory Output Enable
CBA17 - CBA0	: Cell Buffer Memory Address
CBD91 - CBD0	: Cell Buffer Memory Data Bus
CBCS1_B, CBCS0_B	: Cell Buffer Memory Chip Select
CBWE_B	: Cell Buffer Memory Write Enable
CBOE_B	: Cell Buffer Memory Output Enable

3. CPU Interface

IOCS_B	: I/O Chip Select
MCS_B	: Memory Chip Select
RDY_B	: I/O Ready, Memory Ready
INT	: Interrupt Request
HCLK	: Host Clock
AD31 - AD00	: Address and Data
R/W_B	: Read/Write
UWE_B	: Upper Word Enable

4. JTAG

JDI	: JTAG Data Input
JDO	: JTAG Data Output
JCK	: JTAG Data Clock
JMS	: JTAG Mode Select
JRST_B	: JTAG Reset

5. Other

SWCLK	: System Clock
RESET_B	: Hardware Reset
IC	: Internal Connected
CG	: Connect Ground
PU	: Pull-up

6. UTOPIA

(1) 8-bit 12-PHY Polling Mode/15-PHY Polling Mode

UCLK0 : UTOPIA Clock
RXADDR03-RXADDR00 : Receive Address
RXDATA007-RXDATA000 : Receive Data Bus
RXSOC0 : Receive Start of Cell
RXENB0_B : Receive Enable Data Transfers
RXCLAV0 : Receive Cell Buffer Available
TXADDR03-TXADDR00 : Transmit Address
TXDATA007-TXDATA000 : Transmit Data Bus
TXSOC0 : Transmit Start of Cell
TXENB0_B : Transmit Enable Data Transfers
TXCLAV0 : Transmit Cell Buffer Available
UCLK1 : UTOPIA Clock
RXADDR13-RXADDR10 : Receive Address
RXDATA107-RXDATA100 : Receive Data Bus
RXSOC1 : Receive Start of Cell
RXENB1_B : Receive Enable Data Transfers
RXCLAV1 : Receive Cell Buffer Available
TXADDR13-TXADDR10 : Transmit Address
TXDATA107-TXDATA100 : Transmit Data Bus
TXSOC1 : Transmit Start of Cell
TXENB1_B : Transmit Enable Data Transfers
TXCLAV1 : Transmit Cell Buffer Available
UCLK2 : UTOPIA Clock
RXADDR23-RXADDR20 : Receive Address
RXDATA207-RXDATA200 : Receive Data Bus
RXSOC2 : Receive Start of Cell
RXENB2_B : Receive Enable Data Transfers
RXCLAV2 : Receive Cell Buffer Available
TXADDR23-TXADDR20 : Transmit Address
TXDATA207-TXDATA200 : Transmit Data Bus
TXSOC2 : Transmit Start of Cell
TXENB2_B : Transmit Enable Data Transfers
TXCLAV2 : Transmit Cell Buffer Available
UCLK3 : UTOPIA Clock
RXADDR33-RXADDR30 : Receive Address
RXDATA307-RXDATA300 : Receive Data Bus
RXSOC3 : Receive Start of Cell
RXENB3_B : Receive Enable Data Transfers
RXCLAV3 : Receive Cell Buffer Available
TXADDR33-TXADDR30 : Transmit Address
TXDATA307-TXDATA300 : Transmit Data Bus
TXSOC3 : Transmit Start of Cell
TXENB3_B : Transmit Enable Data Transfers
TXCLAV3 : Transmit Cell Buffer Available

(2) 16-bit Multiplexed Status Polling Mode

UCLK0 : UTOPIA Clock
RXADDR04-RXADDR00 : Receive Address
RXDATA015-RXDATA000 : Receive Data Bus
RXSOC0 : Receive Start of Cell
RXENB0_B : Receive Enable Data Transfers
RXCLAV0[3]-RXCLAV0[0] : Receive Cell Buffer Available
TXADDR04-TXADDR00 : Transmit Address
TXDATA015-TXDATA000 : Transmit Data Bus
TXSOC0 : Transmit Start of Cell
TXENB0_B : Transmit Enable Data Transfers
TXCLAV0[3]-TXCLAV0[0] : Transmit Cell Buffer Available
UCLK1 : UTOPIA Clock
RXADDR14-RXADDR10 : Receive Address
RXDATA115-RXDATA100 : Receive Data Bus
RXSOC1 : Receive Start of Cell
RXENB1_B : Receive Enable Data Transfers
RXCLAV1[3]-RXCLAV1[0] : Receive Cell Buffer Available
TXADDR14-TXADDR10 : Transmit Address
TXDATA115-TXDATA100 : Transmit Data Bus
TXSOC1 : Transmit Start of Cell
TXENB1_B : Transmit Enable Data
TXCLAV1[3]-TXCLAV1[0] : Transmit Cell Buffer Available

(3) 16-bit 2-Group Weighted Polling Mode

UCLK0	:	UTOPIA Clock
RXADDR0A3-RXADDR0A0	:	Receive Address
RXADDR0B3-RXADDR0B0	:	Receive Address
RXDATA015-RXDATA000	:	Receive Data Bus
RXSOC0	:	Receive Start of Cell
RXENB0A_B, RXENB0B_B	:	Receive Enable Data Transfers
RXCLAV0A, RXCLAV0B	:	Receive Cell Buffer Available
TXADDR0A3-TXADDR0A0	:	Transmit Address
TXADDR0B3-TXADDR0B0	:	Transmit Address
TXDATA015-TXDATA000	:	Transmit Data Bus
TXSOC0	:	Transmit Start of Cell
TXENB0A_B, TXENB0B_B	:	Transmit Enable Data Transfers
TXCLAV0A, TXCLAV0B	:	Transmit Cell Buffer Available
UCLK1	:	UTOPIA Clock
RXADDR1A3-RXADDR1A0	:	Receive Address
RXADDR1B3-RXADDR1B0	:	Receive Address
RXDATA115-RXDATA100	:	Receive Data Bus
RXSOC1	:	Receive Start of Cell
RXENB1A_B, RXENB1B_B	:	Receive Enable Data Transfers
RXCLAV1A, RXCLAV1B	:	Receive Cell Buffer Available
TXADDR1A3-TXADDR1A0	:	Transmit Address
TXADDR1B3-TXADDR1B0	:	Transmit Address
TXDATA115-TXDATA100	:	Transmit Data Bus
TXSOC1	:	Transmit Start of Cell
TXENB1A_B, TXENB1B_B	:	Transmit Enable Data Transfers
TXCLAV1A, TXCLAV1B	:	Transmit Cell Buffer Available

(4) 16-bit 1-Group Weighted Polling Mode

UCLK0	:	UTOPIA Clock
RXADDR04-RXADDR00	:	Receive Address
RXDATA015-RXDATA000	:	Receive Data Bus
RXSOC0	:	Receive Start of Cell
RXENB0_B	:	Receive Enable Data Transfers
RXCLAV0	:	Receive Cell Buffer Available
TXADDR04-TXADDR00	:	Transmit Address
TXDATA015-TXDATA000	:	Transmit Data Bus
TXSOC0	:	Transmit Start of Cell
TXENB0_B	:	Transmit Enable Data Transfers
TXCLAV0	:	Transmit Cell Buffer Available
UCLK1	:	UTOPIA Clock
RXADDR14-RXADDR10	:	Receive Address
RXDATA115-RXDATA100	:	Receive Data Bus
RXSOC1	:	Receive Start of Cell
RXENB1_B	:	Receive Enable Data Transfers
RXCLAV1	:	Receive Cell Buffer Available
TXADDR14-TXADDR10	:	Transmit Address
TXDATA115-TXDATA100	:	Transmit Data Bus
TXSOC1	:	Transmit Start of Cell
TXENB1_B	:	Transmit Enable Data Transfers
TXCLAV1	:	Transmit Cell Buffer Available

PIN LAYOUT

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Pin No.	Address	12-PHY Polling Mode/ 15-PHY Polling Mode	Multiplexed Status Polling Mode	2-Group Weighted Polling Mode	1-Group Weighted Polling Mode	I/O
1	A01	AD30	←	←	←	I/O
2	B01	GND	←	←	←	
3	C01	AD24	←	←	←	I/O
4	D01	AD20	←	←	←	I/O
5	E01	AD16	←	←	←	I/O
6	F01	GND	←	←	←	
7	G01	AD10	←	←	←	I/O
8	H01	AD06	←	←	←	I/O
9	J01	GND	←	←	←	
10	K01	AD01	←	←	←	I/O
11	L01	HTA17	←	←	←	O
12	M01	HTA13	←	←	←	O
13	N01	HTA09	←	←	←	O
14	P01	GND	←	←	←	
15	R01	HTA06	←	←	←	O
16	T01	HTA02	←	←	←	O
17	U01	HTCS0_B	←	←	←	O
18	V01	HTD31	←	←	←	I/O
19	W01	HTD29	←	←	←	I/O
20	Y01	V_{DD}	←	←	←	
21	AA01	HTD24	←	←	←	I/O
22	AB01	HTD21	←	←	←	I/O
23	AC01	HTD17	←	←	←	I/O
24	AD01	HTP1	←	←	←	I/O
25	AE01	V_{DD}	←	←	←	
26	AF01	GND	←	←	←	
27	AG01	HTD06	←	←	←	I/O
28	AH01	HTD05	←	←	←	I/O
29	AJ01	HTD01	←	←	←	I/O
30	AK01	PU	←	←	←	I
31	AK02	V_{DD}	←	←	←	
32	AK03	GND	←	←	←	
33	AK04	JCK	←	←	←	I
34	AK05	RXDATA307	RXDATA115	RXDATA115	RXDATA115	I
35	AK06	V_{DD}	←	←	←	
36	AK07	RXDATA301	RXDATA109	RXDATA109	RXDATA109	I
37	AK08	GND	←	←	←	
38	AK09	RXCLAV3	RXCLAV1[2]	RXCLAV1B	CG	I
39	AK10	V_{DD}	←	←	←	
40	AK11	TXADDR33	IC	TXADDR1B3	IC	O

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Pin No.	Address	12-PHY Polling Mode/ 15-PHY Polling Mode	Multiplexed Status Polling Mode	2-Group Weighted Polling Mode	1-Group Weighted Polling Mode	I/O
41	AK12	CG	TXCLAV1[3]	CG	CG	I
42	AK13	TXDATA307	TXDATA115	TXDATA115	TXDATA115	O
43	AK14	V_{DD}	←	←	←	
44	AK15	TXDATA304	TXDATA112	TXDATA112	TXDATA112	O
45	AK16	TXDATA300	TXDATA108	TXDATA108	TXDATA108	O
46	AK17	RXDATA104	RXDATA104	RXDATA104	RXDATA104	I
47	AK18	RXDATA100	RXDATA100	RXDATA100	RXDATA100	I
48	AK19	UCLK1	UCLK1	UCLK1	UCLK1	I
49	AK20	RXCLAV1	RXCLAV1[0]	RXCLAV1A	RXCLAV1	I
50	AK21	RXADDR12	RXADDR12	RXADDR1A2	RXADDR12	O
51	AK22	TXADDR12	TXADDR12	TXADDR1A2	TXADDR12	O
52	AK23	TXCLAV1	TXCLAV1[0]	TXCLAV1A	TXCLAV1	I
53	AK24	TXDATA107	TXDATA107	TXDATA107	TXDATA107	O
54	AK25	TXDATA103	TXDATA103	TXDATA103	TXDATA103	O
55	AK26	CBD87	←	←	←	I/O
56	AK27	CBD84	←	←	←	I/O
57	AK28	V_{DD}	←	←	←	
58	AK29	GND	←	←	←	
59	AK30	CBD77	←	←	←	I/O
60	AJ30	GND	←	←	←	
61	AH30	V_{DD}	←	←	←	
62	AG30	CBD68	←	←	←	I/O
63	AF30	CBD64	←	←	←	I/O
64	AE30	V_{DD}	←	←	←	
65	AD30	CBD58	←	←	←	I/O
66	AC30	CBD54	←	←	←	I/O
67	AB30	V_{DD}	←	←	←	
68	AA30	CBD49	←	←	←	I/O
69	Y30	CBD47	←	←	←	I/O
70	W30	CBCS1_B	←	←	←	O
71	V30	CBA17	←	←	←	O
72	U30	V_{DD}	←	←	←	
73	T30	CBA14	←	←	←	O
74	R30	CBA10	←	←	←	O
75	P30	CBA06	←	←	←	O
76	N30	CBA02	←	←	←	O
77	M30	CBA00	←	←	←	O
78	L30	V_{DD}	←	←	←	
79	K30	CBD39	←	←	←	I/O
80	J30	CBD35	←	←	←	I/O

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Pin No.	Address	12-PHY Polling Mode/ 15-PHY Polling Mode	Multiplexed Status Polling Mode	2-Group Weighted Polling Mode	1-Group Weighted Polling Mode	I/O
81	H30	V_{DD}	←	←	←	
82	G30	CBD29	←	←	←	I/O
83	F30	CBD25	←	←	←	I/O
84	E30	GND	←	←	←	
85	D30	CBD18	←	←	←	I/O
86	C30	V_{DD}	←	←	←	
87	B30	V_{DD}	←	←	←	
88	A30	CBD11	←	←	←	I/O
89	A29	V_{DD}	←	←	←	
90	A28	CBD05	←	←	←	I/O
91	A27	CBD01	←	←	←	I/O
92	A26	RXDATA005	RXDATA005	RXDATA005	RXDATA005	I
93	A25	RXDATA003	RXDATA003	RXDATA003	RXDATA003	I
94	A24	V_{DD}	←	←	←	
95	A23	RXCLAV0	RXCLAV0[0]	RXCLAV0A	RXCLAV0	I
96	A22	V_{DD}	←	←	←	
97	A21	TXADDR03	TXADDR03	TXADDR03	TXADDR03	O
98	A20	TXADDR01	TXADDR01	TXADDR01	TXADDR01	O
99	A19	TXSOC0	TXSOC0	TXSOC0	TXSOC0	O
100	A18	TXDATA005	TXDATA005	TXDATA005	TXDATA005	O
101	A17	GND	←	←	←	
102	A16	TXDATA001	TXDATA001	TXDATA001	TXDATA001	O
103	A15	RXDATA205	RXDATA013	RXDATA013	RXDATA013	I
104	A14	RXDATA201	RXDATA009	RXDATA009	RXDATA009	I
105	A13	RXENB2_B	IC	RXENB0B_B	IC	O
106	A12	RXCLAV2	RXCLAV0[2]	RXCLAV0B	CG	I
107	A11	RXADDR21	IC	RXADDR0B1	IC	O
108	A10	TXADDR22	IC	TXADDR0B2	IC	O
109	A09	TXCLAV2	TXCLAV0[2]	TXCLAV0B	CG	I
110	A08	GND	←	←	←	
111	A07	TXDATA203	TXDATA011	TXDATA011	TXDATA011	O
112	A06	V_{DD}	←	←	←	
113	A05	GND	←	←	←	
114	A04	R/W_B	←	←	←	I
115	A03	UWE_B	←	←	←	I
116	A02	CG	←	←	←	I
117	B02	AD29	←	←	←	I/O
118	C02	AD27	←	←	←	I/O
119	D02	V_{DD}	←	←	←	
120	E02	AD19	←	←	←	I/O

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Pin No.	Address	12-PHY Polling Mode/ 15-PHY Polling Mode	Multiplexed Status Polling Mode	2-Group Weighted Polling Mode	1-Group Weighted Polling Mode	I/O
121	F02	AD15	←	←	←	I/O
122	G02	AD11	←	←	←	I/O
123	H02	AD09	←	←	←	I/O
124	J02	AD05	←	←	←	I/O
125	K02	AD04	←	←	←	I/O
126	L02	AD00	←	←	←	I/O
127	M02	HTA14	←	←	←	O
128	N02	HTA10	←	←	←	O
129	P02	V_{DD}	←	←	←	
130	R02	HTA05	←	←	←	O
131	T02	HTA01	←	←	←	O
132	U02	HTWE_B	←	←	←	O
133	V02	HTD30	←	←	←	I/O
134	W02	HTD26	←	←	←	I/O
135	Y02	HTD25	←	←	←	I/O
136	AA02	HTD22	←	←	←	I/O
137	AB02	HTD20	←	←	←	I/O
138	AC02	HTD16	←	←	←	I/O
139	AD02	HTD13	←	←	←	I/O
140	AE02	HTD10	←	←	←	I/O
141	AF02	HTD07	←	←	←	I/O
142	AG02	HTD02	←	←	←	I/O
143	AH02	GND	←	←	←	
144	AJ02	GND	←	←	←	
145	AJ03	CBD91	←	←	←	I/O
146	AJ04	JDO	←	←	←	O
147	AJ05	V_{DD}	←	←	←	
148	AJ06	RXDATA306	RXDATA114	RXDATA114	RXDATA114	I
149	AJ07	RXDATA302	RXDATA110	RXDATA110	RXDATA110	I
150	AJ08	RXDATA300	RXDATA108	RXDATA108	RXDATA108	I
151	AJ09	RXENB3_B	IC	RXENB1B_B	IC	O
152	AJ10	V_{DD}	←	←	←	
153	AJ11	RXADDR30	RXADDR14	RXADDR1B0	RXADDR14	O
154	AJ12	TXADDR30	TXADDR14	TXADDR1B0	TXADDR14	O
155	AJ13	TXENB3_B	IC	TXENB1B_B	IC	O
156	AJ14	GND	←	←	←	
157	AJ15	TXDATA303	TXDATA111	TXDATA111	TXDATA111	O
158	AJ16	RXDATA107	RXDATA107	RXDATA107	RXDATA107	I
159	AJ17	RXDATA103	RXDATA103	RXDATA103	RXDATA103	I
160	AJ18	V_{DD}	←	←	←	

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Pin No.	Address	12-PHY Polling Mode/ 15-PHY Polling Mode	Multiplexed Status Polling Mode	2-Group Weighted Polling Mode	1-Group Weighted Polling Mode	I/O
161	AJ19	V_{DD}	←	←	←	
162	AJ20	GND	←	←	←	
163	AJ21	TXADDR13	TXADDR13	TXADDR1A3	TXADDR13	O
164	AJ22	TXADDR10	TXADDR10	TXADDR1A0	TXADDR10	O
165	AJ23	TXENB1_B	TXENB1_B	TXENB1A_B	TXENB1_B	O
166	AJ24	TXDATA104	TXDATA104	TXDATA104	TXDATA104	O
167	AJ25	TXDATA101	TXDATA101	TXDATA101	TXDATA101	O
168	AJ26	CBD85	←	←	←	I/O
169	AJ27	V_{DD}	←	←	←	
170	AJ28	CBD80	←	←	←	I/O
171	AJ29	CBD76	←	←	←	I/O
172	AH29	CBD74	←	←	←	I/O
173	AG29	GND	←	←	←	
174	AF29	CBD67	←	←	←	I/O
175	AE29	CBD63	←	←	←	I/O
176	AD29	CBD59	←	←	←	I/O
177	AC29	CBD57	←	←	←	I/O
178	AB29	CBD53	←	←	←	I/O
179	AA29	CBD52	←	←	←	I/O
180	Y29	CBD48	←	←	←	I/O
181	W29	CBD44	←	←	←	I/O
182	V29	CBOE_B	←	←	←	O
183	U29	GND	←	←	←	
184	T29	CBA13	←	←	←	O
185	R29	CBA09	←	←	←	O
186	P29	CBA05	←	←	←	O
187	N29	CBA01	←	←	←	O
188	M29	CBD41	←	←	←	I/O
189	L29	CBD40	←	←	←	I/O
190	K29	CBD36	←	←	←	I/O
191	J29	CBD34	←	←	←	I/O
192	H29	CBD30	←	←	←	I/O
193	G29	CBD26	←	←	←	I/O
194	F29	CBD23	←	←	←	I/O
195	E29	CBD19	←	←	←	I/O
196	D29	GND	←	←	←	
197	C29	CBD14	←	←	←	I/O
198	B29	CBD10	←	←	←	I/O
199	B28	CBD08	←	←	←	I/O
200	B27	CBD02	←	←	←	I/O

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Pin No.	Address	12-PHY Polling Mode/ 15-PHY Polling Mode	Multiplexed Status Polling Mode	2-Group Weighted Polling Mode	1-Group Weighted Polling Mode	I/O
201	B26	CBD00	←	←	←	I/O
202	B25	RXDATA004	RXDATA004	RXDATA004	RXDATA004	I
203	B24	RXDATA000	RXDATA000	RXDATA000	RXDATA000	I
204	B23	RXENB0_B	RXENB0_B	RXENB0A_B	RXENB0_B	O
205	B22	RXADDR03	RXADDR03	RXADDR0A3	RXADDR03	O
206	B21	RXADDR02	RXADDR02	RXADDR0A2	RXADDR02	O
207	B20	TXADDR02	TXADDR02	TXADDR0A2	TXADDR02	O
208	B19	TXCLAV0	TXCLAV0[0]	TXCLAV0A	TXCLAV0	I
209	B18	TXDATA006	TXDATA006	TXDATA006	TXDATA006	O
210	B17	TXDATA002	TXDATA002	TXDATA002	TXDATA002	O
211	B16	TXDATA000	TXDATA000	TXDATA000	TXDATA000	O
212	B15	RXDATA204	RXDATA012	RXDATA012	RXDATA012	I
213	B14	RXDATA200	RXDATA008	RXDATA008	RXDATA008	I
214	B13	RXSOC2	RXLLAV0[3]	CG	CG	I
215	B12	GND	←	←	←	
216	B11	TXADDR23	IC	TXADDR0B3	IC	O
217	B10	CG	TXCLAV0[3]	CG	CG	I
218	B09	TXENB2_B	IC	TXENB0B_B	IC	O
219	B08	TXDATA204	TXDATA012	TXDATA012	TXDATA012	O
220	B07	TXDATA200	TXDATA008	TXDATA008	TXDATA008	O
221	B06	IOCS_B	←	←	←	I
222	B05	CG	←	←	←	I
223	B04	CG	←	←	←	I
224	B03	IC	←	←	←	O
225	C03	AD28	←	←	←	I/O
226	D03	AD26	←	←	←	I/O
227	E03	AD22	←	←	←	I/O
228	F03	AD18	←	←	←	I/O
229	G03	AD14	←	←	←	I/O
230	H03	V_{DD}	←	←	←	
231	J03	AD08	←	←	←	I/O
232	K03	V_{DD}	←	←	←	
233	L03	GND	←	←	←	
234	M03	HTA15	←	←	←	O
235	N03	HTA11	←	←	←	O
236	P03	HTA07	←	←	←	O
237	R03	HTA03	←	←	←	O
238	T03	HTA00	←	←	←	O
239	U03	HTOE_B	←	←	←	O
240	V03	V_{DD}	←	←	←	

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Pin No.	Address	12-PHY Polling Mode/ 15-PHY Polling Mode	Multiplexed Status Polling Mode	2-Group Weighted Polling Mode	1-Group Weighted Polling Mode	I/O
241	W03	GND	←	←	←	
242	Y03	HTD23	←	←	←	I/O
243	AA03	V_{DD}	←	←	←	
244	AB03	GND	←	←	←	
245	AC03	HTD14	←	←	←	I/O
246	AD03	HTD11	←	←	←	I/O
247	AE03	HTP0	←	←	←	I/O
248	AF03	HTD03	←	←	←	I/O
249	AG03	HTD00	←	←	←	I/O
250	AH03	IC	←	←	←	O
251	AH04	CBD90	←	←	←	I/O
252	AH05	JDI	←	←	←	I
253	AH06	JMS	←	←	←	I
254	AH07	RXDATA305	RXDATA113	RXDATA113	RXDATA113	I
255	AH08	GND	←	←	←	
256	AH09	GND	←	←	←	
257	AH10	RXSOC3	RXCLAV1[3]	CG	CG	I
258	AH11	RXADDR31	IC	RXADDR1B1	IC	O
259	AH12	TXADDR31	IC	TXADDR1B1	IC	O
260	AH13	TXSOC3	IC	IC	IC	O
261	AH14	TXDATA305	TXDATA113	TXDATA113	TXDATA113	O
262	AH15	TXDATA301	TXDATA109	TXDATA109	TXDATA109	O
263	AH16	RXDATA106	RXDATA106	RXDATA106	RXDATA106	I
264	AH17	RXDATA102	RXDATA102	RXDATA102	RXDATA102	I
265	AH18	GND	←	←	←	
266	AH19	RXADDR13	RXADDR13	RXADDR1A3	RXADDR13	O
267	AH20	RXADDR10	RXADDR10	RXADDR1A0	RXADDR10	O
268	AH21	TXADDR11	TXADDR11	TXADDR1A1	TXADDR11	O
269	AH22	TXSOC1	TXSOC1	TXSOC1	TXSOC1	O
270	AH23	TXDATA105	TXDATA105	TXDATA105	TXDATA105	O
271	AH24	TXDATA102	TXDATA102	TXDATA102	TXDATA102	O
272	AH25	CBD86	←	←	←	I/O
273	AH26	CBD81	←	←	←	I/O
274	AH27	CBD79	←	←	←	I/O
275	AH28	CBD75	←	←	←	I/O
276	AG28	CBD73	←	←	←	I/O
277	AF28	CBD69	←	←	←	I/O
278	AE28	CBD66	←	←	←	I/O
279	AD28	CBD62	←	←	←	I/O
280	AC28	GND	←	←	←	

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Pin No.	Address	12-PHY Polling Mode/ 15-PHY Polling Mode	Multiplexed Status Polling Mode	2-Group Weighted Polling Mode	1-Group Weighted Polling Mode	I/O
281	AB28	CBD56	←	←	←	I/O
282	AA28	GND	←	←	←	
283	Y28	V_{DD}	←	←	←	
284	W28	CBD45	←	←	←	I/O
285	V28	CBWE_B	←	←	←	O
286	U28	CBA15	←	←	←	O
287	T28	CBA11	←	←	←	O
288	R28	CBA08	←	←	←	O
289	P28	CBA04	←	←	←	O
290	N28	V_{DD}	←	←	←	
291	M28	GND	←	←	←	
292	L28	CBD37	←	←	←	I/O
293	K28	V_{DD}	←	←	←	
294	J28	CBD31	←	←	←	I/O
295	H28	CBD27	←	←	←	I/O
296	G28	CBD24	←	←	←	I/O
297	F28	CBD20	←	←	←	I/O
298	E28	CBD15	←	←	←	I/O
299	D28	CBD13	←	←	←	I/O
300	C28	CBD09	←	←	←	I/O
301	C27	CBD07	←	←	←	I/O
302	C26	CBD03	←	←	←	I/O
303	C25	RXDATA007	RXDATA007	RXDATA007	RXDATA007	I
304	C24	GND	←	←	←	
305	C23	GND	←	←	←	
306	C22	RXSOC0	RXSOC0	RXSOC0	RXSOC0	I
307	C21	GND	←	←	←	
308	C20	V_{DD}	←	←	←	
309	C19	CG	TXCLAV0[1]	CG	CG	I
310	C18	TXDATA007	TXDATA007	TXDATA007	TXDATA007	O
311	C17	TXDATA003	TXDATA003	TXDATA003	TXDATA003	O
312	C16	RXDATA206	RXDATA014	RXDATA014	RXDATA014	I
313	C15	GND	←	←	←	
314	C14	GND	←	←	←	
315	C13	V_{DD}	←	←	←	
316	C12	RXADDR20	RXADDR04	RXADDR0B0	RXADDR04	O
317	C11	TXADDR20	TXADDR04	TXADDR0B0	TXADDR04	O
318	C10	TXSOC2	IC	IC	IC	O
319	C09	TXDATA205	TXDATA013	TXDATA013	TXDATA013	O
320	C08	TXDATA201	TXDATA009	TXDATA009	TXDATA009	O

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Pin No.	Address	12-PHY Polling Mode/ 15-PHY Polling Mode	Multiplexed Status Polling Mode	2-Group Weighted Polling Mode	1-Group Weighted Polling Mode	I/O
321	C07	CG	←	←	←	I
322	C06	RDY_B	←	←	←	O
323	C05	GND	←	←	←	
324	C04	V_{DD}	←	←	←	
325	D04	V_{DD}	←	←	←	
326	E04	AD25	←	←	←	I/O
327	F04	GND	←	←	←	
328	G04	AD17	←	←	←	I/O
329	H04	V_{DD}	←	←	←	
330	J04	GND	←	←	←	
331	K04	AD07	←	←	←	I/O
332	L04	V_{DD}	←	←	←	
333	M04	HTA16	←	←	←	O
334	N04	HTA12	←	←	←	O
335	P04	HTA08	←	←	←	O
336	R04	HTA04	←	←	←	O
337	T04	V_{DD}	←	←	←	
338	U04	HTP3	←	←	←	I/O
339	V04	GND	←	←	←	
340	W04	HTP2	←	←	←	I/O
341	Y04	GND	←	←	←	
342	AA04	V_{DD}	←	←	←	
343	AB04	HTD15	←	←	←	I/O
344	AC04	HTD12	←	←	←	I/O
345	AD04	HTD08	←	←	←	I/O
346	AE04	HTD04	←	←	←	I/O
347	AF04	RESET_B	←	←	←	I
348	AG04	IC	←	←	←	O
349	AG05	CBD89	←	←	←	I/O
350	AG06	IC	←	←	←	
351	AG07	JRST_B	←	←	←	I
352	AG08	GND	←	←	←	
353	AG09	V_{DD}	←	←	←	
354	AG10	UCLK3	CG	CG	CG	I
355	AG11	RXADDR32	IC	RXADDR1B2	IC	O
356	AG12	TXADDR32	IC	TXADDR1B2	IC	O
357	AG13	TXCLAV3	TXCLAV1[2]	TXCLAV1B	CG	I
358	AG14	TXDATA306	TXDATA114	TXDATA114	TXDATA114	O
359	AG15	TXDATA302	TXDATA110	TXDATA110	TXDATA110	O
360	AG16	V_{DD}	←	←	←	

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Pin No.	Address	12-PHY Polling Mode/ 15-PHY Polling Mode	Multiplexed Status Polling Mode	2-Group Weighted Polling Mode	1-Group Weighted Polling Mode	I/O
361	AG17	RXDATA101	RXDATA101	RXDATA101	RXDATA101	I
362	AG18	RXENB1_B	RXENB1_B	RXENB1A_B	RXENB1_B	O
363	AG19	RXADDR11	RXADDR11	RXADDR1A1	RXADDR11	O
364	AG20	GND	←	←	←	
365	AG21	GND	←	←	←	
366	AG22	TXDATA106	TXDATA106	TXDATA106	TXDATA106	O
367	AG23	GND	←	←	←	
368	AG24	GND	←	←	←	
369	AG25	CBD82	←	←	←	I/O
370	AG26	GND	←	←	←	
371	AG27	V_{DD}	←	←	←	
372	AF27	CBD72	←	←	←	I/O
373	AE27	CBD70	←	←	←	I/O
374	AD27	CBD65	←	←	←	I/O
375	AC27	GND	←	←	←	
376	AB27	V_{DD}	←	←	←	
377	AA27	CBD55	←	←	←	I/O
378	Y27	GND	←	←	←	
379	W27	CBD46	←	←	←	I/O
380	V27	CBCS0_B	←	←	←	O
381	U27	CBA16	←	←	←	O
382	T27	CBA12	←	←	←	O
383	R27	V_{DD}	←	←	←	
384	P27	CBA03	←	←	←	O
385	N27	GND	←	←	←	
386	M27	CBD38	←	←	←	I/O
387	L27	GND	←	←	←	
388	K27	GND	←	←	←	
389	J27	CBD28	←	←	←	I/O
390	H27	GND	←	←	←	
391	G27	CBD21	←	←	←	I/O
392	F27	CBD16	←	←	←	I/O
393	E27	V_{DD}	←	←	←	
394	D27	GND	←	←	←	
395	D26	CBD06	←	←	←	I/O
396	D25	GND	←	←	←	
397	D24	RXDATA006	RXDATA006	RXDATA006	RXDATA006	I
398	D23	V_{DD}	←	←	←	
399	D22	UCLK0	UCLK0	UCLK0	UCLK0	I
400	D21	CG	RXCLAV0[1]	CG	CG	I

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Pin No.	Address	12-PHY Polling Mode/ 15-PHY Polling Mode	Multiplexed Status Polling Mode	2-Group Weighted Polling Mode	1-Group Weighted Polling Mode	I/O
401	D20	GND	←	←	←	
402	D19	TXADDR00	TXADDR00	TXADDR0A0	TXADDR00	O
403	D18	TXENB0_B	TXENB0_B	TXENB0A_B	TXENB0_B	O
404	D17	TXDATA004	TXDATA004	TXDATA004	TXDATA004	O
405	D16	RXDATA207	RXDATA015	RXDATA015	RXDATA015	I
406	D15	V_{DD}	←	←	←	
407	D14	UCLK2	CG	CG	CG	I
408	D13	RXADDR23	IC	RXADDR0B3	IC	O
409	D12	TXADDR21	IC	TXADDR0B1	IC	O
410	D11	GND	←	←	←	
411	D10	TXDATA206	TXDATA014	TXDATA014	TXDATA014	O
412	D09	TXDATA202	TXDATA010	TXDATA010	TXDATA010	O
413	D08	GND	←	←	←	
414	D07	INT	←	←	←	O
415	D06	CG	←	←	←	I
416	D05	AD31	←	←	←	I/O
417	E05	V_{DD}	←	←	←	
418	F05	V_{DD}	←	←	←	
419	G05	AD21	←	←	←	I/O
420	H05	V_{DD}	←	←	←	
421	J05	AD12	←	←	←	I/O
422	K05	V_{DD}	←	←	←	
423	L05	AD02	←	←	←	I/O
424	M05	V_{DD}	←	←	←	
425	N05	GND	←	←	←	
426	P05	V_{DD}	←	←	←	
427	R05	V_{DD}	←	←	←	
428	T05	HTCS1_B	←	←	←	O
429	U05	V_{DD}	←	←	←	
430	V05	HTD28	←	←	←	I/O
431	W05	V_{DD}	←	←	←	
432	Y05	HTD19	←	←	←	I/O
433	AA05	V_{DD}	←	←	←	
434	AB05	GND	←	←	←	
435	AC05	V_{DD}	←	←	←	
436	AD05	V_{DD}	←	←	←	
437	AE05	SWCLK	←	←	←	I
438	AF05	V_{DD}	←	←	←	
439	AF06	CBD88	←	←	←	I/O
440	AF07	GND	←	←	←	

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Pin No.	Address	12-PHY Polling Mode/ 15-PHY Polling Mode	Multiplexed Status Polling Mode	2-Group Weighted Polling Mode	1-Group Weighted Polling Mode	I/O
441	AF08	V_{DD}	←	←	←	
442	AF09	RXDATA303	RXDATA111	RXDATA111	RXDATA111	I
443	AF10	V_{DD}	←	←	←	
444	AF11	GND	←	←	←	
445	AF12	V_{DD}	←	←	←	
446	AF13	V_{DD}	←	←	←	
447	AF14	V_{DD}	←	←	←	
448	AF15	V_{DD}	←	←	←	
449	AF16	RXDATA105	RXDATA105	RXDATA105	RXDATA105	I
450	AF17	V_{DD}	←	←	←	
451	AF18	RXSOC1	RXSOC1	RXSOC1	RXSOC1	I
452	AF19	V_{DD}	←	←	←	
453	AF20	V_{DD}	←	←	←	
454	AF21	V_{DD}	←	←	←	
455	AF22	V_{DD}	←	←	←	
456	AF23	V_{DD}	←	←	←	
457	AF24	CBD83	←	←	←	I/O
458	AF25	V_{DD}	←	←	←	
459	AF26	V_{DD}	←	←	←	
460	AE26	GND	←	←	←	
461	AD26	V_{DD}	←	←	←	
462	AC26	V_{DD}	←	←	←	
463	AB26	CBD60	←	←	←	I/O
464	AA26	V_{DD}	←	←	←	
465	Y26	CBD50	←	←	←	I/O
466	W26	V_{DD}	←	←	←	
467	V26	V_{DD}	←	←	←	
468	U26	V_{DD}	←	←	←	
469	T26	V_{DD}	←	←	←	
470	R26	CBA07	←	←	←	O
471	P26	V_{DD}	←	←	←	
472	N26	CBD43	←	←	←	I/O
473	M26	V_{DD}	←	←	←	
474	L26	CBD33	←	←	←	I/O
475	K26	V_{DD}	←	←	←	
476	J26	V_{DD}	←	←	←	
477	H26	V_{DD}	←	←	←	
478	G26	CBD17	←	←	←	I/O
479	F26	GND	←	←	←	
480	E26	V_{DD}	←	←	←	

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Pin No.	Address	12-PHY Polling Mode/ 15-PHY Polling Mode	Multiplexed Status Polling Mode	2-Group Weighted Polling Mode	1-Group Weighted Polling Mode	I/O
481	E25	V_{DD}	←	←	←	
482	E24	V_{DD}	←	←	←	
483	E23	V_{DD}	←	←	←	
484	E22	RXDATA001	RXDATA001	RXDATA001	RXDATA001	I
485	E21	V_{DD}	←	←	←	
486	E20	RXADDR00	RXADDR00	RXADDR0A0	RXADDR00	O
487	E19	V_{DD}	←	←	←	
488	E18	V_{DD}	←	←	←	
489	E17	V_{DD}	←	←	←	
490	E16	V_{DD}	←	←	←	
491	E15	RXDATA202	RXDATA010	RXDATA010	RXDATA010	I
492	E14	V_{DD}	←	←	←	
493	E13	RXADDR22	IC	RXADDR0B2	IC	O
494	E12	V_{DD}	←	←	←	
495	E11	V_{DD}	←	←	←	
496	E10	V_{DD}	←	←	←	
497	E09	HCLK	←	←	←	I
498	E08	V_{DD}	←	←	←	
499	E07	V_{DD}	←	←	←	
500	E06	IC	←	←	←	
501	F06	GND	←	←	←	
502	G06	AD23	←	←	←	I/O
503	H06	GND	←	←	←	
504	J06	AD13	←	←	←	I/O
505	K06	GND	←	←	←	
506	L06	AD03	←	←	←	I/O
507	M06	GND	←	←	←	
508	N06	V_{DD}	←	←	←	
509	P06	GND	←	←	←	
510	R06	GND	←	←	←	
511	T06	GND	←	←	←	
512	U06	GND	←	←	←	
513	V06	HTD27	←	←	←	I/O
514	W06	GND	←	←	←	
515	Y06	HTD18	←	←	←	I/O
516	AA06	GND	←	←	←	
517	AB06	HTD09	←	←	←	I/O
518	AC06	GND	←	←	←	
519	AD06	V_{DD}	←	←	←	
520	AE06	GND	←	←	←	

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Pin No.	Address	12-PHY Polling Mode/ 15-PHY Polling Mode	Multiplexed Status Polling Mode	2-Group Weighted Polling Mode	1-Group Weighted Polling Mode	I/O
521	AE07	V_{DD}	←	←	←	
522	AE08	GND	←	←	←	
523	AE09	RXDATA304	RXDATA112	RXDATA112	RXDATA112	I
524	AE10	GND	←	←	←	
525	AE11	RXADDR33	IC	RXADDR1B3	IC	O
526	AE12	GND	←	←	←	
527	AE13	GND	←	←	←	
528	AE14	GND	←	←	←	
529	AE15	GND	←	←	←	
530	AE16	GND	←	←	←	
531	AE17	GND	←	←	←	
532	AE18	CG	RXCLAV1[1]	CG	CG	I
533	AE19	GND	←	←	←	
534	AE20	CG	TXCLAV1[1]	CG	CG	I
535	AE21	GND	←	←	←	
536	AE22	TXDATA100	TXDATA100	TXDATA100	TXDATA100	O
537	AE23	GND	←	←	←	
538	AE24	CBD78	←	←	←	I/O
539	AE25	GND	←	←	←	
540	AD25	CBD71	←	←	←	I/O
541	AC25	GND	←	←	←	
542	AB25	CBD61	←	←	←	I/O
543	AA25	GND	←	←	←	
544	Y25	CBD51	←	←	←	I/O
545	W25	GND	←	←	←	
546	V25	GND	←	←	←	
547	U25	GND	←	←	←	
548	T25	GND	←	←	←	
549	R25	GND	←	←	←	
550	P25	GND	←	←	←	
551	N25	CBD42	←	←	←	I/O
552	M25	GND	←	←	←	
553	L25	CBD32	←	←	←	I/O
554	K25	GND	←	←	←	
555	J25	CBD22	←	←	←	I/O
556	H25	GND	←	←	←	
557	G25	CBD12	←	←	←	I/O
558	F25	GND	←	←	←	
559	F24	CBD04	←	←	←	I/O
560	F23	GND	←	←	←	

(15/15)

Pin No.	Address	12-PHY Polling Mode/ 15-PHY Polling Mode	Multiplexed Status Polling Mode	2-Group Weighted Polling Mode	1-Group Weighted Polling Mode	I/O
561	F22	RXDATA002	RXDATA002	RXDATA002	RXDATA002	I
562	F21	GND	←	←	←	
563	F20	RXADDR01	RXADDR01	RXADDR0A1	RXADDR01	O
564	F19	GND	←	←	←	
565	F18	GND	←	←	←	
566	F17	GND	←	←	←	
567	F16	GND	←	←	←	
568	F15	RXDATA203	RXDATA011	RXDATA011	RXDATA011	I
569	F14	GND	←	←	←	
570	F13	V_{DD}	←	←	←	
571	F12	GND	←	←	←	
572	F11	TXDATA207	TXDATA015	TXDATA015	TXDATA015	O
573	F10	GND	←	←	←	
574	F09	MCS_B	←	←	←	I
575	F08	GND	←	←	←	
576	F07	GND	←	←	←	

CONTENTS

1. PIN FUNCTIONS

Although the μPD98412 is a device operating at 3.3 V, it can be directly connected to a PHY device, CPU, and memory with a 5-V TTL interface.

1.1 Power Supply

Table 1-1. Power Supply

Pin Name	Pin No.	I/O	Function
V_{DD}	20, 25, 31, 35, 39, 43, 57, 61, 64, 67, 72, 78, 81, 86, 87, 89, 94, 96, 112, 119, 129, 147, 152, 160, 161, 169, 230, 232, 240, 243, 283, 290, 293, 308, 315, 324, 325, 329, 332, 337, 342, 353, 360, 371, 376, 383, 393, 398, 406, 417, 418, 420, 422, 424, 426, 427, 429, 431, 433, 435, 436, 438, 441, 443, 445 - 448, 450, 452 - 456, 458, 459, 461, 462, 464, 466 - 469, 471, 473, 475 - 477, 480 - 483, 485, 487 - 490, 492, 494 - 496, 498, 499, 508, 519, 521, 570	—	These pins supply a power of +3.3 V ± 5%.
GND	2, 6, 9, 14, 26, 32, 37, 58, 60, 84, 101, 110, 113, 143, 144, 156, 162, 173, 183, 196, 215, 233, 241, 244, 255, 256, 265, 280, 282, 291, 304, 305, 307, 313, 314, 323, 327, 330, 339, 341, 352, 364, 365, 367, 368, 370, 375, 378, 385, 387, 388, 390, 394, 396, 401, 410, 413, 425, 434, 440, 444, 460, 479, 501, 503, 505, 507, 509 - 512, 514, 516, 518, 520, 522, 524, 526 - 531, 533, 535, 537, 539, 541, 543, 545 - 550, 552, 554, 556, 558, 560, 562, 564 - 567, 569, 571, 573, 575, 576	—	These are ground pins.

1.2 UTOPIA Interface

The μPD98412 employs a UTOPIA Level2 (cell level transfer) interface between PHY layer and ATM layer. Symbol, pim number, and function are varied depending on the polling mode.

(1) 8-bit 12-PHY polling mode/15-PHY polling mode

Table 1-2. Receive Interface Signals (1/2)

Symbol	Pin No.	I/O	Function
RXADDR03 - RXADDR00	205, 206, 563, 486	O	Multi-PHY select address of receive interface 0. RXADDR03 is the MSB.
RXDATA007 - RXDATA000	303, 397, 92, 202, 93, 561, 484, 203	I	Cell data input of receive interface 0. Cell data is input from a PHY layer device in byte units. The μPD98412 reads the data at the rising edge of UCLK0. RXDATA007 is the MSB.
RXSOC0	306	I	Cell transfer start signal of receive interface 0. This signal is input from a PHY layer device in synchronization with the first byte of cell data.
RXENB0_B	204	O	Transfer enable signal of receive interface 0. This signal informs a PHY layer device that the μPD98412 is ready for reception in the next clock cycle.
RXCLAV0	95	I	Cell transfer enable signal of receive interface 0. This pin inputs a signal that indicates that no more cells will be supplied to the μPD98412 after the current cell has been transferred.
UCLK0	399	I	UTOPIA clock input of receive interface 0. Data is transferred/received at the rising edge of this clock.
RXADDR13 - RXADDR10	266, 50, 363, 267	O	Multi-PHY select address of receive interface 1. RXADDR13 is the MSB.
RXDATA107 - RXDATA100	158, 263, 449, 46, 159, 264, 361, 47	I	Cell data input of receive interface 1. Cell data is input from a PHY layer device in byte units. The μPD98412 reads the data at the rising edge of UCLK1. RXDATA107 is the MSB.
RXSOC1	451	I	Cell transfer start signal of receive interface 1. This signal is input from a PHY layer device in synchronization with the first byte of cell data.
RXENB1_B	362	O	Transfer enable signal of receive interface 1. This signal informs a PHY layer device that the μPD98412 is ready for reception in the next clock cycle.
RXCLAV1	49	I	Cell transfer enable signal of receive interface 1. This pin inputs a signal that indicates that no more cells will be supplied to the μPD98412 after the current cell has been transferred.
UCLK1	48	I	UTOPIA clock input of receive interface 1. Data is transferred/received at the rising edge of this clock.

Table 1-2. Receive Interface Signals (2/2)

Symbol	Pin No.	I/O	Function
RXADDR23 - RXADDR20	408, 493, 107, 316	O	Multi-PHY select address of receive interface 2. RXADDR23 is the MSB.
RXDATA207 - RXDATA200	405, 312, 103, 212, 568, 491, 104, 213	I	Cell data input of receive interface 2. Cell data is input from a PHY layer device in byte units. The μPD98412 reads the data at the rising edge of UCLK2. RXDATA207 is the MSB.
RXSOC2	214	I	Cell transfer start signal of receive interface 2. This signal is input from a PHY layer device in synchronization with the first byte of cell data.
RXENB2_B	105	O	Transfer enable signal of receive interface 2. This signal informs a PHY layer device that the μPD98412 is ready for reception in the next clock cycle.
RXCLAV2	106	I	Cell transfer enable signal of receive interface 2. This pin inputs a signal that indicates that no more cells will be supplied to the μPD98412 after the current cell has been transferred.
UCLK2	407	I	UTOPIA clock input of receive interface 2. Data is transferred/received at the rising edge of this clock.
RXADDR33 - RXADDR30	525, 355, 258, 153	O	Multi-PHY select address of receive interface 3. RXADDR33 is the MSB.
RXDATA307 - RXDATA300	34, 148, 254, 523, 442, 149, 36, 150	I	Cell data input of receive interface 3. Cell data is input from a PHY layer device in byte units. The μPD98412 reads the data at the rising edge of UCLK3. RXDATA307 is the MSB.
RXSOC3	257	I	Cell transfer start signal of receive interface 3. This signal is input from a PHY layer device in synchronization with the first byte of cell data.
RXENB3_B	151	O	Transfer enable signal of receive interface 3. This signal informs a PHY layer device that the μPD98412 is ready for reception in the next clock cycle.
RXCLAV3	38	I	Cell transfer enable signal of receive interface 3. This pin inputs a signal that indicates that no more cells will be supplied to the μPD98412 after the current cell has been transferred.
UCLK3	354	I	UTOPIA clock input of receive interface 3. Data is transferred/received at the rising edge of this clock.

Table 1-3. Transmit Interface Signals (1/2)

Symbol	Pin No.	I/O	Function
TXADDR03 - TXADDR00	97, 207, 98, 402	O	Multi-PHY select address of transmit interface 0. TXADDR03 is the MSB.
TXDATA007 - TXDATA000	310, 209, 100, 404, 311, 210, 102, 211	O	Cell data output of transmit interface 0. Cell data is output to a PHY layer device in byte units. The μPD98412 outputs the data at the rising edge of UCLK0. TXDATA007 is the MSB. (3-state buffer)
TXSOC0	99	O	Cell transfer start signal of transmit interface 0. This signal is output to a PHY layer device in synchronization with the first byte of cell data. (3-state buffer)
TXENB0_B	403	O	Transfer enable signal of transmit interface 0. This signal informs a PHY layer device that the μPD98412 outputs data in the current clock cycle.
TXCLAV0	208	I	Cell transfer enable signal of transmit interface 0. This pin inputs a signal that indicates that the μPD98412 is ready to receive the next cell after transfer of the current cell is completed.
TXADDR13 - TXADDR10	163, 51, 268, 164	O	Multi-PHY select address of transmit interface 1. TXADDR13 is the MSB.
TXDATA107 - TXDATA100	53, 366, 270, 166, 54, 271, 167, 536	O	Cell data output of transmit interface 1. The μPD98412 outputs the data at the rising edge of UCLK1. TXDATA107 is the MSB. (3-state buffer)
TXSOC1	269	O	Cell transfer start signal of transmit interface 1. This signal is output to a PHY layer device in synchronization with the first byte of cell data. (3-state buffer)
TXENB1_B	165	O	Transfer enable signal of transmit interface 1. This signal informs a PHY layer device that the μPD98412 outputs data in the current clock cycle.
TXCLAV1	52	I	Cell transfer enable signal of transmit interface 1. This pin inputs a signal that indicates that the μPD98412 is ready to receive the next cell after transfer of the current cell is completed.

Table 1-3. Transmit Interface Signals (2/2)

Symbol	Pin No.	I/O	Function
TXADDR23 - TXADDR20	216, 108, 409, 317	O	Multi-PHY select address of transmit interface 2. TXADDR23 is the MSB.
TXDATA207 - TXDATA200	572, 411, 319, 219, 111, 412, 320, 220	O	Cell data output of transmit interface 2. The μPD98412 outputs the data at the rising edge of UCLK2. TXDATA207 is the MSB. (3-state buffer)
TXSOC2	318	O	Cell transfer start signal of transmit interface 2. This signal is output to a PHY layer device in synchronization with the first byte of cell data. (3-state buffer)
TXENB2_B	218	O	Transfer enable signal of transmit interface 2. This signal informs a PHY layer device that the μPD98412 outputs data in the current clock cycle.
TXCLAV2	109	I	Cell transfer enable signal of transmit interface 2. This pin inputs a signal that indicates that the μPD98412 is ready to receive the next cell after transfer of the current cell is completed.
TXADDR33 - TXADDR30	40, 356, 259, 154	O	Multi-PHY select address of transmit interface 3. TXADDR33 is the MSB.
TXDATA307 - TXDATA300	42, 358, 261, 44, 157, 359, 262, 45	O	Cell data output of transmit interface 3. The μPD98412 outputs the data at the rising edge. TXDATA307 is the MSB. (3-state buffer)
TXSOC3	260	O	Cell transfer start signal of transmit interface 3. This signal is output to a PHY layer device in synchronization with the first byte of cell data. (3-state buffer)
TXENB3_B	155	O	Transfer enable signal of transmit interface 3. This signal informs a PHY layer device that the μPD98412 outputs data in the current clock cycle.
TXCLAV3	357	I	Cell transfer enable signal of transmit interface 3. This pin inputs a signal that indicates that the μPD98412 is ready to receive the next cell after transfer of the current cell is completed.

(2) 16-bit multiplexed status polling mode

Table 1-4. Receive Interface Signals

Symbol	Pin No.	I/O	Function
RXADDR04 - RXADDR00	316, 205, 206, 563, 486	O	Multi-PHY select address of receive interface 0. RXADDR04 is the MSB.
RXDATA015 - RXDATA000	405, 312, 103, 212, 568, 491, 104, 213, 303, 397, 92, 202, 93, 561, 484, 203	I	Cell data input of receive interface 0. Cell data is input from a PHY layer device in 16-bit units. The μPD98412 reads the data at the rising edge of UCLK0. RXDATA015 is the MSB.
RXSOC0	306	I	Cell transfer start signal of receive interface 0. This signal is input from a PHY layer device in synchronization with the first byte of cell data.
RXENB0_B	204	O	Transfer enable signal of receive interface 0. This signal informs a PHY layer device that the μPD98412 is ready for reception in the next clock cycle.
RXCLAV0[0] - RXCLAV0[3]	95, 400, 106, 214	I	Cell transfer enable signal of receive interface 0. This pin inputs a signal that indicates that no more cells will be supplied to the μPD98412. Pins to be connected (RXCLAV0[0]-[3]) differ depending on PHY address of the connected PHY device.
UCLK0	399	I	UTOPIA clock input of receive interface 0. Data is transferred/received at the rising edge of this clock.
RXADDR14 - RXADDR10	153, 266, 50, 363, 267	O	Multi-PHY select address of receive interface 1. RXADDR14 is the MSB.
RXDATA115 - RXDATA100	34, 148, 254, 523, 442, 149, 36, 150, 158, 263, 449, 46, 159, 264, 361, 47	I	Cell data input of receive interface 1. Cell data is input from a PHY layer device in 16-bit units. The μPD98412 reads the data at the rising edge of UCLK1. RXDATA115 is the MSB.
RXSOC1	451	I	Cell transfer start signal of receive interface 1. This signal is input from a PHY layer device in synchronization with the first byte of cell data.
RXENB1_B	362	O	Transfer enable signal of receive interface 1. This signal informs a PHY layer device that the μPD98412 is ready for reception in the next clock cycle.
RXCLAV1[0] - RXCLAV1[3]	49, 532, 38, 257	I	Cell transfer enable signal of receive interface 1. This pin inputs a signal that indicates that no more cells will be supplied to the μPD98412 after the current cell has been transferred. Pins to be connected (RXCLAV1[0]-[3]) differ depending on PHY address of the connected PHY device.
UCLK1	48	I	UTOPIA clock input of receive interface 1. Data is transferred/received at the rising edge of this clock.

Table 1-5. Transmit Interface Signals

Symbol	Pin No.	I/O	Function
TXADDR04 - TXADDR00	317, 97, 207, 98, 402	O	Multi-PHY select address of transmit interface 0. TXADDR04 is the MSB.
TXDATA015 - TXDATA000	572, 411, 319, 219, 111, 412, 320, 220, 310, 209, 100, 404, 311, 210, 102, 211	O	Cell data output of transmit interface 0. Cell data is output to a PHY layer device in 16-bit units. The μPD98412 outputs the data at the rising edge of UCLK0. TXDATA015 is the MSB. (3-state buffer)
TXSOC0	99	O	Cell transfer start signal of transmit interface 0. This signal is output to a PHY layer device in synchronization with the first byte of cell data. (3-state buffer)
TXENB0_B	403	O	Transfer enable signal of transmit interface 0. This signal informs a PHY layer device that the μPD98412 outputs data in the current clock cycle.
TXCLAV0[0] - TXCLAV0[3]	208, 309, 109, 217	I	Cell transfer enable signal of transmit interface 0. This pin inputs a signal that indicates that the μPD98412 is ready to receive the next cell after transfer of the current cell is completed. Pins to be connected (TXCLAV0[0]-[3]) differ depending on PHY address of the connected PHY device.
TXADDR14 - TXADDR10	154, 163, 51, 268, 164	O	Multi-PHY select address of transmit interface 1. TXADDR14 is the MSB.
TXDATA115 - TXDATA100	42, 358, 261, 44, 157, 359, 262, 45, 53, 366, 270, 166, 54, 271, 167, 536	O	Cell data output of transmit interface 1. The μPD98412 outputs the data at the rising edge of UCLK1. TXDATA115 is the MSB. (3-state buffer)
TXSOC1	269	O	Cell transfer start signal of transmit interface 1. This signal is output to a PHY layer device in synchronization with the first byte of cell data. (3-state buffer)
TXENB1_B	165	O	Transfer enable signal of transmit interface 1. This signal informs a PHY layer device that the μPD98412 outputs data in the current clock cycle.
TXCLAV1[0] - TXCLAV1[3]	52, 534, 357, 41	I	Cell transfer enable signal of transmit interface 1. This pin inputs a signal that indicates that the μPD98412 is ready to receive the next cell after transfer of the current cell is completed. Pins to be connected (TXCLAV1[0]-[3]) differ depending on PHY address of the connected PHY device.

(3) 16-bit 2-group weighted polling mode

Table 1-6. Receive Interface Signals (1/2)

Symbol	Pin No.	I/O	Function
RXADDR0A3 - RXADDR0A0	205, 206, 563, 486	O	Multi-PHY select address of receive interface 0, group A. RXADDR0A3 is the MSB.
RXADDR0B3 - RXADDR0B0	408, 493, 107, 316	O	Multi-PHY select address of receive interface 0, group B. RXADDR0B3 is the MSB.
RXENB0A_B	204	O	Transfer enable signal of receive interface 0, group A. This signal informs a PHY layer device that the μPD98412 is ready for reception in the next clock cycle.
RXENB0B_B	105	O	Transfer enable signal of receive interface 0, group B. This signal informs a PHY layer device that the μPD98412 is ready for reception in the next clock cycle.
RXCLAV0A	95	I	Cell transfer enable signal of receive interface 0, group A. This pin inputs a signal that indicates that no more cells will be supplied to the μPD98412 after the current cell has been transferred.
RXCLAV0B	106	I	Cell transfer enable signal of receive interface 0, group B. This pin inputs a signal that indicates that no more cells will be supplied to the μPD98412 after the current cell has been transferred.
RXDATA015 - RXDATA000	405, 312, 103, 212, 568, 491, 104, 213, 303, 397, 92, 202, 93, 561, 484, 203	I	Cell data input of receive interface 0. Cell data is input from a PHY layer device in 16-bit units. The μPD98412 reads the data at the rising edge of UCLK0. RXDATA015 is the MSB.
RXSOC0	306	I	Cell transfer start signal of receive interface 0. This signal is input from a PHY layer device in synchronization with the first byte of cell data.
UCLK0	399	I	UTOPIA clock input of receive interface 0. Data is transferred/received at the rising edge of this clock.

Table 1-6. Receive Interface Signals (2/2)

Symbol	Pin No.	I/O	Function
RXADDR1A3 - RXADDR1A0	266, 50, 363, 267	O	Multi-PHY select address of receive interface 1, group A. RXADDR1A3 is the MSB.
RXADDR1B3 - RXADDR1B0	525, 355, 258, 153	O	Multi-PHY select address of receive interface 1, group B. RXADDR1B3 is the MSB.
RXENB1A_B	362	O	Transfer enable signal of receive interface 1, group A. This signal informs a PHY layer device that the μPD98412 is ready for reception in the next clock cycle.
RXENB1B_B	151	O	Transfer enable signal of receive interface 1, group B. This signal informs a PHY layer device that the μPD98412 is ready for reception in the next clock cycle.
RXCLAV1A	49	I	Cell transfer enable signal of receive interface 1, group A. This pin inputs a signal that indicates that no more cells will be supplied to the μPD98412 after the current cell has been transferred.
RXCLAV1B	38	I	Cell transfer enable signal of receive interface 1, group B. This pin inputs a signal that indicates that no more cells will be supplied to the μPD98412 after the current cell has been transferred.
RXDATA115 - RXDATA100	34, 148, 254, 523, 442, 149, 36, 150, 158, 263, 449, 46, 159, 264, 361, 47	I	Cell data input of receive interface 1. Cell data is input from a PHY layer device in 16-bit units. The μPD98412 reads the data at the rising edge of UCLK1. RXDATA115 is the MSB.
RXSOC1	451	I	Cell transfer start signal of receive interface 1. This signal is input from a PHY layer device in synchronization with the first byte of cell data.
UCLK1	48	I	UTOPIA clock input of receive interface 1. Data is transferred/received at the rising edge of this clock.

Table 1-7. Transmit Interface Signals (1/2)

Symbol	Pin No.	I/O	Function
TXADDR0A3 - TXADDR0A0	97, 207, 98, 402	O	Multi-PHY select address of transmit interface 0, group A. TXADDR0A3 is the MSB.
TXADDR0B3 - TXADDR0B0	216, 108, 409, 317	O	Multi-PHY select address of transmit interface 0, group B. TXADDR0B3 is the MSB.
TXENB0A_B	403	O	Transfer enable signal of transmit interface 0, group A. This signal informs a PHY layer device that the μPD98412 outputs data in the current clock cycle.
TXENB0B_B	218	O	Transfer enable signal of transmit interface 0, group B. This signal informs a PHY layer device that the μPD98412 outputs data in the current clock cycle.
TXCLAV0A	208	I	Cell transfer enable signal of transmit interface 0, group A. This pin inputs a signal that indicates that the μPD98412 is ready to receive the next cell after transfer of the current cell is completed.
TXCLAV0B	109	I	Cell transfer enable signal of transmit interface 0, group B. This pin inputs a signal that indicates that the μPD98412 is ready to receive the next cell after transfer of the current cell is completed.
TXDATA015 - TXDATA000	572, 411, 319, 219, 111, 412, 320, 220, 310, 209, 100, 404, 311, 210, 102, 211	O	Cell data output of transmit interface 0. Cell data is output to a PHY layer device in 16-bit units. The μPD98412 outputs the data at the rising edge of UCLK0. TXDATA015 is the MSB. (3-state buffer)
TXSOC0	99	O	Cell transfer start signal of transmit interface 0. This signal is output to a PHY layer device in synchronization with the first byte of cell data. (3-state buffer)

Table 1-7. Transmit Interface Signals (2/2)

Symbol	Pin No.	I/O	Function
TXADDR1A3 - TXADDR1A0	163, 51, 268, 164	O	Multi-PHY select address of transmit interface 1, group A. TXADDR1A3 is the MSB.
TXADDR1B3 - TXADDR1B0	40, 356, 259, 154	O	Multi-PHY select address of transmit interface 1, group B. TXADDR1B3 is the MSB.
TXENB1A_B	165	O	Transfer enable signal of transmit interface 1, group A. This signal informs a PHY layer device that the μPD98412 outputs data in the current clock cycle.
TXENB1B_B	155	O	Transfer enable signal of transmit interface 1, group B. This signal informs a PHY layer device that the μPD98412 outputs data in the current clock cycle.
TXCLAV1A	52	I	Cell transfer enable signal of transmit interface 1, group A. This pin inputs a signal that indicates that the μPD98412 is ready to receive the next cell after transfer of the current cell is completed.
TXCLAV1B	357	I	Cell transfer enable signal of transmit interface 1, group B. This pin inputs a signal that indicates that the μPD98412 is ready to receive the next cell after transfer of the current cell is completed.
TXDATA115 - TXDATA100	42, 358, 261, 44, 157, 359, 262, 45, 53, 366, 270, 166, 54, 271, 167, 536	O	Cell data output of transmit interface 1. Cell data is output to a PHY layer device in 16-bit units. The μPD98412 outputs the data at the rising edge of UCLK1. TXDATA115 is the MSB. (3-state buffer)
TXSOC1	269	O	Cell transfer start signal of transmit interface 1. This signal is output to a PHY layer device in synchronization with the first byte of cell data. (3-state buffer)

(4) 16-bit 1-group weighted polling mode

Table 1-8. Receive Interface Signals

Symbol	Pin No.	I/O	Function
RXADDR04 - RXADDR00	316, 205, 206, 563, 486	O	Multi-PHY select address of receive interface 0. RXADDR04 is the MSB.
RXDATA015 - RXDATA000	405, 312, 103, 212, 568, 491, 104, 213, 303, 397, 92, 202, 93, 561, 484, 203	I	Cell data input of receive interface 0. Cell data is input from a PHY layer device in 16-bit units. The μPD98412 reads the data at the rising edge of UCLK0. RXDATA015 is the MSB.
RXSOC0	306	I	Cell transfer start signal of receive interface 0. This signal is input from a PHY layer device in synchronization with the first byte of cell data.
RXENB0_B	204	O	Transfer enable signal of receive interface 0. This signal informs a PHY layer device that the μPD98412 is ready for reception in the next clock cycle.
RXCLAV0	95	I	Cell transfer enable signal of receive interface 0. This pin inputs a signal that indicates that no more cells will be supplied to the μPD98412 after the current cell has been transferred.
UCLK0	399	I	UTOPIA clock input of receive interface 0. Data is transferred/received at the rising edge of this clock.
RXADDR14 - RXADDR10	153, 266, 50, 363, 267	O	Multi-PHY select address of receive interface 1. RXADDR14 is the MSB.
RXDATA115 - RXDATA100	34, 148, 254, 523, 442, 149, 36, 150, 158, 263, 449, 46, 159, 264, 361, 47	I	Cell data input of receive interface 1. Cell data is input from a PHY layer device in 16-bit units. The μPD98412 reads the data at the rising edge of UCLK1. RXDATA115 is the MSB.
RXSOC1	451	I	Cell transfer start signal of receive interface 1. This signal is input from a PHY layer device in synchronization with the first byte of cell data.
RXENB1_B	362	O	Transfer enable signal of receive interface 1. This signal informs a PHY layer device that the μPD98412 is ready for reception in the next clock cycle.
RXCLAV1	49	I	Cell transfer enable signal of receive interface 1. This pin inputs a signal that indicates that no more cells will be supplied to the μPD98412 after the current cell has been transferred.
UCLK1	48	I	UTOPIA clock input of receive interface 1. Data is transferred/received at the rising edge of this clock.

Table 1-9. Transmit Interface Signals

Symbol	Pin No.	I/O	Function
TXADDR04 - TXADDR00	317, 97, 207, 98, 402	O	Multi-PHY select address of transmit interface 0. TXADDR04 is the MSB.
TXDATA015 - TXDATA000	572, 411, 319, 219, 111, 412, 320, 220, 310, 209, 100, 404, 311, 210, 102, 211	O	Cell data output of transmit interface 0. Cell data is output to a PHY layer device in 16-bit units. The μPD98412 outputs the data at the rising edge of UCLK0. TXDATA015 is the MSB. (3-state buffer)
TXSOC0	99	O	Cell transfer start signal of transmit interface 0. This signal is output to a PHY layer device in synchronization with the first byte of cell data. (3-state buffer)
TXENB0_B	403	O	Transfer enable signal of transmit interface 0. This signal informs a PHY layer device that the μPD98412 outputs data in the current clock cycle.
TXCLAV0	208	I	Cell transfer enable signal of transmit interface 0. This pin inputs a signal that indicates that the μPD98412 is ready to receive the next cell after transfer of the current cell is completed.
TXADDR14 - TXADDR10	154, 163, 51, 268, 164	O	Multi-PHY select address of transmit interface 1. TXADDR14 is the MSB.
TXDATA115 - TXDATA100	42, 358, 261, 44, 157, 359, 262, 45, 53, 366, 270, 166, 54, 271, 167, 536	O	Cell data output of transmit interface 1. The μPD98412 outputs the data at the rising edge of UCLK1. TXDATA115 is the MSB. (3-state buffer)
TXSOC1	269	O	Cell transfer start signal of transmit interface 1. This signal is output to a PHY layer device in synchronization with the first byte of cell data. (3-state buffer)
TXENB1_B	165	O	Transfer enable signal of transmit interface 1. This signal informs a PHY layer device that the μPD98412 outputs data in the current clock cycle.
TXCLAV1	52	I	Cell transfer enable signal of transmit interface 1. This pin inputs a signal that indicates that the μPD98412 is ready to receive the next cell after transfer of the current cell is completed.

1.3 Memory Interface Signals

The μPD98412 has two types of memory interfaces. One of them is used to store a cell header translation table and an address pointer to the cell buffer to the HTT & control memory, and the other is used to store cell data to the cell buffer memory. Table 1-10 shows the interface signals of the HTT & control memory. Table 1-11 shows the interface signals of the cell buffer memory.

Table 1-10. HTT & Control Memory Interface Signals

Symbol	Pin No.	I/O	Function
HTA17 - HTA00	11, 333, 234, 127, 12, 334, 235, 128, 13, 335, 236, 15, 130, 336, 237, 16, 131, 238	O	Address output
HTD31 - HTD00	18, 133, 19, 430, 513, 134, 135, 21, 242, 136, 22, 137, 432, 515, 23, 138, 343, 245, 139, 344, 246, 140, 517, 345, 141, 27, 28, 346, 248, 142, 29, 249	I/O	Data I/O bus (32-bit/word units) (w/pull-down resistor)
HTP3 - HTP0	338, 340, 24, 247	I/O	Parity I/O (w/pull-down resistor)
HTCS1_B, HTCS0_B	428, 17	O	Chip select signal
HTWE_B	132	O	Write enable signal
HTOE_B	239	O	Output enable signal

Table 1-11. Cell Buffer Memory Interface Signals

Symbol	Pin No.	I/O	Function
CBA17 - CBA00	71, 381, 286, 73, 184, 382, 287, 74, 185, 288, 470, 75, 186, 289, 384, 76, 187, 77	O	Address output
★ CBD91 - CBD00	145, 251, 349, 439, 55, 272, 168, 56, 457, 369, 273, 170, 274, 538, 59, 171, 275, 172, 276, 372, 540, 373, 277, 62, 174, 278, 374, 63, 175, 279, 542, 463, 176, 65, 177, 281, 377, 66, 178, 179, 544, 465, 68, 180, 69, 379, 284, 181, 472, 551, 188, 189, 79, 386, 292, 190, 80, 191, 474, 553, 294, 192, 82, 389, 295, 193, 83, 296, 194, 555, 391, 297, 195, 85, 478, 392, 298, 197, 299, 557, 88, 198, 300, 199, 301, 395, 90, 559, 302, 200, 91, 201	I/O	Data bus (92-bit/word units) (w/pull-down resistor)
CBCS1_B, CBCS0_B	70, 380	O	Chip select signal
CBWE_B	285	O	Write enable signal
CBOE_B	182	O	Output enable signal

1.4 Microprocessor Interface Signals

The μPD98412 supports a 32-bit address/data multiplexed synchronous bus type microprocessor interface.

Table 1-12. Microprocessor Interface Signal

Symbol	Pin No.	I/O	Function
IOCS_B	221	I	I/O chip select signal
MCS_B	574	I	Memory chip select signal
INT	414	O	Interrupt request signal
HCLK	497	I	Microprocessor bus clock (8 to 33 MHz)
AD31 - AD0	416, 1, 117, 225, 118, 226, 326, 3, 502, 227, 419, 4, 120, 228, 328, 5, 121, 229, 504, 421, 122, 7, 123, 231, 331, 8, 124, 125, 506, 423, 10, 126	I/O	Address/data bus
R/W_B	114	I	Read/write select signal
UWE_B	115	I	High-order word enable signal
RDY_B	322	O	Ready signal (3-state buffer)

1.5 JTAG

Table 1-13. JTAG Interface Signals

Symbol	Pin No.	I/O	Function
JDI	252	I	JTAG serial data input
JDO	146	O	JTAG serial data output (normally open) (3-state buffer)
JCK	33	I	JTAG serial clock input
JMS	253	I	JTAG mode select signal
JRST_B	351	I	JTAG reset signal

1.6 Others

Table 1-14. Other Interface Signals

Symbol	Pin No.	I/O	Function
SWCLK	437	I	System clock input (8 to 40 MHz)
RESET_B	347	I	Hardware reset signal (Schmitt input buffer)
CG	116, 222, 223, 321, 415	I	Always connect to GND.
PU	30	I	Always pull up to V_{DD}.
IC	224, 250, 348, 350, 500	O	Internally connected (always open).

1.7 Recommended Connections of Unused Pins

Table 1-15. Recommended Connections of Unused Pins

Pin Name	I/O	Recommended Connections
RXDATA***	I	Connect to GND.
RXSOC*	I	Connect to GND.
RXCLAV*	I	Connect to GND.
UCLK*	I	Connect to GND.
TXCLAV*	I	Connect to GND.
HTD31 - HTD00	I/O (w/pull-down resistor)	Open.
HTP3 - HTP0	I/O (w/pull-down resistor)	Open.
CBD91 - CBD00	I/O (w/pull-down resistor)	Open.
IOCS_B	I	Pull up to V_{DD}.
MCS_B	I	Pull up to V_{DD}.
AD31 - AD00	I/O	Pull up to V_{DD}.
R/W_B	I	Pull up to V_{DD}.
UWE_B	I	Pull up to V_{DD}.
JDI	I	Connect to GND.
JCK	I	Connect to GND.
JMS	I	Connect to GND.
JRST_B	I	Connect to GND.
All output pins	O	Open.

1.8 Pin Status at Reset

Table 1-16. Pin Status at Reset

Pin Name	I/O	Pin Status at Reset
RXADDR*	O	High level
RXENB*_B	O	High level
TXADDR*	O	High level
TXDATA***	O (3-state buffer)	Hi-Z
TXSOC*	O (3-state buffer)	Hi-Z
TXENB*_B	O	High level
HTA17 - HTA00	O	Low level
HTCS1_B, HTCS0_B	O	High level
HTWE_B	O	High level
HTOE_B	O	High level
HTP3 - HTP0	I/O (w/pull-down resistor)	Low level
HTD31 - HTD00	I/O (w/pull-down resistor)	Low level
CBD91 - CBD00	I/O (w/pull-down resistor)	Low level
CBA17 - CBA00	O	Low level
CBOE_B	O	High level
CBWE_B	O	High level
CBCS1_B, CBCS0_B	O	High level
INT	O	Low level
RDY_B	O (3-state buffer)	Hi-Z
AD31 - AD00	I/O	Hi-Z
JDO	O (3-state buffer)	Hi-Z

2. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Test Conditions	Rating	Unit
Supply voltage	V_{DD}		–0.5 to +4.6	V
Input voltage	V_I	$V_I < V_{DD}$ + 3.0 V	–0.5 to +6.6	V
Output voltage	V_O	$V_O < V_{DD}$ + 3.0 V	–0.5 to +6.6	V
Storage temperature	T_{stg}		–65 to +150	°C

Caution If any of the parameters exceeds the absolute maximum ratings, even momentarily, the quality of the product may be impaired. The absolute maximum ratings are values that may physically damage the product(s). Be sure to use the product(s) within the ratings.

Capacitance

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	Frequency = 1 MHz	–	10	20	pF
Output capacitance	C_O	Frequency = 1 MHz	–	10	20	pF
Input/output capacitance	C_{IO}	Frequency = 1 MHz	–	10	20	pF

Recommended Operating Condition

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}		3.135	3.300	3.465	V
Low-level input voltage	V_{IL}	Other than RESET_B signal	0	–	0.8	V
High-level input voltage	V_{IH}	Other than RESET_B signal	2.0	–	5.5	V
Negative trigger voltage	V_N	RESET_B signal	0.6		1.8	V
Positive trigger voltage	V_P	RESET_B signal	1.2		2.4	V
★ Hysteresis voltage	V_H		0.3		1.5	V
Operating temperature	T_A		–40	–	+85	°C

DC Characteristics (T_A = –40 to +85 °C, V_{DD} = 3.3 V ±5%)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Output leakage current	I_{OZ}	$V_O = V_{DD}$ or GND	–	–	±10	μA
Input leakage current	I_{LI1}	$V_I = V_{DD}$ or GND, **Note 1**	–	–	±10	μA
	I_{LI2}	$V_I = V_{DD}$ **Note 2** (50 kΩ pull-down)	25	120	220	μA
Low-level output leakage current	I_{OL1}	V_{OL} = 0.4 V, **Note 3**	6.0	–	–	mA
	I_{OL2}	V_{OL} = 0.4 V, **Note 4, 5**	9.0	–	–	mA
	I_{OL3}	V_{OL} = 0.4 V, **Note 6**	12.0	–	–	mA
High-level output leakage current	I_{OH1}	V_{OH} = 2.4 V, **Note 3**	–3.0	–	–	mA
	I_{OH2}	V_{OH} = 2.4 V, **Note 4**	–4.0	–	–	mA
	I_{OH2}	V_{OH} = 2.4 V, **Note 5** (UTOPIA)	–6.0	–	–	mA
	I_{OH3}	V_{OH} = 2.4 V, **Note 6**	–5.0	–	–	mA
Low-level output leakage voltage	V_{OL}	I_{OL} = 0 mA	–	–	0.1	V
High-level output leakage voltage	V_{OH1}	I_{OH} = 0 mA, **Note 7**	V_{DD} – 0.2	–	–	V
	V_{OH2}	I_{OH} = 0 mA, **Note 8**	V_{DD} – 0.4	–	–	V
★ Operating current	I_{DD}	$V_I = V_{DD}$ or GND	–	**Note 9**	1300	mA

Notes 1. RXDATA***, RXSOC*, RXCLAV*, UCLK*, TCLAV*, AD31-AD00, MCS_B, IOCS_B, R/W_B, UWE_B, HCLK, JDI, JCK, JMS, JRST_B, SWCLK, RESET_B pins

2. HTD31-HTD00, HTP3-HTP0, CBD91-CBD00 pins

3. INT, JDO pins

4. HTA17-HTA00, HTWE_B, HTOE_B, CBA17-CBA00, CBCS0_B, CBWE_B, CBOE_B, HTCS1_B, HTCS0_B, CBCS1_B, HTD31-HTD00, HTP3-HTP0, CBD91-CBD00 pins

5. RXADDR**, TXADDR**, RXENB*_B, TXENB*_B, TXDATA***, TXSOC* pins

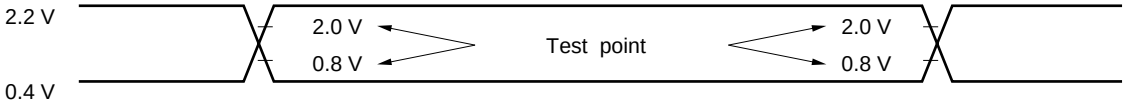
6. RDY_B, AD31-AD00 pins

7. INT, JDO, RXADDR**, TXADDR**, RXENB*_B, TXENB*_B, TXDATA***, TXSOC*, HTCS1_B, HTCS0_B, CBCS1_B, HTA17-HTA00, HTWE_B, HTOE_B, CBA17-CBA00, CBCS0_B, CBWE_B, CBOE_B, RDY_B, AD31-AD00 pins

8. HTD31-HTD00, HTP3-HTP0, CBD91-CBD00 pins

9. The approximate TYP. value of the operating current (I_{DD}) depends on the throughput of switching. For example with the following conditions, it is calculated as shown below.
Conditions: 8-bit UTOPIA interface × 4 ports, SWCLK = 40 MHz, UCLK0 to UCLK3 = 50 MHz
Calculation formula: I_{DD} (TYP.) = 267 × t + 600 mA, t (throughput): 0 – 1.5 [Unit: Gbps]

AC Test Output Waveform

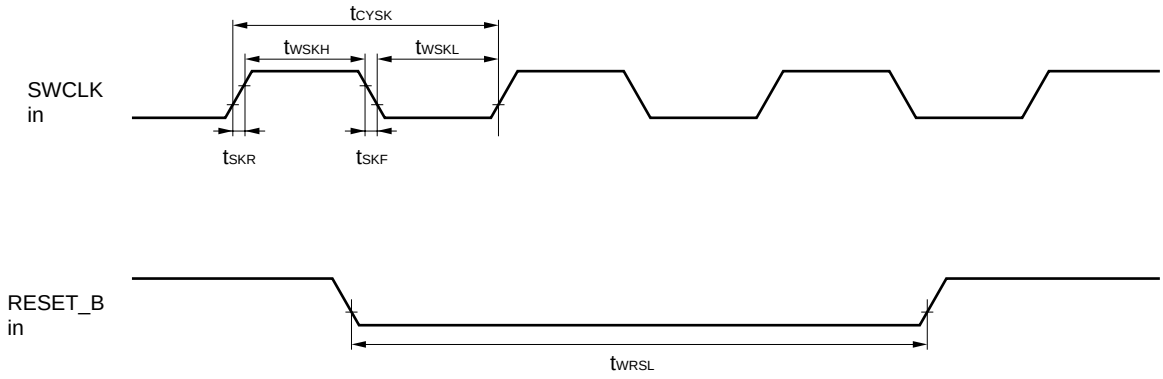


AC Characteristics (T_A = –40 to +85 °C, V_{DD} = 3.3 V ±5%)

(1) Control Signal

	Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
	SWCLK cycle time	t_{CYSL}		25		125	ns
★	SWCLK high-level width	t_{WSKH}		10.5		–	ns
★	SWCLK low-level width	t_{WSKL}		10.5		–	ns
	SWCLK rise time	t_{SKR}		–		2	ns
	SWCLK fall time	t_{SKF}		–		2	ns
	RESET_B low-level width	t_{WRSL}		16		–	t_{CYSK}

Control Signal



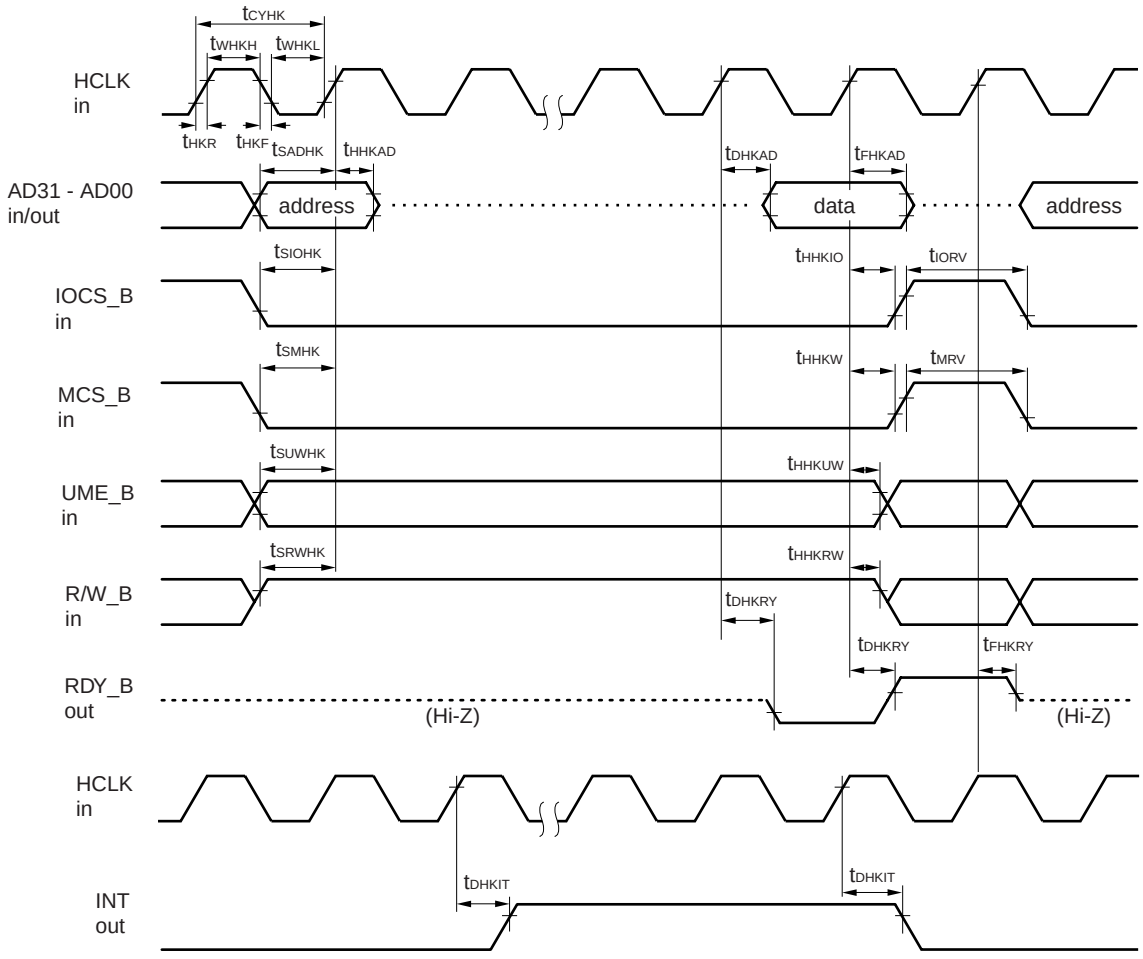
(2) Processor interface (32-bit mode, read/write)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
HCLK cycle time	t_{CYHK}		30		125	ns
HCLK high-level width	t_{WHKH}		12		–	ns
HCLK low-level width	t_{WHKL}		12		–	ns
HCLK rise time	t_{HKR}		–		3	ns
HCLK fall time	t_{HKF}		–		3	ns
HCLK ↑→ INT output delay time	t_{DHKIT}	Load capacitance 30 pF	1		17	ns
HCLK ↑→ RDY_B output delay time	t_{DHKRY}	Load capacitance 70 pF	1		17	ns
HCLK ↑→ RDY_B float output delay time	t_{FHKRY}	Load capacitance 70 pF	1		17	ns
HCLK ↑→ AD output delay time	t_{DHKAD}	Load capacitance 70 pF	1		17	ns
HCLK ↑→ AD float output delay time	t_{FHKAD}	Load capacitance 70 pF	1		17	ns
AD setup time (vs. HCLK ↑)	t_{SADHK}		8		–	ns
AD hold time (vs. HCLK ↑)	t_{HHKAD}		1		–	ns
IOCS_B setup time (vs. HCLK ↑)	t_{SIOHK}		8		–	ns
IOCS_B hold time (vs. HCLK ↑)	t_{HHKIO}		1		–	ns
★ IOCS_B recovery time	t_{IORV}		**Note**		–	ns
MCS_B setup time (vs. HCLK ↑)	t_{SMHK}		8		–	ns
MCS_B hold time (vs. HCLK ↑)	t_{HHKM}		1		–	ns
★ MCS_B recovery time	t_{MRV}		**Note**		–	ns
UWE_B setup time (vs. HCLK ↑)	t_{SUWHK}		8		–	ns
UWE_B hold time (vs. HCLK ↑)	t_{HHKUW}		1		–	ns
R/W_B setup time (vs. HCLK ↑)	t_{SRWHK}		8		–	ns
R/W_B hold time (vs. HCLK ↑)	t_{HHKRW}		1		–	ns

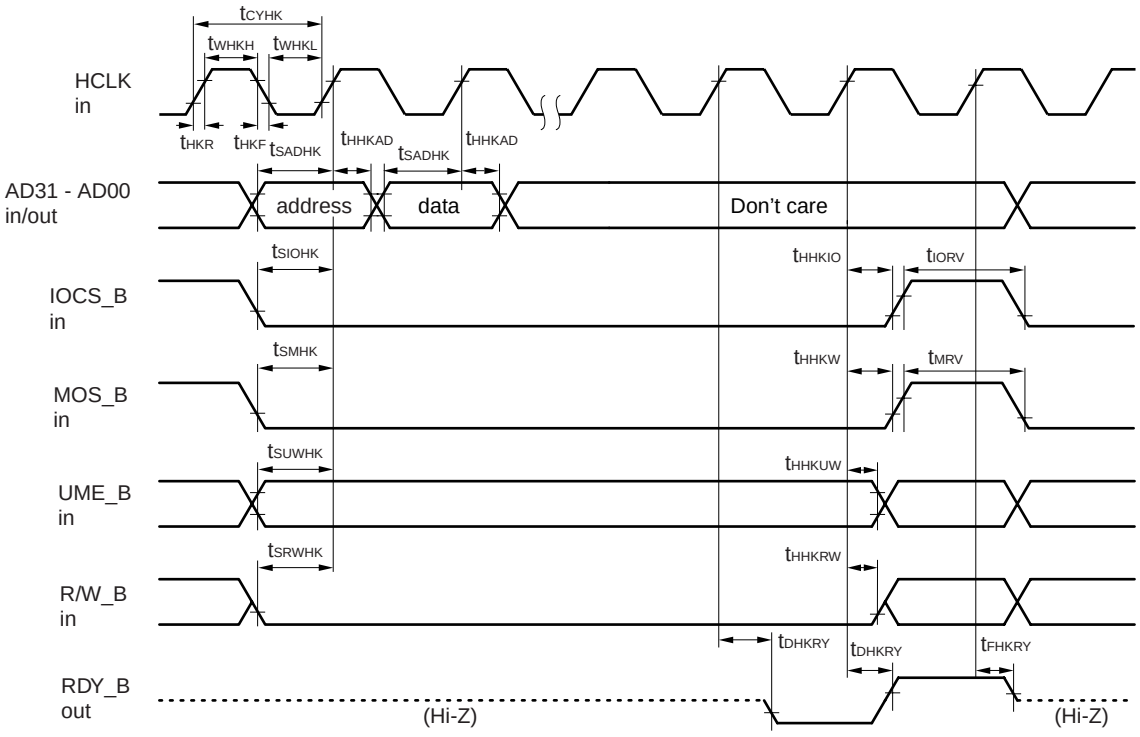
Note (1) When HCLK cycle time (t_{CYHK}) < 4 × SWCLK cycle time (t_{CYSK}):
IOCS_B recovery time (t_{IORV}) = MCS_B recovery time (t_{MRV}) = t_{CYHK}

(2) When HCLK cycle time (t_{CYHK}) ≥ 4 × SWCLK cycle time (t_{CYSK}):
IOCS_B recovery time (t_{IORV}) = MCS_B recovery time (t_{MRV}) = $t_{CYHK} \times 2$

Processor interface (32-bit mode, read)



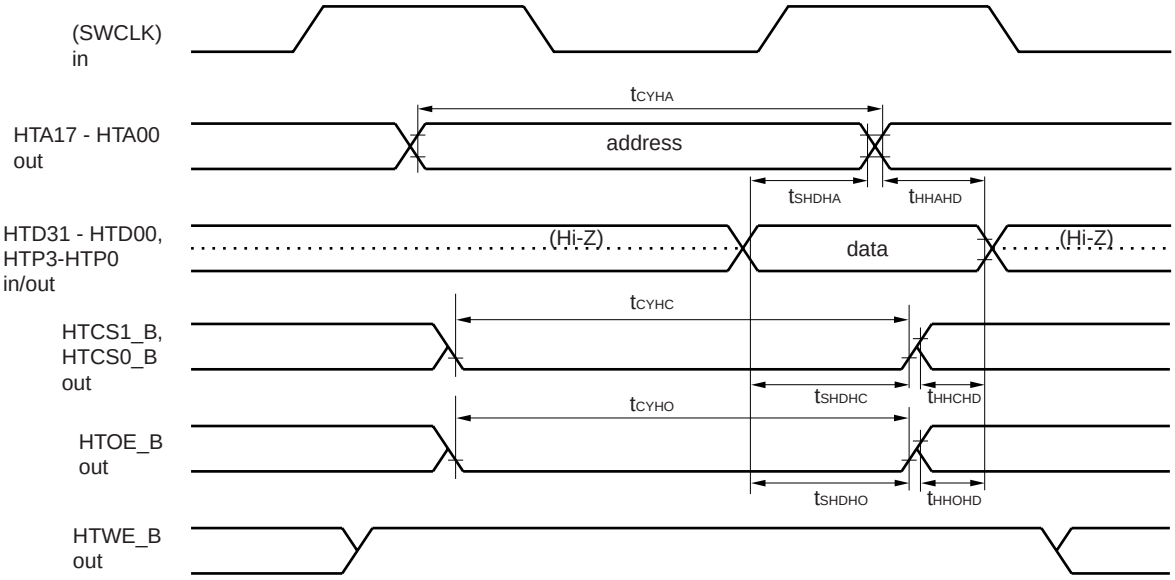
Processor interface (32-bit mode, write)



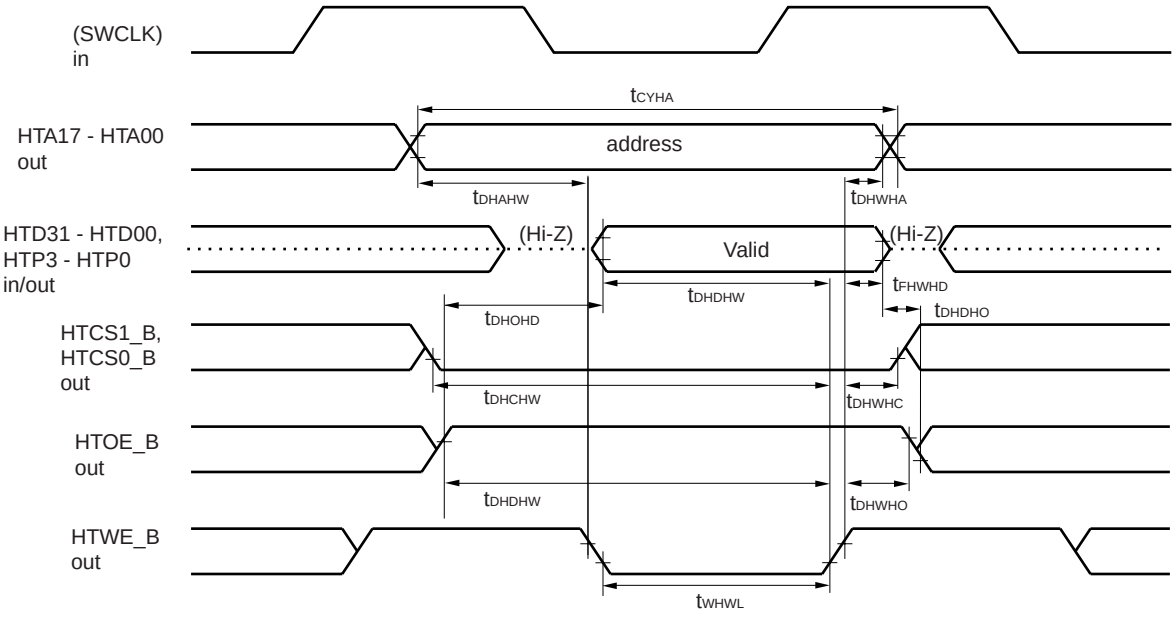
★ (3) HTT & control memory interface

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
HTA cycle time	t_{CYHA}	Load capacitance 50 pF	t_{CYSK} – 2			ns
HTD, HTP setup time (vs. HTA)	t_{SHDHA}		9			ns
HTD, HTP hold time (vs. HTA)	t_{HHAHD}		1			ns
HTCS_B cycle time	t_{CYHC}	Load capacitance 50 pF	t_{CYSK} – 2			ns
HTD, HTP setup time (vs. HTCS_B)	t_{SHDHC}		9			ns
HTD, HTP hold time (vs. HTCS_B)	t_{HHCHD}		1			ns
HTOE_B cycle time	t_{CYHO}	Load capacitance 50 pF	t_{CYSK} – 2			ns
HTD, HTP setup time (vs. HTOE_B)	t_{SHDHO}		9			ns
HTD, HTP hold time (vs. HTOE_B)	t_{HHOHD}		1			ns
HTWE_B low-level width	t_{WHWL}	Load capacitance 50 pF	t_{WSKL} – 1.5			ns
Data → HTWE_B ↑ output delay time	t_{DHDHW}	Load capacitance 50 pF	t_{WSKL} – 3			ns
HTWE_B ↑→ Data float output delay time	t_{FHWHD}	Load capacitance 50 pF	0			ns
HTA → HTWE_B ↓ output delay time	t_{DHAHW}	Load capacitance 50 pF	t_{WSKH} – 5			ns
HTCS_B ↓→ HTWE_B ↑ output delay time	t_{DHCHW}	Load capacitance 50 pF	t_{CYSK} – 6			ns
HTOE_B ↑→ HTWE_B ↑ output delay time	t_{DHOHW}	Load capacitance 50 pF	t_{CYSK} – 6			ns
HTWE_B ↑→ HTA output delay time	t_{DHWHA}	Load capacitance 50 pF	0			ns
HTWE_B ↑→ HTCS_B ↑ output delay time	t_{DHWHC}	Load capacitance 50 pF	0			ns
HTWE_B ↑→ HTOE_B ↓ output delay time	t_{DHWHO}	Load capacitance 50 pF	0			ns
HTD float → HTOE_B ↓ output delay time	t_{DHDHO}	Load capacitance 50 pF	0			ns
HTOE_B ↑→ Data output delay time	t_{DHOHD}	Load capacitance 50 pF	t_{WSKH} – 3			ns

HTT & control memory interface (read)



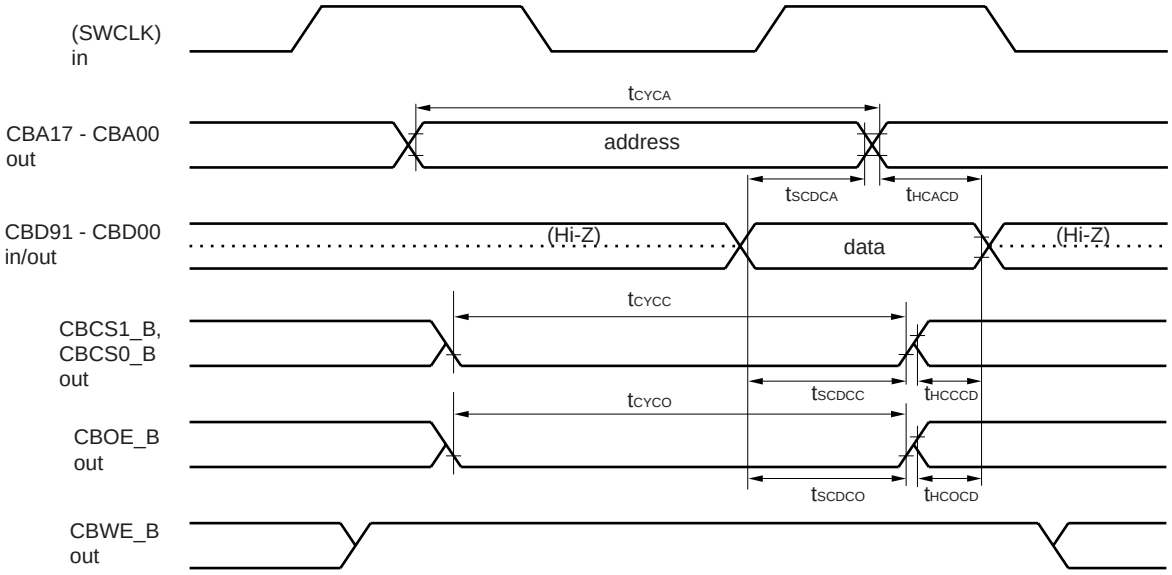
HTT & control memory interface (write)



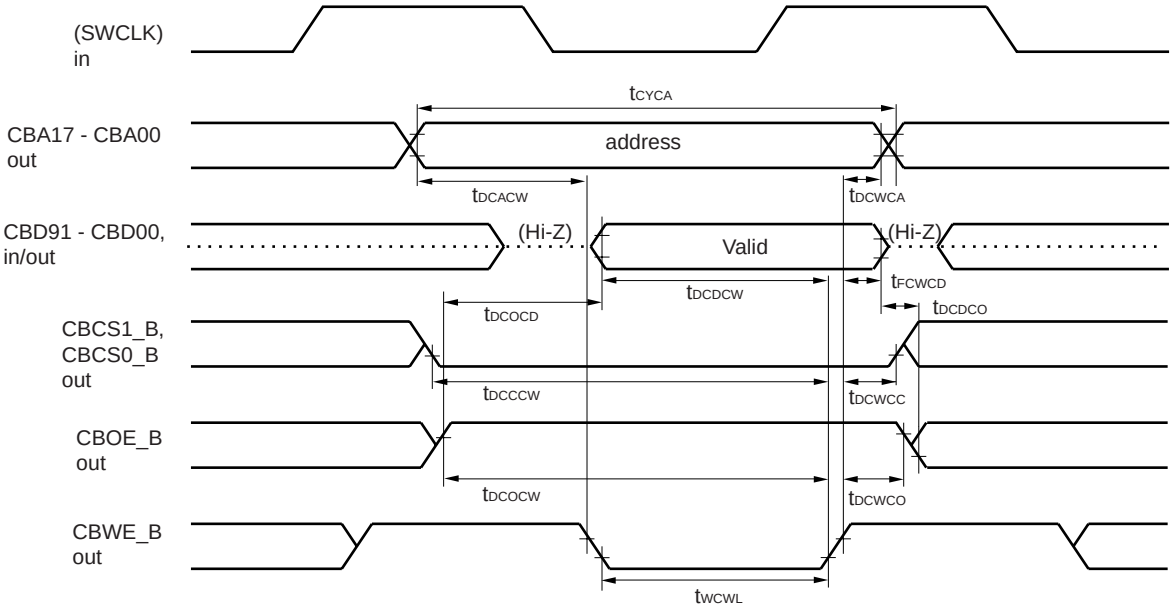
★ **(4) Cell buffer memory interface**

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
CBA cycle time	t_{CYCA}	Load capacitance 50 pF	t_{CYSK} – 2			ns
CBD setup time (vs. CBA)	t_{SCDCA}		9			ns
CBD hold time (vs. CBA)	t_{HCACD}		1			ns
CBCS_B cycle time	t_{CYCC}	Load capacitance 50 pF	t_{CYSK} – 2			ns
CBD setup time (vs. CBCS_B)	t_{SCDCC}		9			ns
CBD hold time (vs. CBCS_B)	t_{HCCCD}		1			ns
CBOE_B cycle time	t_{CYCO}	Load capacitance 50 pF	t_{CYSK} – 2			ns
CBD setup time (vs. CBOE_B)	t_{SCDCO}		9			ns
CBD hold time (vs. CBOE_B)	t_{HCOCD}		1			ns
CBWE_B low-level width	t_{WCWL}	Load capacitance 50 pF	t_{WSKL} – 1.5			ns
Data → CBWE_B ↑ output delay time	t_{DCDCW}	Load capacitance 50 pF	t_{WSKL} – 3			ns
CBWE_B ↑→ Data float output delay time	t_{FCWCD}	Load capacitance 50 pF	0			ns
CBA → CBWE_B ↓ output delay time	t_{DCACW}	Load capacitance 50 pF	t_{WSKH} – 5			ns
CBCS_B ↓→ CBWE_B ↑ output delay time	t_{DCCCW}	Load capacitance 50 pF	t_{CYSK} – 6			ns
CBOE_B ↑→ CBWE_B ↑ output delay time	t_{DCOCW}	Load capacitance 50 pF	t_{CYSK} – 6			ns
CBWE_B ↑→ CBA output delay time	t_{DCWCA}	Load capacitance 50 pF	0			ns
CBWE_B ↑→ CBCS_B ↑ output delay time	t_{DCWCC}	Load capacitance 50 pF	0			ns
CBWE_B ↑→ CBOE_B ↓ output delay time	t_{DCWCO}	Load capacitance 50 pF	0			ns
CBD float → CBOE_B ↓ output delay time	t_{DCDCO}	Load capacitance 50 pF	0			ns
CBOE_B ↑→ Data output delay time	t_{DCOCD}	Load capacitance 50 pF	t_{WSKH} – 3			ns

Cell buffer memory interface (read)



Cell buffer memory interface (write)

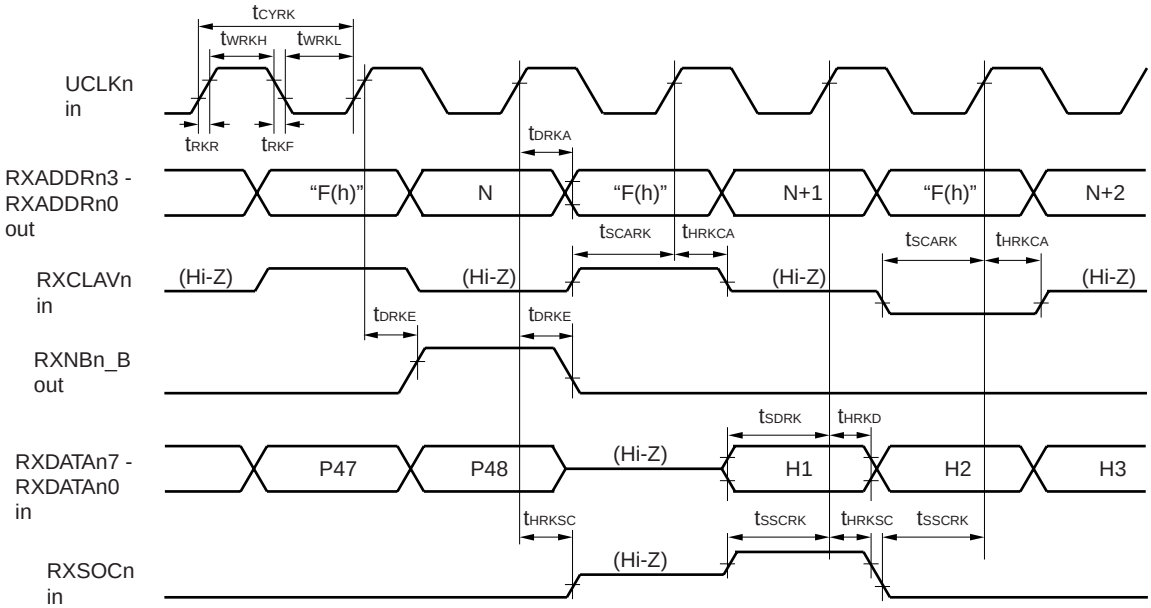


(5) UTOPIA interface (reception)

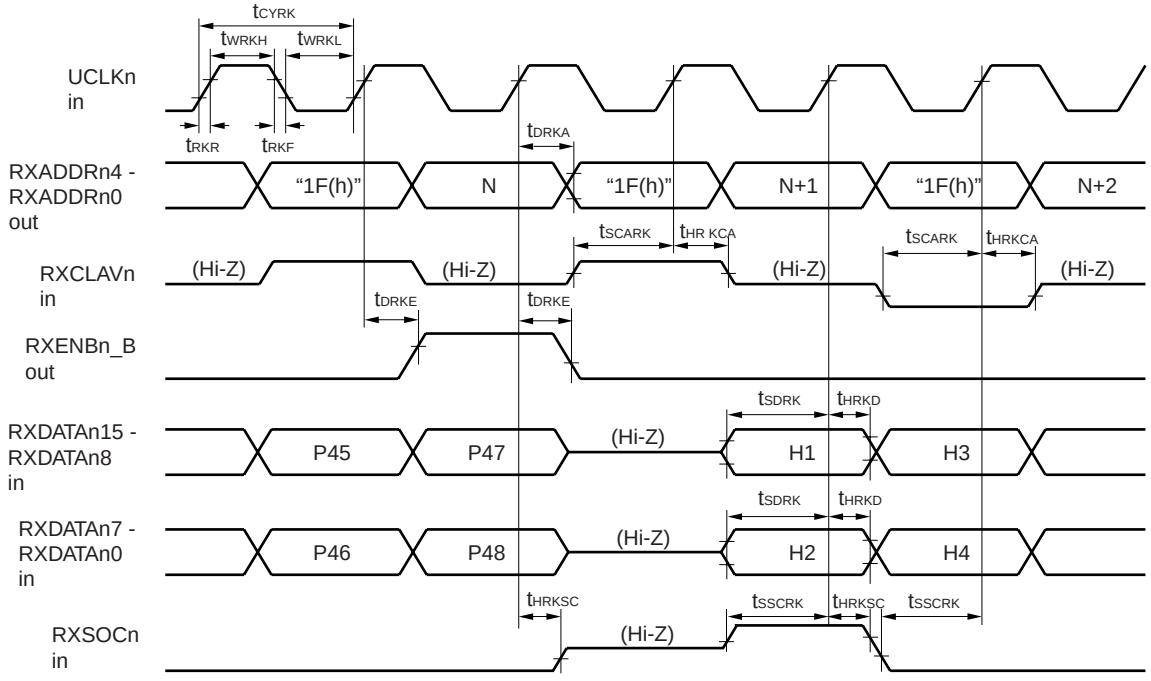
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
UCLK cycle time	t_{CYRK}		20		125	ns
UCLK high-level width	t_{WRKH}		8			ns
UCLK low-level width	t_{WRKL}		8			ns
UCLK rise time	t_{RKR}				2	ns
UCLK fall time	t_{RKF}				2	ns
UCLK ↑→ RXADDR output delay time	t_{DRKA}	Load capacitance 50 pF	1		14	ns
UCLK ↑→ RXENB_B output delay time	t_{DRKE}	Load capacitance 50 pF	1		14	ns
RXCLAV setup time (vs. UCLK ↑)	t_{SCARK}		4			ns
RXCLAV hold time (vs. UCLK ↑)	t_{HRKCA}		1			ns
RXDATA setup time (vs. UCLK ↑)	t_{SDRK}		4			ns
RXDATA hold time (vs. UCLK ↑)	t_{HRKD}		1			ns
RXSOC setup time (vs. UCLK ↑)	t_{SSCRK}		4			ns
RXSOC hold time (vs. UCLK ↑)	t_{HRKSC}		1			ns

UTOPIA interface (reception) (n = 0 - 3)

8-bit mode



16-bit mode

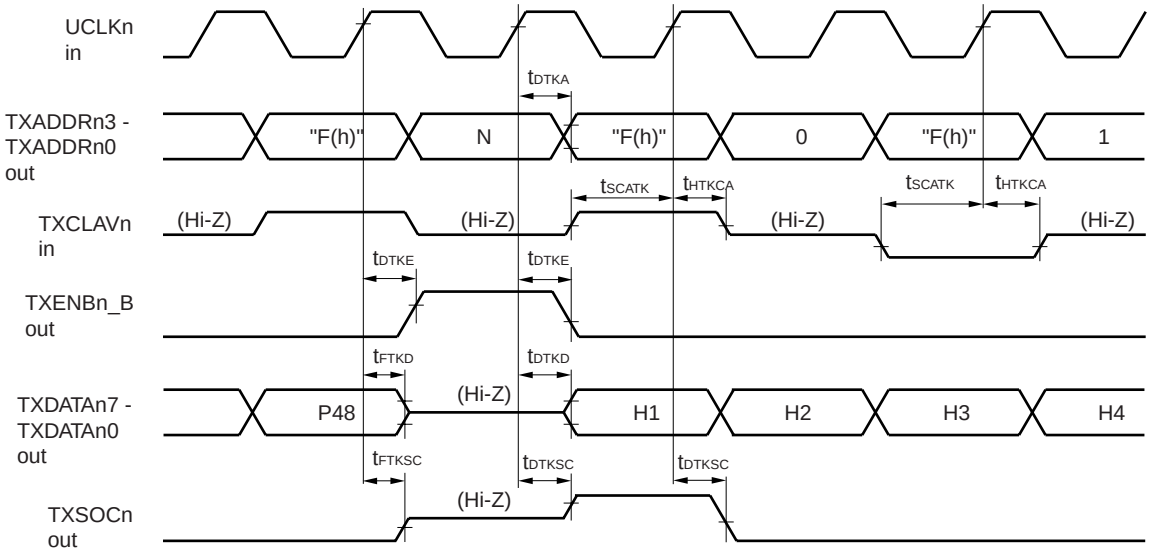


(6) UTOPIA interface (transmission)

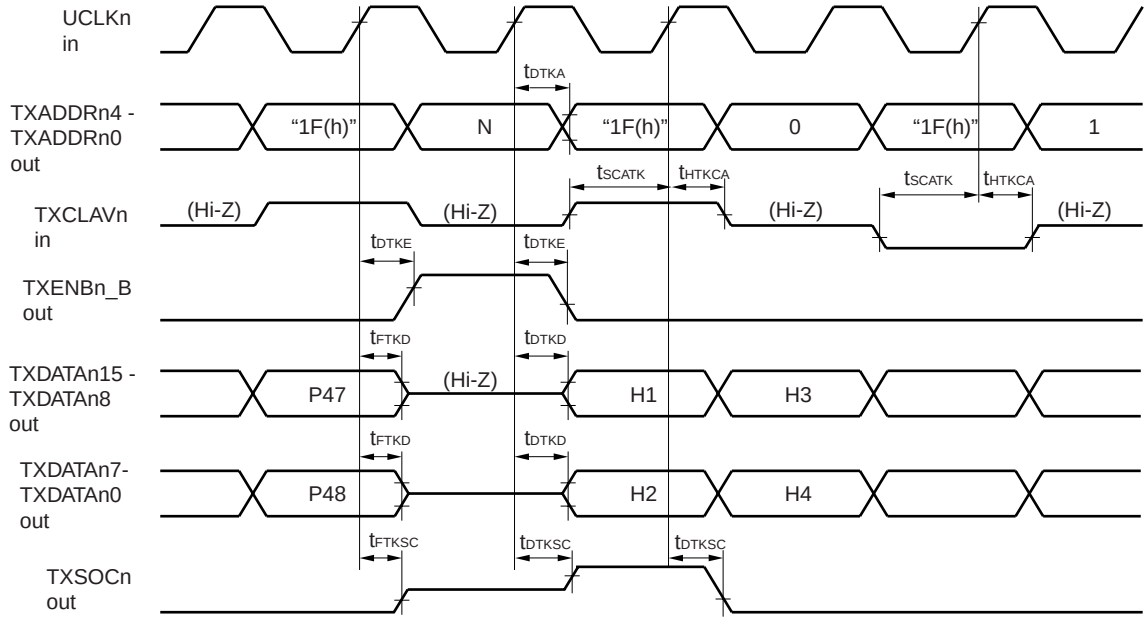
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
UCLK ↑→ TXADDR output delay time	t_{DTKA}	Load capacitance 50 pF	1		14	ns
UCLK ↑→ TXENB_B output delay time	t_{DTKE}	Load capacitance 50 pF	1		14	ns
UCLK ↑→ TXDATA output delay time	t_{DTKD}	Load capacitance 50 pF	1		14	ns
UCLK ↑→ TXDATA float output delay time	t_{FTKD}	Load capacitance 50 pF	1		14	ns
UCLK ↑→ TXSOC output delay time	t_{DTKSC}	Load capacitance 50 pF	1		14	ns
UCLK ↑→ TXSOC float output delay time	t_{FTKSC}	Load capacitance 50 pF	1		14	ns
TXCLAV setup time (vs. UCLK ↑)	t_{SCATK}		4			ns
TXCLAV hold time (vs. UCLK ↑)	t_{HTKCA}		1			ns

UTOPIA interface (transmission) (n = 0 - 3)

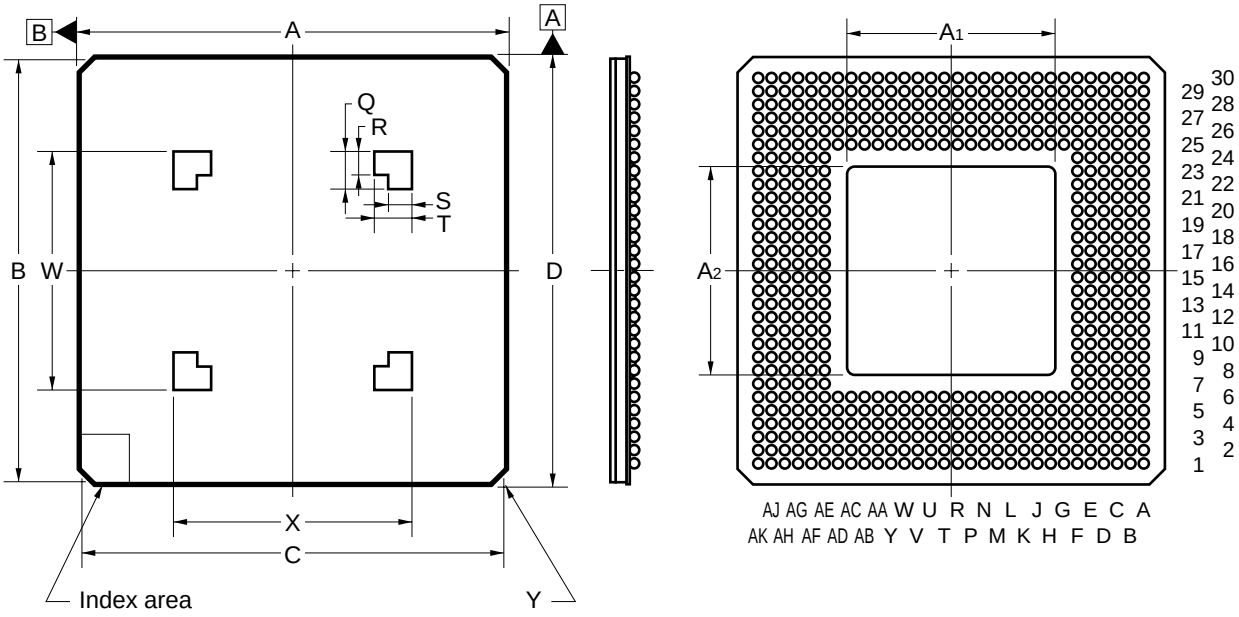
8-bit mode

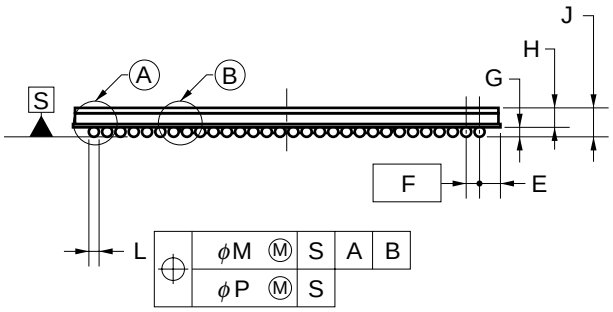


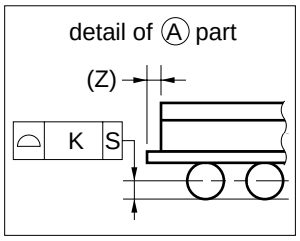
16-bit mode

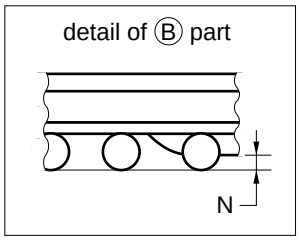


3. PACKAGE DRAWING









ITEM	MILLIMETERS
A	40.00±0.20
A_1	23.00 MAX.
A_2	23.00 MAX.
B	39.60±0.15
C	39.60±0.15
D	40.00±0.20
E	1.585
F	1.27 (T.P.)
G	0.60±0.10
H	$0.80^{+0.20}_{-0.10}$
J	$1.40^{+0.30}_{-0.20}$
K	0.15
L	φ0.75±0.15
M	0.30
N	0.25 MIN.
P	0.10
Q	3.0
R	2.0
S	2.0
T	3.0
W	22.73
X	22.73
Y	C 0.40
Z	0.20

S576N7-127-H6-1

4. RECOMMENDED SOLDERING CONDITIONS

Solder this product under the following recommended conditions.

For details of the recommended soldering conditions, refer to information document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended, consult NEC.

Surface-mount type

- **μPD98412N7-H6: 576-pin tape BGA (40 × 40)**

Soldering Method(s)	Soldering Conditions	Recommended Conditions Symbol
Infrared reflow	Package peak temperature: 235 °C, Time: 30 sec max. (210 °C min.), Number of times: three times max., Number of days: 7[Note] (after that, prebaking is necessary at 125 °C for 10 hours)	IR35-107-3
Partial heating	Pin temperature: 300 °C max. (per device side), Time: 3 sec max. (per device side)	–

Note Number of days in storage after the dry pack has been opened. The storage conditions are at 25 °C, 65% RH MAX.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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