

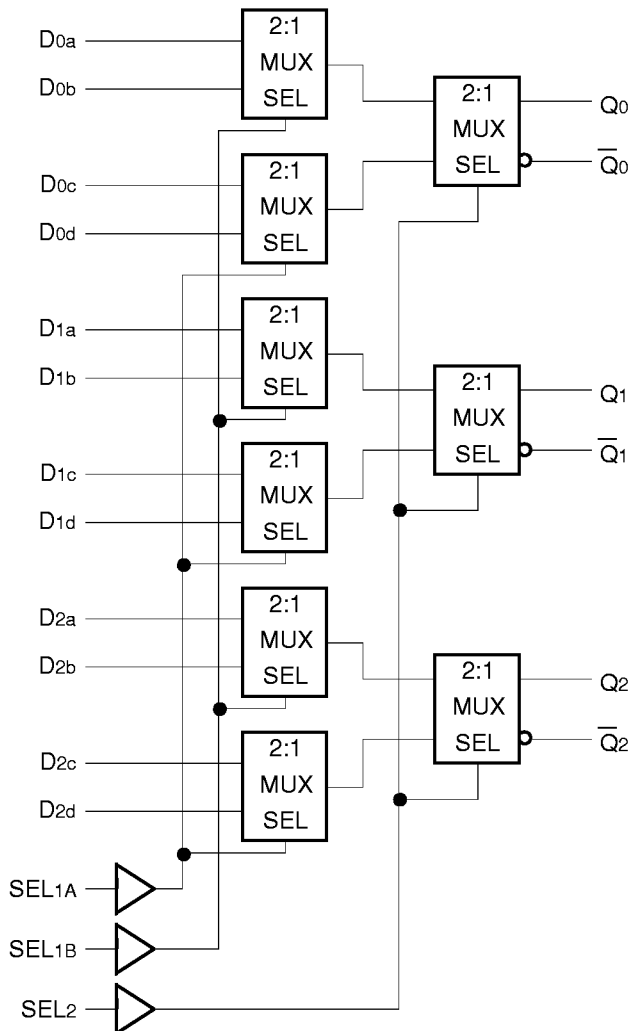
FEATURES

- 725ps max. D to output
- Extended 100E VEE range of -4.2V to -5.5V
- Differential outputs
- Split select architecture
- Fully compatible with industry standard 10KH, 100K ECL levels
- Internal 75KΩ input pulldown resistors
- ESD protection of 2000V
- Fully compatible with Motorola MC10E/100E171
- Available in 28-pin PLCC package

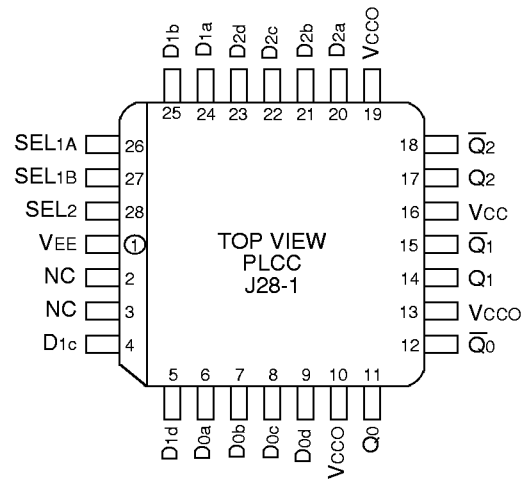
DESCRIPTION

The SY10/100E171 offer three 4:1 multiplexers with differential outputs, designed for use in new, high-performance ECL systems. The leading 4-bit multiplexer operation is organized pairwise, with each pair being a 2-bit multiplexer. Separate select (SEL1A, SEL1B) controls are provided within each pair. The SEL1A and SEL1B signals control the leading multiplexers, while the SEL2 signal controls the output multiplexer. The three select signals can be used to determine which of the four data inputs will be propagated to the corresponding outputs.

BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

Pin	Function
D0x-D2x	Data Inputs
SEL1A, SEL1B	First-stage Select Inputs
SEL2	Second-stage Select Input
Q0-Q2	True Output
Q0-Q2	Inverted Output
VCCO	Vcc to Output

TRUTH TABLE

Pin	State	Operation
SEL2	H	Output c/d data
SEL1A	H	Input d data
SEL1B	H	Input b data

DC ELECTRICAL CHARACTERISTICS

VEE = VEE (Min.) to VEE (Max.); VCC = VCCO = GND

Symbol	Parameter	TA = 0°C			TA = +25°C			TA = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I _{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	μA	—
I _{EE}	Power Supply Current	—	—	—	—	—	—	—	—	—	mA	—
		10E	56	67	56	67	56	67	56	67		
		100E	56	67	56	67	65	77				

AC ELECTRICAL CHARACTERISTICS

VEE = VEE (Min.) to VEE (Max.); VCC = VCCO = GND

Symbol	Parameter	TA = 0°C			TA = +25°C			TA = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t _{PLH} t _{PHL}	Propagation Delay to Output D SEL1 SEL2	275 450 350	480 650 550	650 850 700	275 450 350	480 650 550	650 850 700	275 450 350	480 650 550	650 850 700	ps	—
t _{skew}	Within-Device Skew D _{nm} , D _{nm} to Q _n D _a , D _b , D _c , D _d to Q	— —	60 40	— —	— —	60 40	— —	— —	60 40	— —	ps	1
t _r t _f	Rise/Fall Time 20% to 80%	300	475	650	300	475	650	300	475	650	ps	—

NOTE:

1. Within-device skew is defined as identical transitions on similar paths through a device; n = 0, 1, 2 m = a, b, c, d.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E171JC	J28-1	Commercial
SY10E171JCTR	J28-1	Commercial
SY100E171JC	J28-1	Commercial
SY100E171JCTR	J28-1	Commercial

28 LEAD PLASTIC LEADED CHIP CARRIER (J28-1)

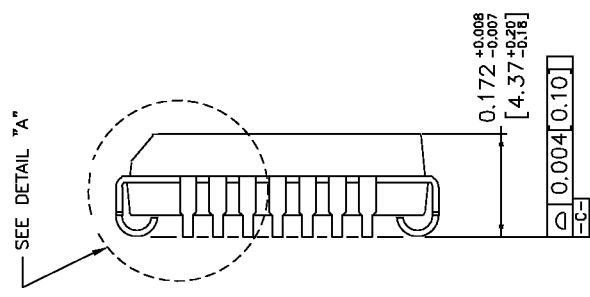
FILE/REV #: PD0008A03

PD/0008/ASCORP

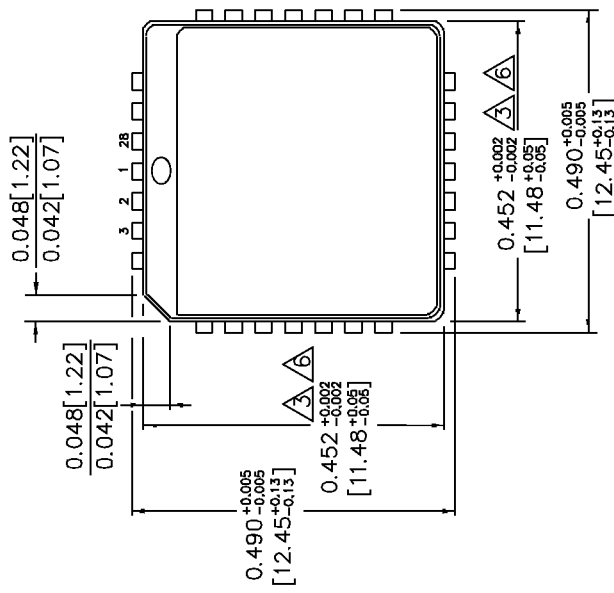
PAGE 1 OF 1

REV.	REVISION DESCRIPTION	DATE
01	CONVERT TO DESIGNER VERSION A.D. FORMAT AND COVER PAGE TO SPEC. CHANGE BODY WIDTH DIMENSION FROM 0.450(11.43) TO 0.443(11.25) TYP. GEOMETRICAL ERROR.	08/18/94
02	CONVERT DWG FROM DESIGNER TO AUTOCAD REL. 12. REFERENCE AMKOR DWG. NO. 34653 REV. 00.	02/22/96
03	CONVERT DWG TO REL. 13 AND ONE PAGE DOCUMENT.	02/18/98

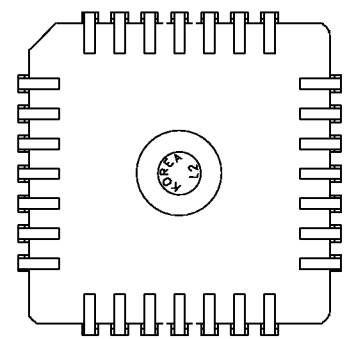
SIDE VIEW



TOP VIEW

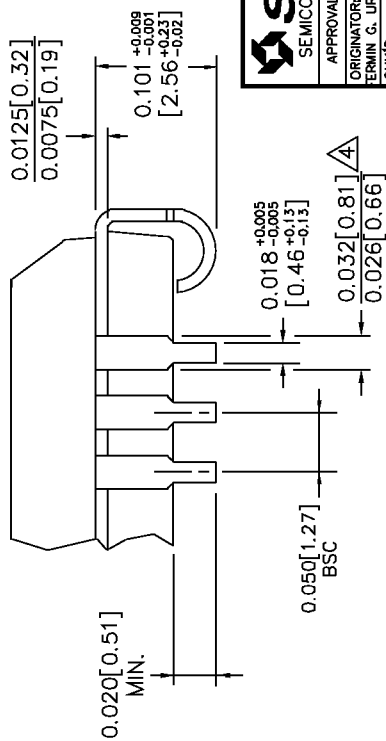


BOTTOM VIEW



NOTES:

1. DIMENSIONS ARE IN INCHES [MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008 [0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.



DETAIL "A"

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SEMICONDUCTOR

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APPROVALS	DATE	APPROVALS	DATE	SIZE	PACKAGE OUTLINE
ORIGINATOR: ERMIN G. URRUTIA	02/23/98	QUALITY: MARSHALL WILDER		A	28 LEAD PLCC
CHK'D: WON CHANG		DOCUMENT CONTROL: BRIAN SANFILIPPO			
RELEASE DATE:					

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SCALE: N/A
REVISION: 03