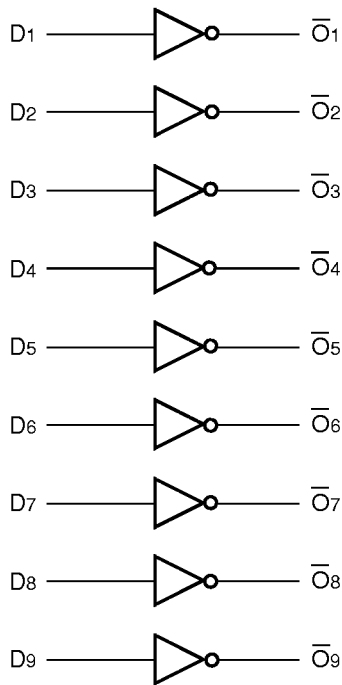


### FEATURES

- Max. propagation delay of 700ps
- IEE min. of -55mA
- Extended supply voltage option:  
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- 70% faster than National 300K at lower power
- Internal 75KΩ input pull-down resistors
- Function and pinout compatible with National and Signetics F100K
- ESD protection of 2000V
- Available in 24-pin CERPDP, 24-pin CERPACK and 28-pin PLCC packages

### BLOCK DIAGRAM



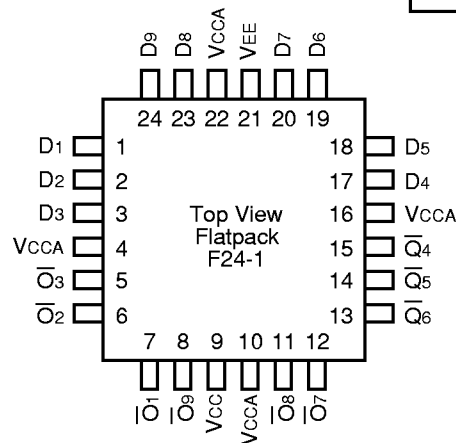
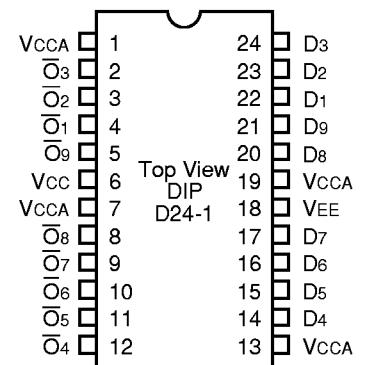
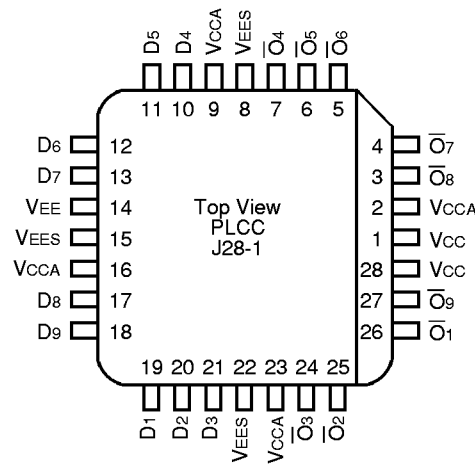
### PIN NAMES

Pin	Function
D1 – D9	Data Inputs
$\bar{Q}_1 - \bar{Q}_9$	Data Outputs
VEES	VEE Substrate
VCCA	VCCO for ECL Outputs

### DESCRIPTION

The SY100S321 is a monolithic 9-bit inverter. The device contains nine inverting buffer gates with single input and output.

### PIN CONFIGURATIONS



## DC ELECTRICAL CHARACTERISTICS

$V_{EE} = -4.2V$  to  $-5.5V$  unless otherwise specified,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I <sub>IH</sub>	Input HIGH Current	—	—	200	μA	$V_{IN} = V_{IH} (Max.)$
I <sub>EE</sub>	Power Supply Current	-55	-41	-25	mA	Inputs Open

## AC ELECTRICAL CHARACTERISTICS

### CERDIP

$V_{EE} = -4.2V$  to  $-5.5V$  unless otherwise specified,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	T <sub>A</sub> = 0°C		T <sub>A</sub> = +25°C		T <sub>A</sub> = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay <sup>(1)</sup> Data to Output	300	900	300	900	300	900	ps	
t <sub>TLH</sub> t <sub>THL</sub>	Transition Time <sup>(1)</sup> 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	
t <sub>s, G-G</sub>	Skew, Gate-to-Gate	—	200	—	200	—	200	ps	

**NOTE:**

- Reference figures 1 and 2

### CERPACK

$V_{EE} = -4.2V$  to  $-5.5V$  unless otherwise specified,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	T <sub>A</sub> = 0°C		T <sub>A</sub> = +25°C		T <sub>A</sub> = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay <sup>(1)</sup> Data to Output	300	800	300	800	300	800	ps	
t <sub>TLH</sub> t <sub>THL</sub>	Transition Time <sup>(1)</sup> 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	
t <sub>s, G-G</sub>	Skew, Gate-to-Gate	—	200	—	200	—	200	ps	

**NOTE:**

- Reference figures 1 and 2

### PLCC

$V_{EE} = -4.2V$  to  $-5.5V$  unless otherwise specified,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	T <sub>A</sub> = 0°C		T <sub>A</sub> = +25°C		T <sub>A</sub> = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay <sup>(1)</sup> Data to Output	300	700	300	700	300	700	ps	
t <sub>TLH</sub> t <sub>THL</sub>	Transition Time <sup>(1)</sup> 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	
t <sub>s, G-G</sub>	Skew, Gate-to-Gate	—	200	—	200	—	200	ps	

**NOTE:**

- Reference figures 1 and 2

**TEST CIRCUITRY<sup>(1)</sup>**

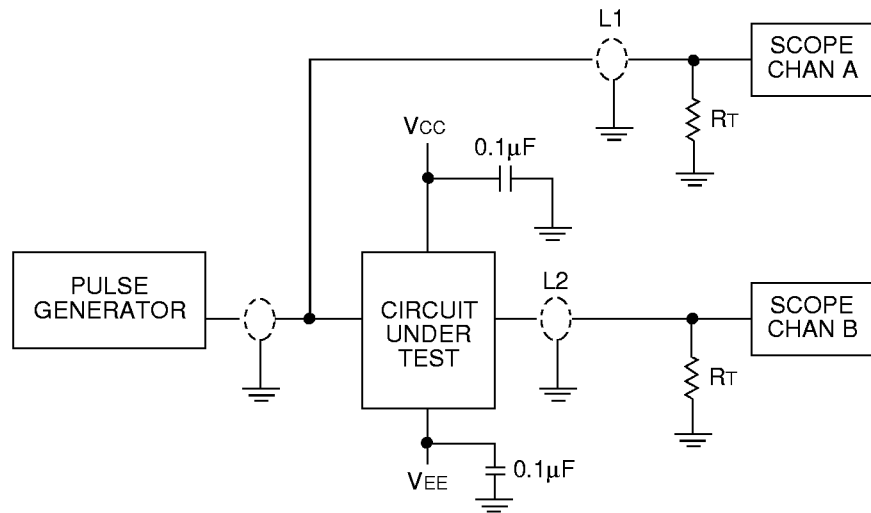


Figure 1. AC Test Circuit

**NOTE:**

- 1.  $V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V.$
- L1 and L2 = equal length 50Ω impedance lines.
- $R_T = 50\Omega$  terminator internal to scope.
- Decoupling 0.1µF from GND to  $V_{CC}$  and  $V_{EE}.$
- All unused outputs are loaded with 50Ω to GND.
- $C_L =$  Fixture and stray capacitance  $\leq 3pF.$

**SWITCHING WAVEFORMS**

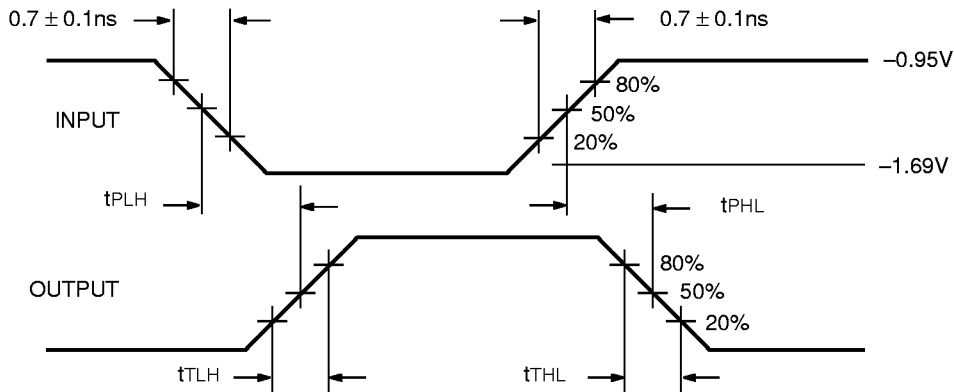


Figure 2. Propagation Delay and Transition Times

**NOTE:**

$V_{EE} = -4.2V$  to  $-5.5V$  unless otherwise specified,  $V_{CC} = V_{CCA} = GND$

**PRODUCT ORDERING CODE**

Ordering Code	Package Type	Operating Range
SY100S321DC	D24-1	Commercial
SY100S321FC	F24-1	Commercial
SY100S321JC	J28-1	Commercial
SY100S321JCTR	J28-1	Commercial

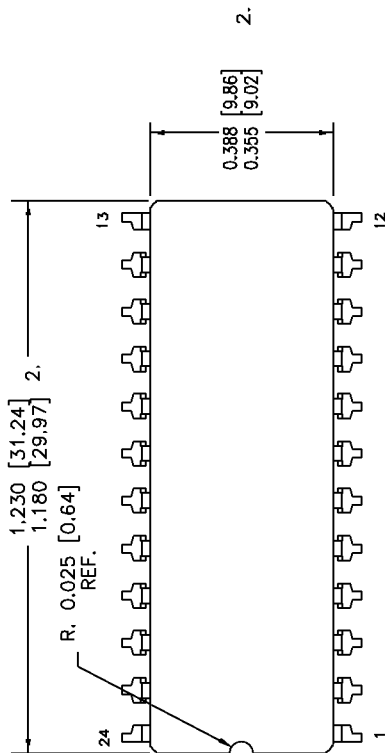
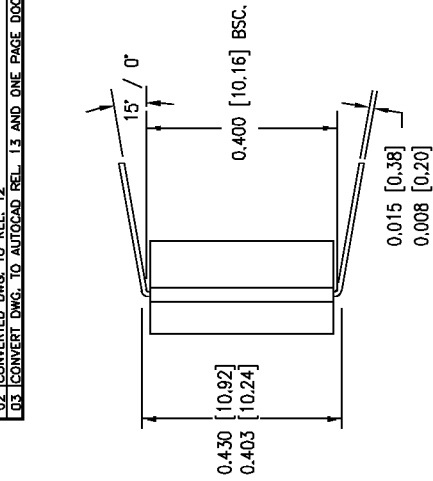
**24 LEAD CERDIP (D24-1)**

FILE/REV #: PD0003A03

PD/0003/ASCORP

PAGE 1 OF 1

REV.	REVISION DESCRIPTION	DATE
01	CONVERT DWG. TO DESIGNER VERSION 4.0 FORMAT.	12/30/93
02	CONVERTED DWG. TO REL. 12	03/15/96
03	CONVERT DWG. TO AUTOCAD REL. 1.3 AND ONE PAGE DOCUMENT.	02/18/98



**NOTES:**

1. DIMENSIONS ARE IN INCHES[MM].
- THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.



3250 SCOTT BOULEVARD  
SANTA CLARA CA 95054  
TEL: 408-980-9191  
FAX: 408-567-7878

APPROVALS	DATE	APPROVALS	DATE	SIZE	24 LEAD CERDIP (400" WIDE) PACKAGE OUTLINE
ORIGINATOR: FERMIN G. LURRITA	02/23/98	QUALITY: MARSHALL WILDER		A	
CHK'D: WON CHANG		DOCUMENT CONTROL: BRIAN SANFILIPPO			
RELEASE DATE:					SCALE N/A
					REVISION 03

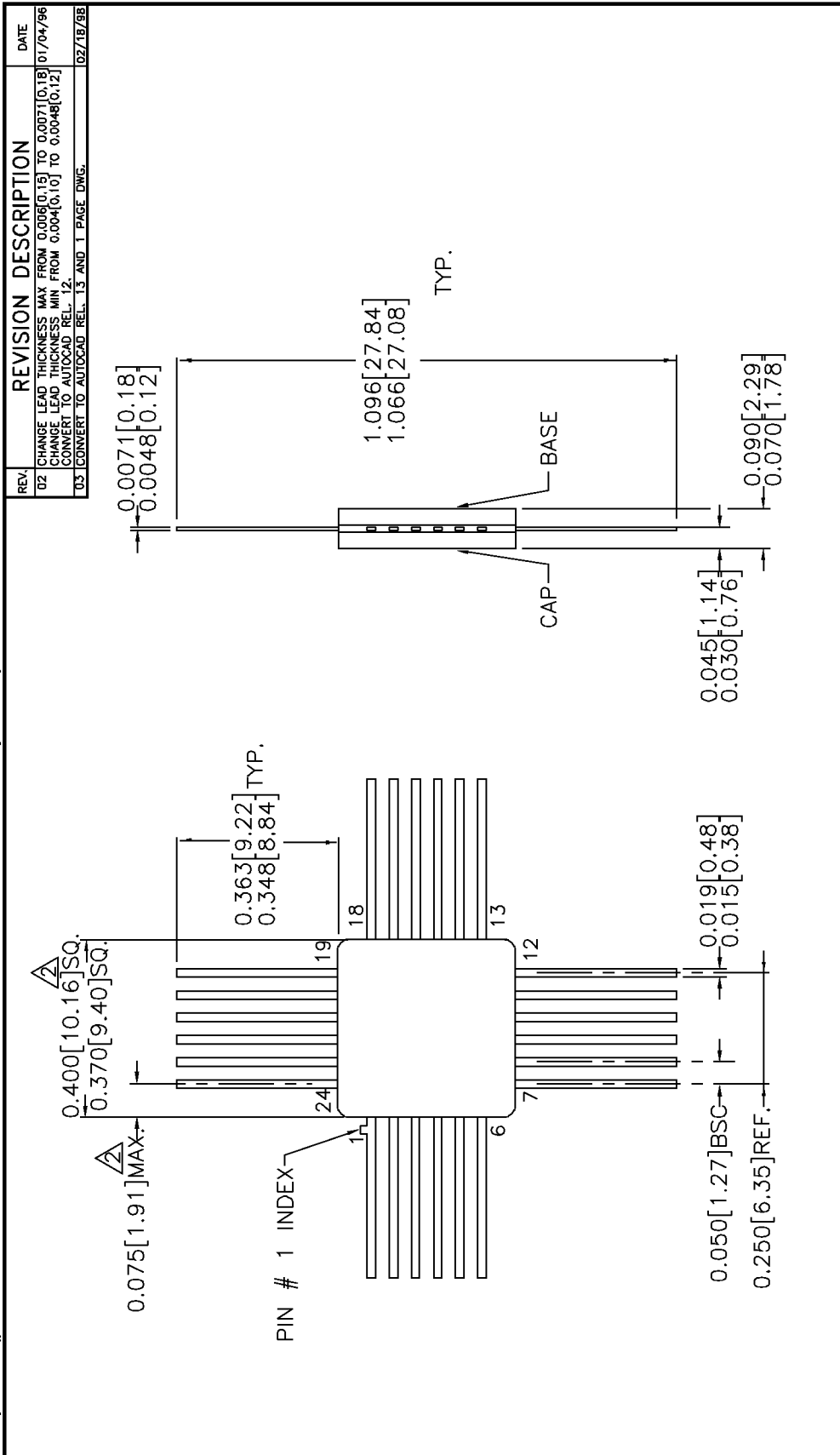
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**24 LEAD CERPACK (F24-1)**

FILE/REV #: PD0006A03

PD/0006/ASCORP

PAGE 1 OF 1



**REVISION DESCRIPTION**

REV.	REVISION DESCRIPTION	DATE
02	CHANGE LEAD THICKNESS MAX FROM 0.006 [0.15] TO 0.0071 [0.18] CHANGE LEAD THICKNESS MIN FROM 0.004 [0.10] TO 0.0048 [0.12] (CONVERT TO AUTOCAD REL. 12)	01/04/96
03	CONVERT TO AUTOCAD REL. 13 AND 1 PAGE DWG.	02/18/98

**NOTES:**

1. DIMENSIONS ARE IN INCHES [MM].
- THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.



3250 SCOTT BOULEVARD  
SANTA CLARA CA 95054  
TEL: 408-980-9191  
FAX: 408-587-7878

APPROVALS	DATE	APPROVALS	DATE	SIZE	24 LEAD CERPACK
ORIGINATOR: FERNUN G. URRUTIA	02/23/98	QUALITY: MARSHALL WILDER		A	PACKAGE OUTLINE
CHK'D: WON CHANG		DOCUMENT CONTROL: BRIAN SANFILIPPO			
RELEASE DATE:					

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SCALE: N/A  
REVISION: 03

**28 LEAD PLASTIC LEADED CHIP CARRIER (J28-1)**

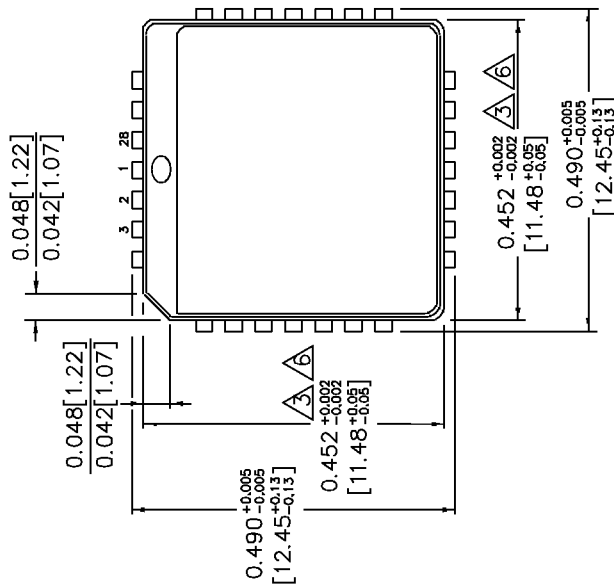
FILE/REV #: PD0008A03

PD/0008/ASCORP

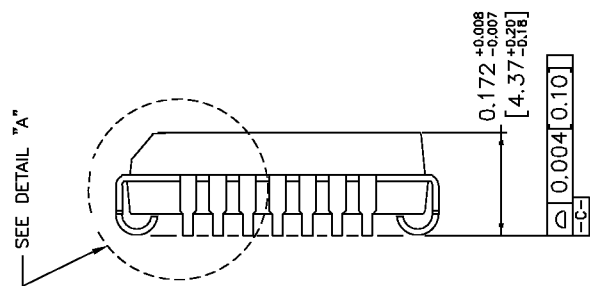
PAGE 1 OF 1

REV	REVISION DESCRIPTION	DATE
01	CONVERT TO DESIGNER VERSION A.0. FORMAT. ADD COVER PAGE TO SPEC. CHANGE BODY WIDTH DIMENSION FROM 0.450[11.43] TO 0.443[11.25]. TYPOGRAPHICAL ERROR.	08/18/94
02	CONVERT DWG FROM DESIGNER TO AUTOCAD. REL. 12. REFERENCE AMKOR DWG. NO. 34853 REV. 00.	02/22/96
03	CONVERT DWG TO REL. 13 AND ONE PAGE DOCUMENT.	02/18/98

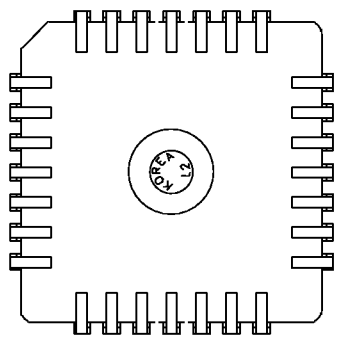
TOP VIEW



SIDE VIEW



BOTTOM VIEW



**NOTES:**

1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.



3250 SCOTT BOULEVARD  
SANTA CLARA, CA. 95054  
TEL: 408-980-9191  
FAX: 408-587-7878

APPROVALS	DATE	APPROVALS	DATE	SIZE	SCALE
ORIGINATOR: ERMIN G. URRUTIA	02/23/98	QUALITY: MARSHALL WILDER		A	28 LEAD PLCC
CHK'D: WON CHANG		DOCUMENT CONTROL: BRIAN SANFILIPPO			PACKAGE OUTLINE
RELEASE DATE:					THESE SPECIFICATIONS ARE THE PROPERTY OF SYNERGY SEMICONDUCTOR. ARE ISSUED IN STRICT CONFIDENCE AND SHALL NOT BE REPRODUCED, COPIED, OR USED AS THE BASIS FOR THE CONSTRUCTION OR SALE OF APPARATUS WITHOUT WRITTEN PERMISSION.
					SCALE N/A
					REVISION 03

DETAIL "A"