

8-bit Data Bus
Static RAM Card

MF31M0-M6DAPXX
MF32M0-M6DAPXX

Connector Type

Two-piece 60-pin

DESCRIPTION

Mitsubishi's static RAM cards provide large memory capacities on a device approximately the size of a credit card (85.6mm × 54mm × 3.4mm). The cards use an 8-bit data bus. The devices use a replaceable lithium battery to maintain data. Available in 1 M byte and 2 M byte capacities, Mitsubishi's Static RAM cards are available with a 60-pin, two-piece type connector.

- Electrostatic discharge protection to 25kV
- Buffered interface
- 60-pin connector
- 8-bit data width
- Write protect switch
- Battery voltage pin

FEATURES

- Uses TSOP (Thin Small Outline Package) to achieve very high memory density coupled with high reliability, without enlarging card size.

APPLICATIONS

- Office automation
- Computers
- Telecommunications
- Data Communications
- Industrial
- Consumer

PRODUCT LIST

Type name	Item	Memory capacity	Data bus width (bits)	Access time (ns)	Connector type	Number of pins	Outline drawing
MF31M0-M6DAPXX		1 MB	8	200	Two-piece	60	60P-004
MF32M0-M6DAPXX		2 MB					

STATIC RAM CARDS

PIN ASSIGNMENT

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	NC	} No connection	2	VBATT	Battery voltage
3	NC		4	NC	No connection
5	A12		6	CD 1	Card detect 1 (Note 1)
7	A 7		8	A15	} Address input
9	A 6	10	A16		
11	A 5	12	A17		
13	A 4	14	A18		
15	A 3	} Address input	16	A19	} A20 (NC for 1MB)
17	A 2		18	A20	
19	A 1		20	NC	
21	A 0		22	NC	
23	D 0	} Data I/O	24	NC	} No connection
25	D 1		26	NC	
27	D 2		28	NC	
29	GND		30	GND	
31	D 3	} Ground	32	GND	} Ground
33	D 4		34	NC	
35	D 5		36	NC	
37	D 6		38	NC	
39	D 7	} Data I/O	40	NC	} No connection
41	\overline{CE}		42	NC	
43	A10		44	NC	
45	\overline{OE}		46	NC	
47	A11	} Address input	48	WP	Write protect
49	A 9		50	NC	No connection
51	A 8		52	B 0	} Memory card type detect (Note 2)
53	A13		54	B 1	
55	A14	56	B 2		
57	\overline{WE}	Write Enable	58	CD2	Card detect 2 (Note 1)
59	VCC	Power supply	60	VCC	Power supply

Note 1 : Installing the card shorts connector pins 6 and 58, allowing host equipment to detect that a card is installed.

2 : Pins 52, 54 and 56 are either grounded or left open according to the card type (see table), allowing the host equipment to identify the card is installed.

3 : No signal should be applied to any "NC" pin.

	B 0	B 1	B 2
Card Type	52	54	56
RAM	GND	GND	GND
OTP	GND	NC	GND
Mask ROM	NC	GND	GND

STATIC RAM CARDS

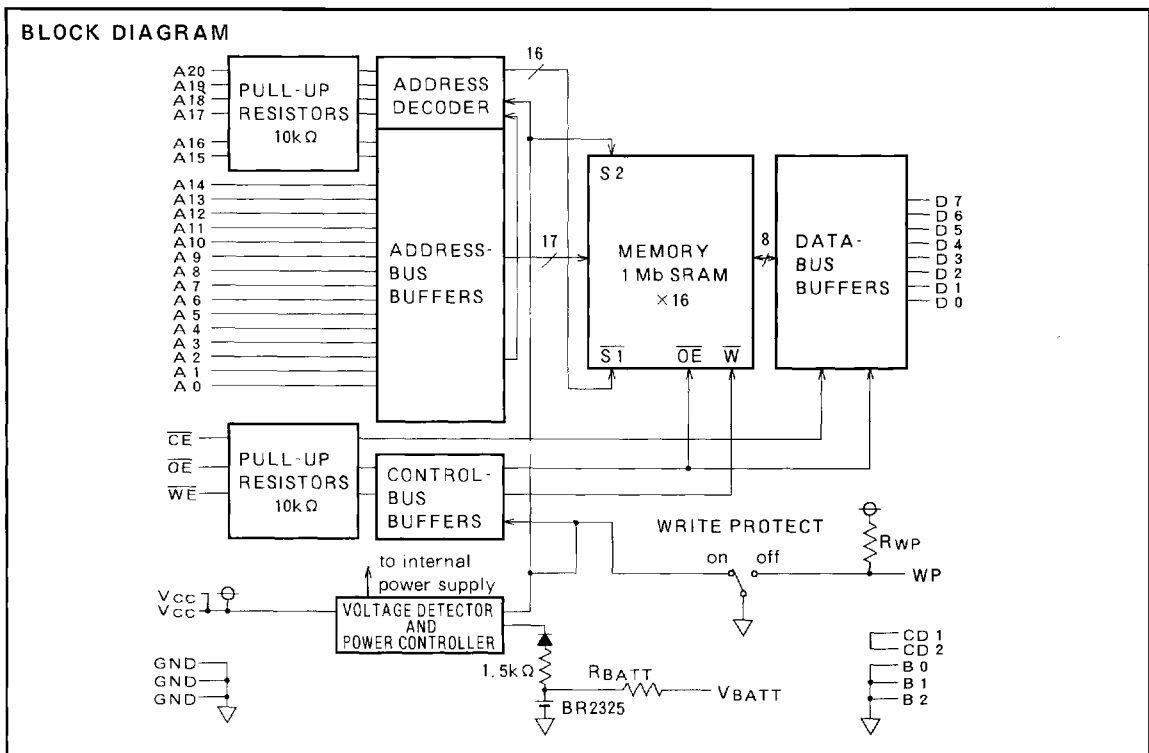
BATTERY VOLTAGE PIN (V_{BATT})

This pin is connected to the battery through a $100k\Omega$ ($94k\Omega \sim 106k\Omega$) resistor. If this pin is shorted with GND, the battery will be discharged. Never supply voltage to this pin as the battery cannot be charged.

WRITE PROTECT MODE (WP)

When the write protect switch is switched on, this card goes into a write protect mode that allows reading but not writing of data.

The WP pin is pulled-up by a $51k\Omega$ ($45k\Omega \sim 57k\Omega$) resistor. In normal mode the WP pin is grounded (the write protect switch is switched off). However when the card is switched into write protect mode the WP pin is no longer grounded and is pulled high. By testing the condition of this pin the system can easily tell whether the card is in write protect mode or not.



FUNCTION TABLE

Mode	\overline{CE}	WE	\overline{OE}	D_m	I_{cc}
Standby	H	X	X	High impedance	Standby
Write	L	L	H	D_{in}	Active
Read	L	H	L	D_{out}	Active
Output disable	L	H	H	High impedance	Active

Note 4 : H = V_{IH} , L = V_{IL} , X = V_{IH} or V_{IL}

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	-0.3 ~ +7	V
V_I	Input voltage		-0.5 ~ $V_{CC} + 0.3$ (7.0 max.)	V
V_O	Output voltage		0 ~ V_{CC}	V
T_{opr}	Operating temperature	Read, Write, Data retention	0 ~ 70	°C
T_{stg}	Storage temperature		-30 ~ 80	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = 0 \sim 50^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	Supply voltage	4.5		5.5	V
GND	Supply voltage		0		V
V_{IL}	Low-level input voltage	0		0.8	V
V_{IH}	High-level input voltage	$0.7 \times V_{CC}$		V_{CC}	V

ELECTRICAL CHARACTERISTICS ($T_a = 0 \sim 50^\circ\text{C}$, $V_{CC} = 4.5 \sim 5.5\text{V}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	High-level output voltage	$I_{OH} = -1\text{mA}$	2.4			V
V_{OL}	Low-level output voltage	$I_{OL} = 2\text{mA}$			0.4	V
I_{IH}	High-level input current	$V_I = V_{CC}$			25	μA
I_{IL}	Low-level input current	$V_I = 0\text{V}$			-10	μA
		other inputs A 0 ~ A14	-350			μA
I_{OZH}	Off-state high-level output current	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$; $V_O = V_{CC}$			10	μA
I_{OZL}	Off-state low-level output current	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$; $V_O = 0\text{V}$			-10	μA
$I_{CC1 \cdot 1}$	Active supply current (minimum cycle)	$\overline{CE} = V_{IL}$, other inputs = V_{IH} or V_{IL} , Outputs = pulled-up or pulled-down by 1 M Ω resistors			230	mA
$I_{CC1 \cdot 2}$	Active supply current (minimum cycle)	$\overline{CE} \leq 0.2\text{V}$, other inputs $\leq 0.2\text{V}$ or $\geq V_{CC} - 0.2\text{V}$, Outputs = pulled-up or pulled-down by 1 M Ω resistors			170	mA
$I_{CC2 \cdot 1}$	Standby supply current	$\overline{CE} = V_{IH}$, $A_n = \overline{OE} = \overline{WE} = V_{IH}$, $D_m = V_{IL}$ or V_{IH}			75	mA
$I_{CC2 \cdot 2}$	Standby supply current	$\overline{CE} \geq V_{CC} - 0.2\text{V}$, $A_n = \overline{OE} = \overline{WE} \geq V_{CC} - 0.2\text{V}$, $D_m \leq 0.2\text{V}$ or $\geq V_{CC} - 0.2\text{V}$			18	mA
RBATT	Battery series resistor		94	100	106	k Ω
RWP	WP pull-up resistor		45	51	57	k Ω

Note 5 : Currents flowing into the IC card are taken as positive.

6 : Typical values are measured at $V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$.

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CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
C _I	Input capacitance	V _I = GND, v _i = 25mVrms, f = 1 MHz, T _a = 25°C	1 MB			pF
			2 MB		45	
C _O	Output capacitance	V _O = GND, v _o = 25mVrms, f = 1 MHz, T _a = 25°C	1 MB			pF
			2 MB		30	

Note 7 : These parameters are not 100% tested.

SWITCHING CHARACTERISTICS

Read Cycle (T_a = 0 ~ 50°C, V_{CC} = 4.5 ~ 5.5V, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t _{CR}	Read cycle time	200			ns
t _{a(A)}	Address access time			200	ns
t _{a(CE)}	Card select access time			200	ns
t _{a(OE)}	Output enable access time			100	ns
t _{dis(CE)}	Output disable time (from \overline{CE})			70	ns
t _{dis(OE)}	Output disable time (from \overline{OE})			70	ns
t _{en(CE)}	Output enable time (from \overline{CE})	5			ns
t _{en(OE)}	Output enable time (from \overline{OE})	5			ns
t _{V(A)}	Data valid time (after address)	10			ns

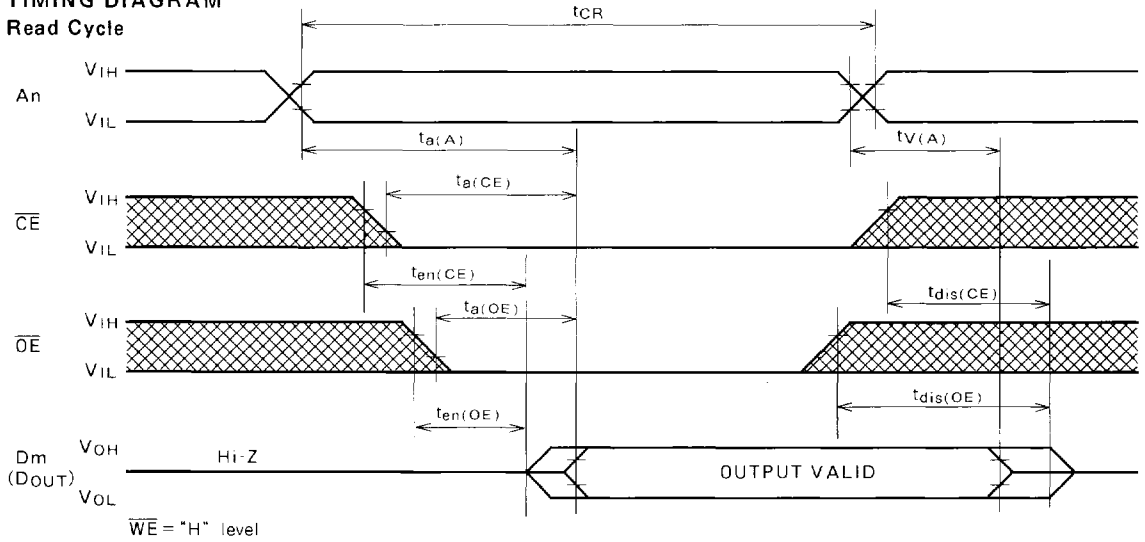
TIMING REQUIREMENTS


Write Cycle (T_a = 0 ~ 55°C, V_{CC} = 4.5 ~ 5.5V, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t _{CW}	Write cycle time	200			ns
t _{w(WE)}	Write pulse width	120			ns
t _{SU(A)}	Address setup time	20			ns
t _{SU(A-WEH)}	Address setup time before write pulse rise	140			ns
t _{SU(CE)}	Card select setup time	120			ns
t _{SU(D)}	Data setup time	60			ns
t _{h(D)}	Data hold time	30			ns
t _{rec(WE)}	Write recovery time	30			ns
t _{dis(OE)}	Output disable time (from \overline{OE})			70	ns
t _{en(OE)}	Output enable time (from \overline{OE})	5			ns

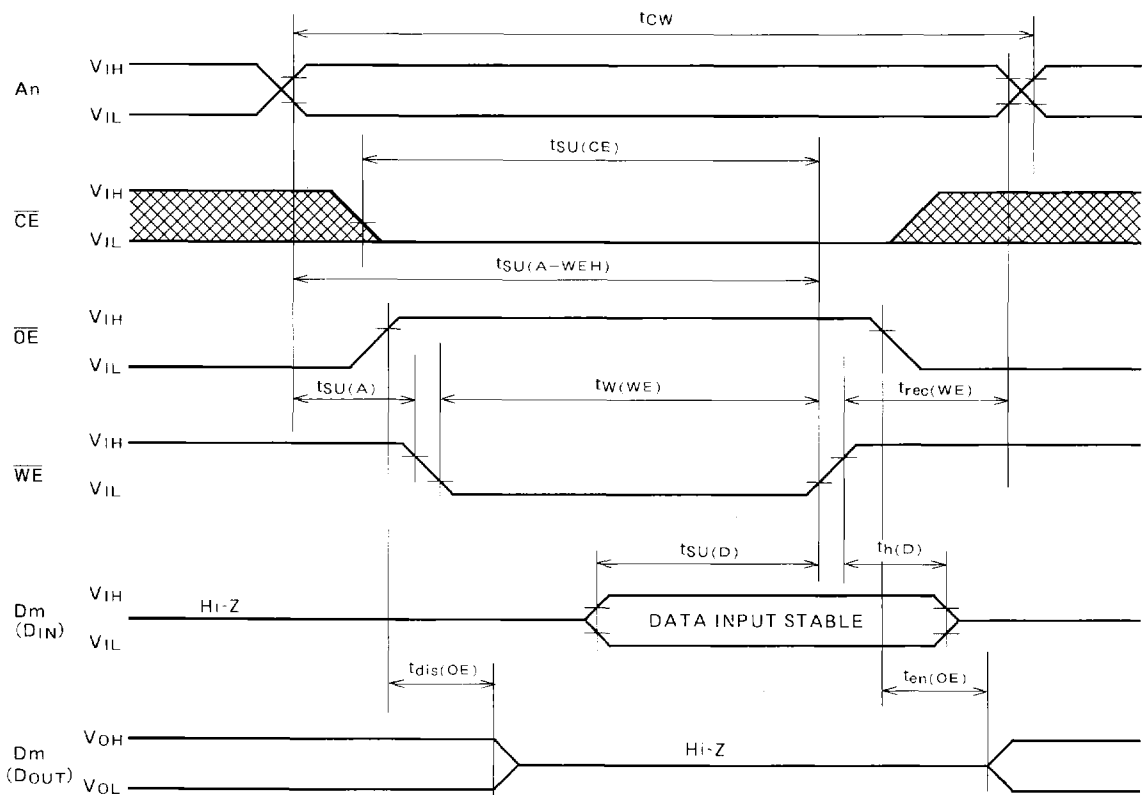
TIMING DIAGRAM

Read Cycle



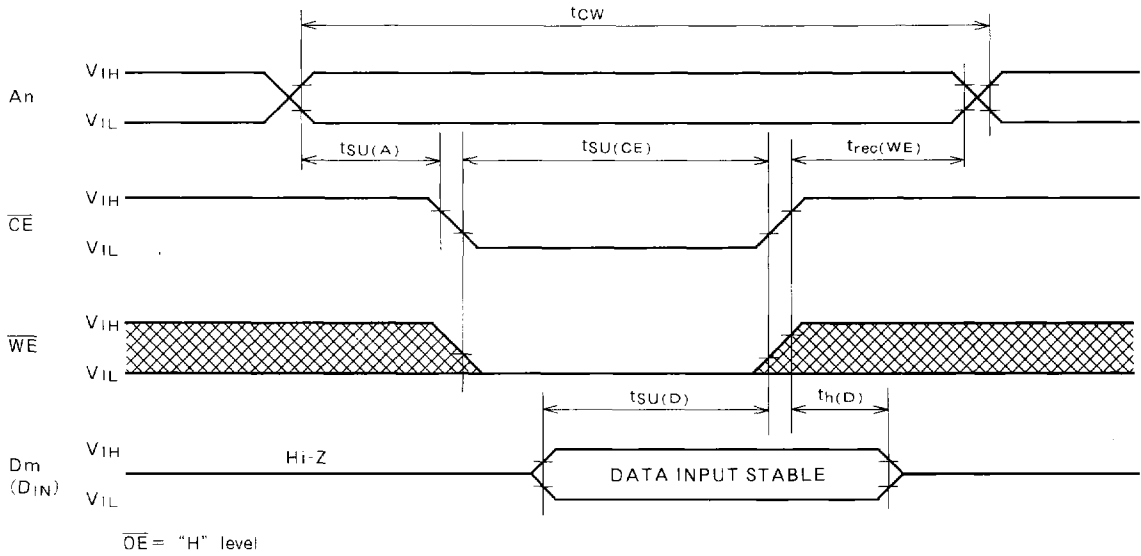
Note 8 :  Indicates the don't care input.

Write Cycle (\overline{WE} control)



TIMING DIAGRAM

Write Cycle (\overline{CE} control)



Note 9 : Test Conditions

Input pulse levels : $V_{IL}=0.4V$, $V_{IH}=0.8 \times V_{CC} V$

Input pulse rise, fall time : $t_r=t_f=10ns$

Reference voltage

Input : $V_{IL}=0.8V$, $V_{IH}=0.7 \times V_{CC} V$

Output : $V_{OL}=0.8V$, $V_{OH}=2.0V$

(t_{en} and t_{dis} are measured when output voltage is $\pm 500mV$ from steady state.)

Load : 100pF + 1 TTL gate

5 pF + 1 TTL gate (at t_{en} and t_{dis} measuring)

10 : The data write is performed during the interval when both \overline{CE} and \overline{WE} are low "L" level.

11 : Don't apply inverted phase signal externally when D_m pin is in output mode.

ELECTRICAL CHARACTERISTICS

BATTERY BACKUP ($T_a = 0 \sim 50^\circ C$, unless otherwise noted)

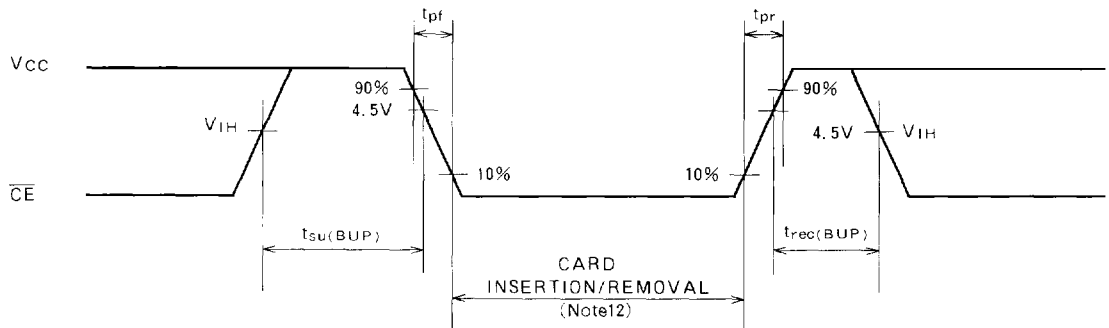
Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{batt}	Back up available voltage	All pins open	2.6			V
$I_{CC(BUP)}$	Battery back up supply current	All pins open, $V_{batt} = 3V$, $T_a = 25^\circ C$	1 MB		9	μA
			2 MB		17	

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TIMING REQUIREMENTS ($T_a = 0 \sim 50^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{pr}	Power supply rise time			20	ms
t_{pf}	Power supply fall time			20	ms
$t_{su(BPU)}$	Battery back up setup time	1			μs
$t_{rec(BPU)}$	Battery back up recovery time	20			ms

TIMING DIAGRAM



Note 12 : The battery must not be removed unless V_{CC} is present, otherwise all data will be lost.

BATTERY SPECIFICATIONS

A replaceable battery (type BR2325) with a capacity of 165mAH is used ;
 Estimated battery life.

MF31M 0 - MXXXXXX	2.0years
MF32M 0 - MXXXXXX	1.1years

Note 13 : Conditions Temperature : 25°C
 Humidity : 60%RH