

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

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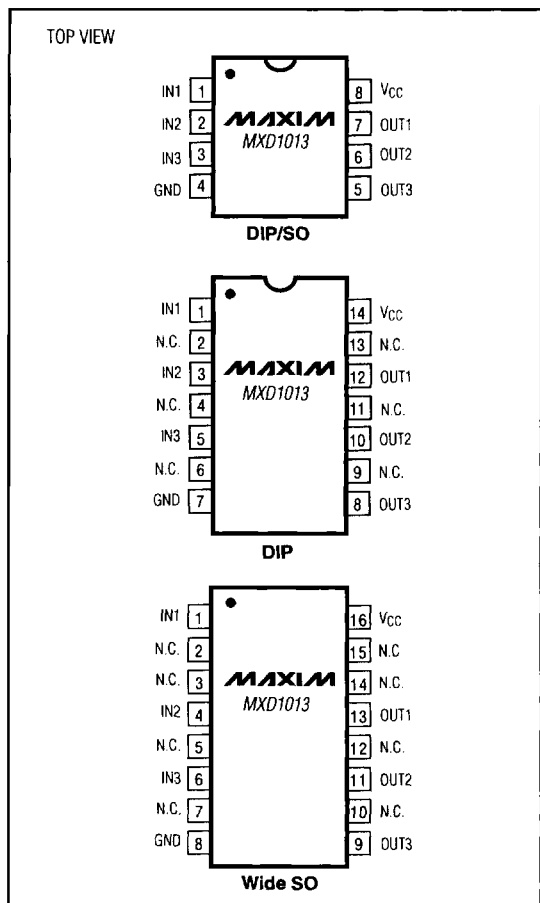
Three-in-One Silicon Delay Line

General Description

The MXD1013 silicon delay line offers three independent logic-buffered delays in a single package. Each provides a nominal accuracy of $\pm 2\text{ns}$ for delay times between 10ns and 75ns, increasing to 5% for delays of 150ns. The MXD1013 reproduces the input logic level at the output after a fixed delay (see *Delay Table*). The part is designed to reproduce leading and trailing edges with equal precision. Each output is capable of driving up to ten 74LS loads.

Maxim can customize standard delays to meet special needs.

Pin Configurations



Features

- ♦ Delay Tolerances $\pm 2\text{ns}$
- ♦ Stability and Precision Over Temperature and Supply Voltage
- ♦ Leading and Trailing Edge Accuracy
- ♦ Custom Delays Available
- ♦ TTL/CMOS Compatible

Ordering Information

PART**	TEMP. RANGE	PIN-PACKAGE
MXD1013-__CPA	0°C to +70°C	8 Plastic DIP
MXD1013-__CPD	0°C to +70°C	14 Plastic DIP
MXD1013-__CSA	0°C to +70°C	8 SO
MXD1013-__CWE	0°C to +70°C	16 Wide SO
MXD1013-__C/D	0°C to +70°C	Dice*
MXD1013-__EPA	-40°C to +85°C	8 Plastic DIP
MXD1013-__EPD	-40°C to +85°C	14 Plastic DIP
MXD1013-__ESA	-40°C to +85°C	8 SO
MXD1013-__EWE	-40°C to +85°C	16 Wide SO

* Contact factory for dice specifications.

** To complete the part number, simply consult the Delay Table, select the part-number extension corresponding to the desired delay times, and fill-in the blank in the Ordering Information.

Delay Table (tPHL, tPLH)

PART NO. EXTENSION	DELAY PER OUTPUT (ns)
10	10/10/10
12	12/12/12
15	15/15/15
20	20/20/20
25	25/25/25
30	30/30/30
35	35/35/35
40	40/40/40
45	45/45/45
50	50/50/50
55	55/55/55
60	60/60/60
65	65/65/65
70	70/70/70
75	75/75/75
80*	80/80/80
90*	90/90/90
100*	100/100/100
150**	150/150/150

Custom delays available.

* $\pm 3\%$ tolerance. ** $\pm 5\%$ tolerance.

MXD1013

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Maxim Integrated Products 10-21

Call toll free 1-800-998-8800 for free samples or literature.

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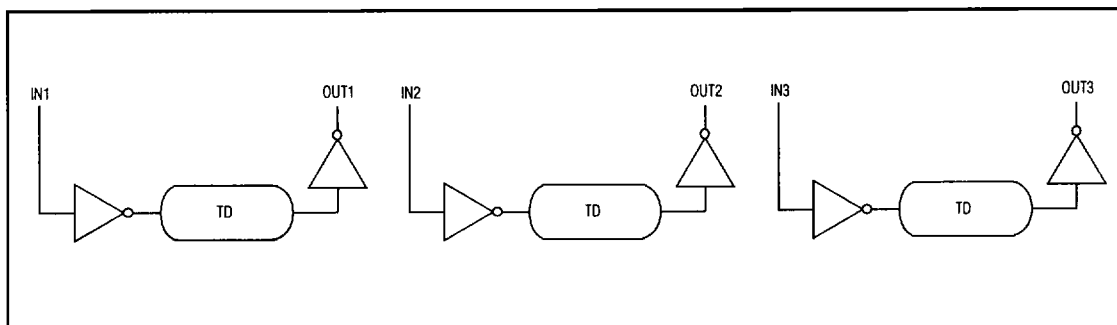


Figure 1. Logic Diagram