

## Direct RDRAM RIMM Modules (with 144 Mbit RDRAMs)

### Overview

The Direct Rambus™ RIMM™ module is a general purpose high-performance memory subsystem suitable for use in a broad range of applications including computer memory, personal computers, workstations, and other applications where high bandwidth and low latency are required.

The Direct Rambus RIMM module consists of 144 Mbit Direct Rambus DRAM (Direct RDRAM™) devices. These are extremely high-speed CMOS DRAMs organized as 8M words by 18 bits. The use of Rambus Signaling Level (RSL) technology permits 600 MHz to 800 MHz transfer rates while using conventional system and board design technologies. Direct RDRAM devices are capable of sustained data transfers at 1.25 ns per two bytes (10 ns per sixteen bytes).

The RDRAM architecture enables the highest sustained bandwidth for multiple, simultaneous, randomly addressed, memory transactions. The separate control and data buses with independent row and column control yield over 95% bus efficiency. The RDRAM's 32-bank architecture supports up to four simultaneous transactions per device.

### Form Factor

The Rambus RIMM modules are offered in a 184-pad 1 mm edge connector pad pitch form factor suitable for 184 contact RIMM connectors. The RIMM module is suitable for desktop and other system applications. The next figure shows an eight device Rambus RIMM module without heat spreader.

### Features

- High speed 800, 711 & 600 MHz RDRAM storage
- 184 edge connector pads with 1 mm pad spacing
- Maximum module PCB size:  
133.5 mm × 31.75 mm × 1.37 mm  
(5.25" × 1.25" × 0.05")
- Each RDRAM has 32 banks, for a total of  
512, 256 or 128 banks on each 256/288 MB,  
128/144MB or 64/72 MB module  
respectively.
- Gold plated edge connector pad contacts
- Serial Presence Detect (SPD) support
- Operates from a 2.5 V supply ( $\pm 5\%$ )
- Low power and powerdown self refresh modes
- Separate Row and Column buses for higher efficiency

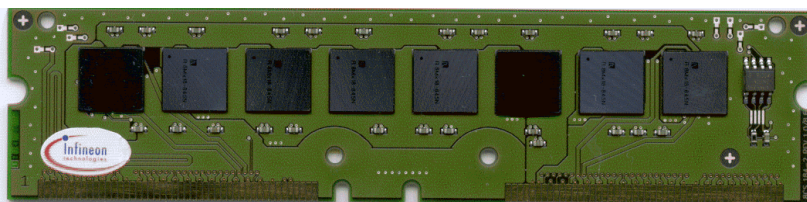


Fig.1 : Rambus RIMM module  
(without heat spreader)

## Part Number Designators

| Organization  | Capacity | I/O Frequency [MHz] | Part Designator | # of RDRAMs | RDRAM Density |
|---------------|----------|---------------------|-----------------|-------------|---------------|
| 64 MB/72 MB   |          |                     |                 |             |               |
| 32 MB × 16    | 64 MB    | 600                 | HYR163220G-653  | 4           | 144 Mbit      |
| 32 MB × 16    | 64 MB    | 711                 | HYR163220G-745  | 4           |               |
| 32 MB × 16    | 64 MB    | 800                 | HYR163220G-845  | 4           |               |
| 32 MB × 16    | 64 MB    | 800                 | HYR163220G-840  | 4           |               |
| 32 MB × 18    | 72 MB    | 600                 | HYR183220G-653  | 4           |               |
| 32 MB × 18    | 72 MB    | 711                 | HYR183220G-745  | 4           |               |
| 32 MB × 18    | 72 MB    | 800                 | HYR183220G-845  | 4           |               |
| 32 MB × 18    | 72 MB    | 800                 | HYR183220G-840  | 4           |               |
| 128 MB/144 MB |          |                     |                 |             |               |
| 64 MB × 16    | 128 MB   | 600                 | HYR166420G-653  | 8           | 144 Mbit      |
| 64 MB × 16    | 128 MB   | 711                 | HYR166420G-745  | 8           |               |
| 64 MB × 16    | 128 MB   | 800                 | HYR166420G-845  | 8           |               |
| 64 MB × 16    | 128 MB   | 800                 | HYR166420G-840  | 8           |               |
| 64 MB × 18    | 144 MB   | 600                 | HYR186420G-653  | 8           |               |
| 64 MB × 18    | 144 MB   | 711                 | HYR186420G-745  | 8           |               |
| 64 MB × 18    | 144 MB   | 800                 | HYR186420G-845  | 8           |               |
| 64 MB × 18    | 144 MB   | 800                 | HYR186420G-840  | 8           |               |
| 256 MB/288 MB |          |                     |                 |             |               |
| 128 MB × 16   | 256 MB   | 600                 | HYR1612820G-653 | 16          | 144 Mbit      |
| 128 MB × 16   | 256 MB   | 711                 | HYR1612820G-745 | 16          |               |
| 128 MB × 16   | 256 MB   | 800                 | HYR1612820G-845 | 16          |               |
| 128 MB × 16   | 256 MB   | 800                 | HYR1612820G-840 | 16          |               |
| 128 MB × 18   | 288 MB   | 600                 | HYR1812820G-653 | 16          |               |
| 128 MB × 18   | 288 MB   | 711                 | HYR1812820G-745 | 16          |               |
| 128 MB × 18   | 288 MB   | 800                 | HYR1812820G-845 | 16          |               |
| 128 MB × 18   | 288 MB   | 800                 | HYR1812820G-840 | 16          |               |

## Pin Configuration

| PIN | Pin Name | PIN | Pin Name | PIN | Pin Name         | PIN | Pin Name         |
|-----|----------|-----|----------|-----|------------------|-----|------------------|
| A1  | GND      | B1  | GND      | A47 | N.C.             | B47 | N.C.             |
| A2  | LDQA8    | B2  | LDQA7    | A48 | N.C.             | B48 | N.C.             |
| A3  | GND      | B3  | GND      | A48 | N.C.             | B49 | N.C.             |
| A4  | LDQA6    | B4  | LDQA5    | A50 | N.C.             | B50 | N.C.             |
| A5  | GND      | B5  | GND      | A51 | V <sub>REF</sub> | B51 | V <sub>REF</sub> |
| A6  | LDQA4    | B6  | LDQA3    | A52 | GND              | B52 | GND              |
| A7  | GND      | B7  | GND      | A53 | SCL              | B53 | SA0              |
| A8  | LDQA2    | B8  | LDQA1    | A54 | V <sub>DD</sub>  | B54 | V <sub>DD</sub>  |
| A9  | GND      | B9  | GND      | A55 | SDA              | B55 | SA1              |
| A10 | LDQA0    | B10 | LCFM     | A56 | SVdd             | B56 | SVdd             |
| A11 | GND      | B11 | GND      | A57 | SWP              | B57 | SA2              |
| A12 | LCTMN    | B12 | LCFMN    | A58 | V <sub>DD</sub>  | B58 | V <sub>DD</sub>  |
| A13 | GND      | B13 | GND      | A59 | RSCK             | B59 | RCMD             |
| A14 | LCTM     | B14 | N.C.     | A60 | GND              | B60 | GND              |
| A15 | GND      | B15 | GND      | A61 | RDQB7            | B61 | RDQB8            |
| A16 | N.C.     | B16 | LROW2    | A62 | GND              | B62 | GND              |
| A17 | GND      | B17 | GND      | A63 | RDQB5            | B63 | RDQB6            |
| A18 | LROW1    | B18 | LROW0    | A64 | GND              | B64 | GND              |
| A19 | GND      | B19 | GND      | A65 | RDQB3            | B65 | RDQB4            |
| A20 | LCOL4    | B20 | LCOL3    | A66 | GND              | B66 | GND              |
| A21 | GND      | B21 | GND      | A67 | RDQB1            | B67 | RDQB2            |
| A22 | LCOL2    | B22 | LCOL1    | A68 | GND              | B68 | GND              |
| A23 | GND      | B23 | GND      | A69 | RCOL0            | B69 | RDQB0            |
| A24 | LCOL0    | B24 | LDQB0    | A70 | GND              | B70 | GND              |
| A25 | GND      | B25 | GND      | A71 | RCOL2            | B71 | RCOL1            |
| A26 | LDQB1    | B26 | LDQB2    | A72 | GND              | B72 | GND              |
| A27 | GND      | B27 | GND      | A73 | RCOL4            | B73 | RCOL3            |
| A28 | LDQB3    | B28 | LDQB4    | A74 | GND              | B74 | GND              |
| A29 | GND      | B29 | GND      | A75 | RROW1            | B75 | RROW0            |
| A30 | LDQB5    | B30 | LDQB6    | A76 | GND              | B76 | GND              |
| A31 | GND      | B31 | GND      | A77 | N.C.             | B77 | RROW2            |
| A32 | LDQB7    | B32 | LDQB8    | A78 | GND              | B78 | GND              |
| A33 | GND      | B33 | GND      | A79 | RCTM             | B79 | N.C.             |

## Pin Configuration (cont'd)

| PIN | Pin Name          | PIN | Pin Name          | PIN | Pin Name | PIN | Pin Name |
|-----|-------------------|-----|-------------------|-----|----------|-----|----------|
| A34 | LSCK              | B34 | LCMD              | A80 | GND      | B80 | GND      |
| A35 | $V_{\text{CMOS}}$ | B35 | $V_{\text{CMOS}}$ | A81 | RCTMN    | B81 | RCFMN    |
| A36 | SOUT              | B36 | SIN               | A82 | GND      | B82 | GND      |
| A37 | $V_{\text{CMOS}}$ | B37 | $V_{\text{CMOS}}$ | A83 | RDQA0    | B83 | RCFM     |
| A38 | N.C.              | B38 | N.C.              | A84 | GND      | B84 | GND      |
| A39 | GND               | B39 | GND               | A85 | RDQA2    | B85 | RDQA1    |
| A40 | N.C.              | B40 | N.C.              | A86 | GND      | B86 | GND      |
| A41 | $V_{\text{DD}}$   | B41 | $V_{\text{DD}}$   | A87 | RDQA4    | B87 | RDQA3    |
| A42 | $V_{\text{DD}}$   | B42 | $V_{\text{DD}}$   | A88 | GND      | B88 | GND      |
| A43 | N.C.              | B43 | N.C.              | A89 | RDQA6    | B89 | RDQA5    |
| A44 | N.C.              | B44 | N.C.              | A90 | GND      | B90 | GND      |
| A45 | N.C.              | B45 | N.C.              | A91 | RDQA8    | B91 | RDQA7    |
| A46 | N.C.              | B46 | N.C.              | A92 | GND      | B92 | GND      |

## Module Connector Pad Description

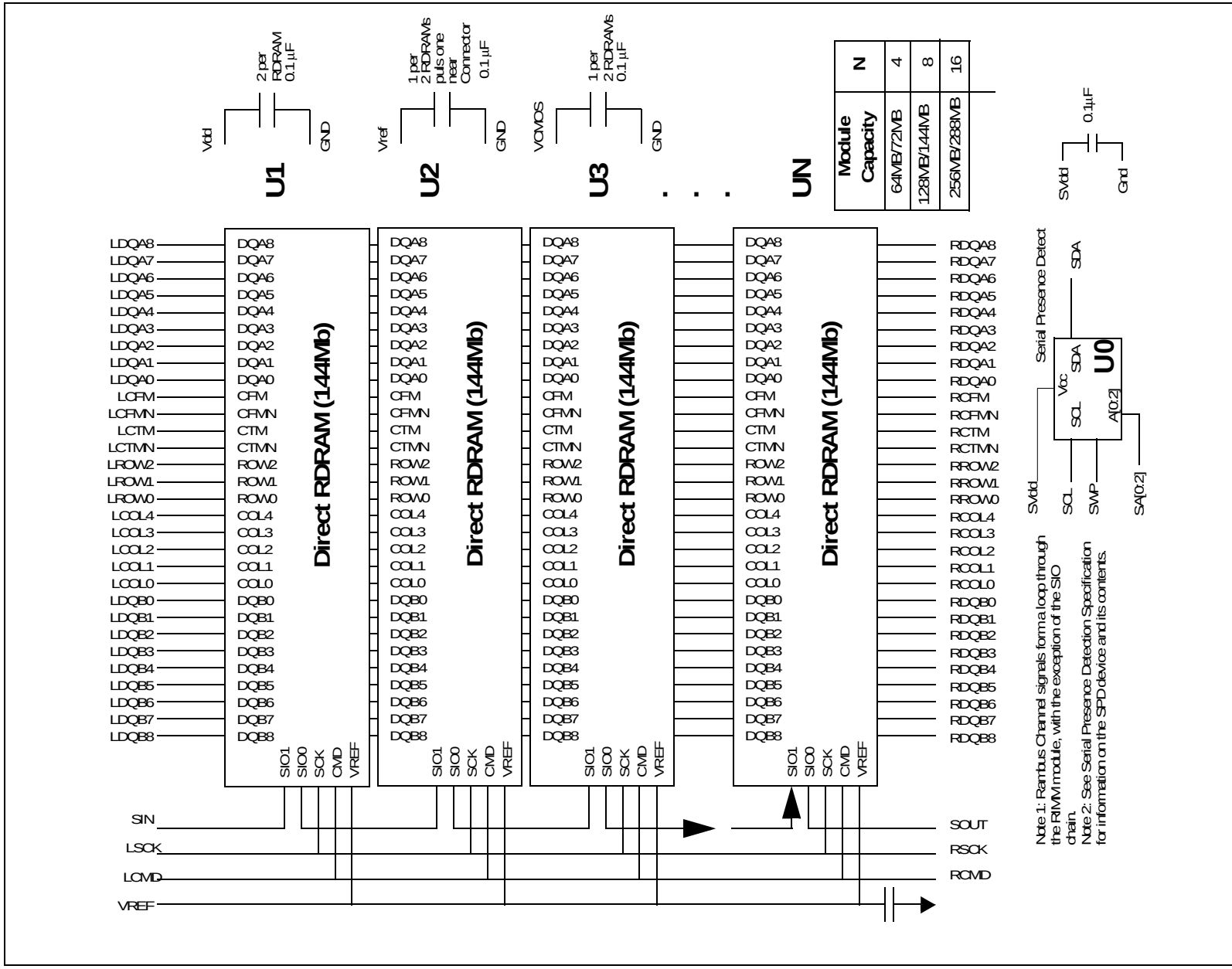
| Signal             | Module Connector Pads                                                                                                                                                                                                                                                                                                                                        | I/O | Type              | Description                                                                                                                                                 |
|--------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| GND                | A1, A3, A5, A7, A9, A11, A13, A15, A17, A19, A21, A23, A25, A27, A29, A31, A33, A39, A52, A60, A62, A64, A66, A68, A70, A72, A74, A76, A78, A80, A82, A84, A86, A88, A90, A92, B1, B3, B5, B7, B9, B11, B13, B15, B17, B19, B21, B23, B25, B27, B29, B31, B33, B39, B52, B60, B62, B64, B66, B68, B70, B72, B74, B76, B78, B80, B82, B84, B86, B88, B90, B92 | –   | –                 | Ground reference for RDRAM core and interface. 72 PCB connector pads.                                                                                       |
| LCFM               | B10                                                                                                                                                                                                                                                                                                                                                          | I   | RSL               | Clock from master. Interface clock used for receiving RSL signals from the Channel. Positive polarity.                                                      |
| LCFMN              | B12                                                                                                                                                                                                                                                                                                                                                          | I   | RSL               | Clock from master. Interface clock used for receiving RSL signals from the Channel. Negative polarity.                                                      |
| LCMD               | B34                                                                                                                                                                                                                                                                                                                                                          | I   | V <sub>CMOS</sub> | Serial Command used to read from and write to the control registers. Also used for power management.                                                        |
| LCOL4 ...<br>LCOL0 | A20, B20, A22, B22, A24                                                                                                                                                                                                                                                                                                                                      | I   | RSL               | Column bus. 5-bit bus containing control and address information for column accesses.                                                                       |
| LCTM               | A14                                                                                                                                                                                                                                                                                                                                                          | I   | RSL               | Clock to master. Interface clock used for transmitting RSL signals to the Channel. Positive polarity.                                                       |
| LCTMN              | A12                                                                                                                                                                                                                                                                                                                                                          | I   | RSL               | Clock to master. Interface clock used for transmitting RSL signals to the Channel. Negative polarity.                                                       |
| LDQA8 ...<br>LDQA0 | A2, B2, A4, B4, A6, B6, A8, B8, A10                                                                                                                                                                                                                                                                                                                          | I/O | RSL               | Data bus A. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. LDQA8 is non-functional on modules with x16 RDRAM devices. |

## Module Connector Pad Description (cont'd)

| Signal             | Module Connector Pads                                                                                                              | I/O | Type              | Description                                                                                                                                                 |
|--------------------|------------------------------------------------------------------------------------------------------------------------------------|-----|-------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LDQB8 ...<br>LDQB0 | B32, A32, B30, A30, B28,<br>A28, B26, A26, B24                                                                                     | I/O | RSL               | Data bus B. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. LDQB8 is non-functional on modules with x16 RDRAM devices. |
| LROW2 ...<br>LROW0 | B16, A18, B18                                                                                                                      | I   | RSL               | Row bus. 3-bit bus containing control and address information for row accesses.                                                                             |
| LSCK               | A34                                                                                                                                | I   | V <sub>CMOS</sub> | Serial Clock input. Clock source used to read from and write to the RDRAM control registers.                                                                |
| N.C.               | A16, B14, A38, B38, A40,<br>B40, A77, B79; A43, B43,<br>A44, B44, A45, B45, A46,<br>B46, A47, B47, A48, B48,<br>A49, B49, A50, B50 | —   | —                 | These pads are not connected. These connector pads are reserved for future use.                                                                             |
| RCFM               | B83                                                                                                                                | I   | RSL               | Clock from master. Interface clock used for receiving RSL signals from the Channel. Positive polarity.                                                      |
| RCFMN              | B81                                                                                                                                | I   | RSL               | Clock from master. Interface clock used for receiving RSL signals from the Channel. Negative polarity.                                                      |
| RCMD               | B59                                                                                                                                | I   | V <sub>CMOS</sub> | Serial Command Input used to read from and write to the control registers. Also used for power management.                                                  |
| RCOL4 ...<br>RCOL0 | A73, B73, A71, B71, A69                                                                                                            | I   | RSL               | Column bus. 5-bit bus containing control and address information for column accesses.                                                                       |
| RCTM               | A79                                                                                                                                | I   | RSL               | Clock to master. Interface clock used for transmitting RSL signals to the Channel. Positive polarity.                                                       |
| RCTMN              | A81                                                                                                                                | I   | RSL               | Clock to master. Interface clock used for transmitting RSL signals to the Channel. Negative polarity.                                                       |
| RDQA8 ...<br>RDQA0 | A91, B91, A89, B89, A87,<br>B87, A85, B85, A83                                                                                     | I/O | RSL               | Data bus A. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. RDQA8 is non-functional on modules with x16 RDRAM devices. |

## Module Connector Pad Description (cont'd)

| Signal             | Module Connector Pads                          | I/O | Type              | Description                                                                                                                                                 |
|--------------------|------------------------------------------------|-----|-------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RDQB8 ...<br>RDQB0 | B61, A61, B63, A63, B65,<br>A65, B67, A67, B69 | I/O | RSL               | Data bus B. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. RDQB8 is non-functional on modules with x16 RDRAM devices. |
| RROW2 ...<br>RROW0 | B77, A75, B75                                  | I   | RSL               | Row bus. 3-bit bus containing control and address information for row accesses.                                                                             |
| RSCK               | A59                                            | I   | V <sub>CMOS</sub> | Serial Clock input. Clock source used to read from and write to the RDRAM control registers.                                                                |
| SA0                | B53                                            | I   | SVDD              | Serial Presence Detect Address 0.                                                                                                                           |
| SA1                | B55                                            | I   | SVDD              | Serial Presence Detect Address 1.                                                                                                                           |
| SA2                | B57                                            | I   | SVDD              | Serial Presence Detect Address 2.                                                                                                                           |
| SCL                | A53                                            | I   | SVDD              | Serial Presence Detect Clock.                                                                                                                               |
| SDA                | A55                                            | I/O | SVDD              | Serial Presence Detect Data (Open Collector I/O).                                                                                                           |
| SIN                | B36                                            | I/O | V <sub>CMOS</sub> | Serial I/O for reading from and writing to the control registers. Attaches to SIO0 of the first RDRAM on the module.                                        |
| SOUT               | A36                                            | I/O | V <sub>CMOS</sub> | Serial I/O for reading from and writing to the control registers. Attaches to SIO1 of the last RDRAM on the module.                                         |
| SVDD               | A56, B56                                       | –   | –                 | SPD Voltage. Used for signals SCL, SDA, SWE, SA0, SA1 and SA2.                                                                                              |
| SWP                | A57                                            | I   | SVDD              | Serial Presence Detect Write Protect (active high). When low, the SPD can be written as well as read.                                                       |
| V <sub>CMOS</sub>  | A35, B35, A37, B37                             | –   | –                 | CMOS I/O Voltage. Used for signals CMD, SCK, SIN, SOUT.                                                                                                     |
| V <sub>DD</sub>    | A41, A42, A54, A58, B41,<br>B42, B54, B58      | –   | –                 | Supply voltage for the RDRAM core and interface logic.                                                                                                      |
| V <sub>REF</sub>   | A51, B51                                       | –   | –                 | Logic threshold reference voltage for RSL signals.                                                                                                          |



RIMM Module Functional Diagram

## Absolute Maximum Ratings

| Symbol       | Parameter                                                         | Limit Values |                | Unit |
|--------------|-------------------------------------------------------------------|--------------|----------------|------|
|              |                                                                   | min.         | max.           |      |
| $V_{I,ABS}$  | Voltage applied to any RSL or CMOS signal pad with respect to GND | - 0.3        | $V_{DD} + 0.3$ | V    |
| $V_{DD,ABS}$ | Voltage on $V_{DD}$ with respect to GND                           | - 0.5        | $V_{DD} + 1.0$ | V    |
| $T_{STORE}$  | Storage temperature                                               | - 50         | 100            | °C   |

## DC Recommended Electrical Conditions

| Symbol         | Parameter and Conditions                                          | Limit Values                    |                               | Unit |
|----------------|-------------------------------------------------------------------|---------------------------------|-------------------------------|------|
|                |                                                                   | min.                            | max.                          |      |
| $V_{DD}$       | Supply voltage                                                    | 2.50 - 0.13                     | 2.50 + 0.13                   | V    |
| $V_{CMOS}$     | CMOS I/O power supply at pad for 2.5 V controllers:               | 2.5 - 0.13                      | 2.5 + 0.25                    | V    |
|                | CMOS I/O power supply at pad for 1.8 V controllers:               | 1.8 - 0.1                       | 1.8 + 0.2                     | V    |
| $V_{REF}$      | Reference voltage                                                 | 1.4 - 0.2                       | 1.4 + 0.2                     | V    |
| $V_{IL}$       | RSL input low voltage                                             | $V_{REF} - 0.5$                 | $V_{REF} - 0.2$               | V    |
| $V_{IH}$       | RSL input high voltage                                            | $V_{REF} + 0.2$                 | $V_{REF} + 0.5$               | V    |
| $V_{IL,CMOS}$  | CMOS input low voltage                                            | - 0.3                           | $0.5 V_{CMOS} - 0.25$         | V    |
| $V_{IH,CMOS}$  | CMOS input high voltage                                           | $0.5 V_{CMOS} + 0.25$           | $V_{CMOS} + 0.7$              | V    |
| $V_{OL,CMOS}$  | CMOS output low voltage @<br>$I_{OL,CMOS} = 1 \text{ mA}$         | -                               | 0.3                           | V    |
| $V_{OH,CMOS}$  | CMOS output high voltage @<br>$I_{OH,CMOS} = - 0.25 \text{ mA}$   | $V_{CMOS} - 0.3$                | -                             | V    |
| $I_{REF}$      | $V_{REF}$ current @ $V_{REF,MAX}$                                 | - 10 × no. RDRAMs <sup>1)</sup> | 10 × no. RDRAMs <sup>1)</sup> | μA   |
| $I_{SCK,CMD}$  | CMOS input leakage current @<br>( $0 \leq V_{CMOS} \leq V_{DD}$ ) | - 10 × no. RDRAMs <sup>1)</sup> | 10 × no. RDRAMs <sup>1)</sup> | μA   |
| $I_{SIN,SOUT}$ | CMOS input leakage current @<br>( $0 \leq V_{CMOS} \leq V_{DD}$ ) | - 10.0                          | 10.0                          | μA   |

1) The table below shows the number of RDRAM devices contained in a RIMM module of listed memory storage capacity.

| RIMM Module Capacity             | 64/72 MB | 128/144 MB | 256/288 MB |
|----------------------------------|----------|------------|------------|
| Number of 144 Mbit RDRAM devices | 4        | 8          | 16         |

## AC Electrical Specifications

| Symbol               | Parameter and Conditions                                                                                | Limit Values |      |                         | Unit |
|----------------------|---------------------------------------------------------------------------------------------------------|--------------|------|-------------------------|------|
|                      |                                                                                                         | min.         | typ. | max.                    |      |
| Z                    | Module Impedance                                                                                        | 25.2         | 28   | 30.8                    | Ω    |
| $T_{PD}$             | Average clock delay from finger of all RSL clock nets (CTM, CTMN, CFM and CFMN)                         | –            | –    | See Table <sup>1)</sup> | ns   |
| $\Delta T_{PD}$      | Propagation delay variation of RSL signals with respect to $T_{PD}^{2)3)}$ for 4 and 8 device modules   | – 21         | –    | 21                      | ps   |
|                      | Propagation delay variation of RSL signals with respect to $T_{PD}^{2)3)}$ for 16 device modules        | – 24         | –    | 24                      | ps   |
| $\Delta T_{PD-CMOS}$ | Propagation delay variation of SCK and CMD signals with respect to an average clock delay <sup>2)</sup> | – 100        | –    | 100                     | ps   |
| $V_A/V_{IN}$         | Attenuation Limit                                                                                       | –            | –    | See Table <sup>1)</sup> | %    |
| $V_{XF}/V_{IN}$      | Forward crosstalk coefficient (300 ps input rise time @ 20%-80%)                                        | –            | –    | See Table <sup>1)</sup> | %    |
| $V_{XB}/V_{IN}$      | Backward crosstalk coefficient (300 ps input rise time @ 20%-80%)                                       | –            | –    | See Table <sup>1)</sup> | %    |

1) Table below lists parameters and specifications for different storage capacity RIMM Modules that use 144 Mbit RDRAM devices.

2) Average clock delay is defined as the average delay from finger to finger of all RSL clock nets (CTM, CTMN, .....CFM and CFMN).

3.) If the RIMM module meets the following specifications, then it is compliant to the specification. If the RIMM .....module does not meet these specifications, then the specification can be adjusted by the "Adjusted  $\Delta T_{PD}$ - .....Specification" table.

## Adjusted $\Delta T_{PD}$ Specification

| Symbol          | Parameter and Conditions                                                                       | Adjusted Min/Max                            | Absolute Min /Max |    | Unit |
|-----------------|------------------------------------------------------------------------------------------------|---------------------------------------------|-------------------|----|------|
| $\Delta T_{PD}$ | Propagation delay variation of RSL signals with respect to $T_{PD}$ for 4 and 8 device modules | $\pm [17 + (18 \cdot N \cdot \Delta Z0)]^a$ | -30               | 30 | ps   |
|                 | Propagation delay variation of RSL signals with respect to $T_{PD}$ for 16 device modules      | $\pm [24 + (18 \cdot N \cdot \Delta Z0)]$   | -50               | 50 | ps   |

a) Where:

N = Number of RDRAM devices installed on the RIMM module

$\Delta Z0 = \text{delta } Z0\% = (\text{max } Z0 - \text{min } Z0) / (\text{min } Z0)$

(max Z= and min Z0 are obtained from the loaded (high impedance) impedance coupons of all RSL layers on the modules)

## AC Electrical Specifications for RIMM Modules

| Symbol          | RIMM Module Capacity:<br>No. of 144 Mbit RDRAMs:                                    | 64/72 MB<br>4 | 128/144 MB<br>8 | 256/288 MB<br>16 | Unit     |
|-----------------|-------------------------------------------------------------------------------------|---------------|-----------------|------------------|----------|
|                 | Parameter and Conditions for -800, 711& -600 RIMM Modules                           | max.          | max.            | max.             |          |
| $T_{PD}$        | Propagation Delay, all RSL signals -800, -711                                       | 1.25          | 1.50            | 2.06             | ns       |
|                 | Propagation Delay, all RSL signals -600                                             | 1.25          | 1.60            | 2.10             | ns       |
| $V_A/V_{IN}$    | Attenuation Limit -800, -711                                                        | 12            | 16              | 25               | %        |
|                 | Attenuation Limit -600                                                              | 8             | 10              | 21               | %        |
| $V_{XF}/V_{IN}$ | Forward crosstalk coefficient (300 ps input rise time @ 20% - 80%) -800, -711, -600 | 2             | 4               | 8                | %        |
| $V_{XB}/V_{IN}$ | Backward crosstalk coefficient (300 ps input rise time @ 20%-80%) -800, -711, -600  | 1.5           | 2.0             | 2.5              | %        |
| $R_{DC}$        | DC Resistance Limit -800, -711, -600                                                | 0.6           | 0.8             | 1.2              | $\Omega$ |

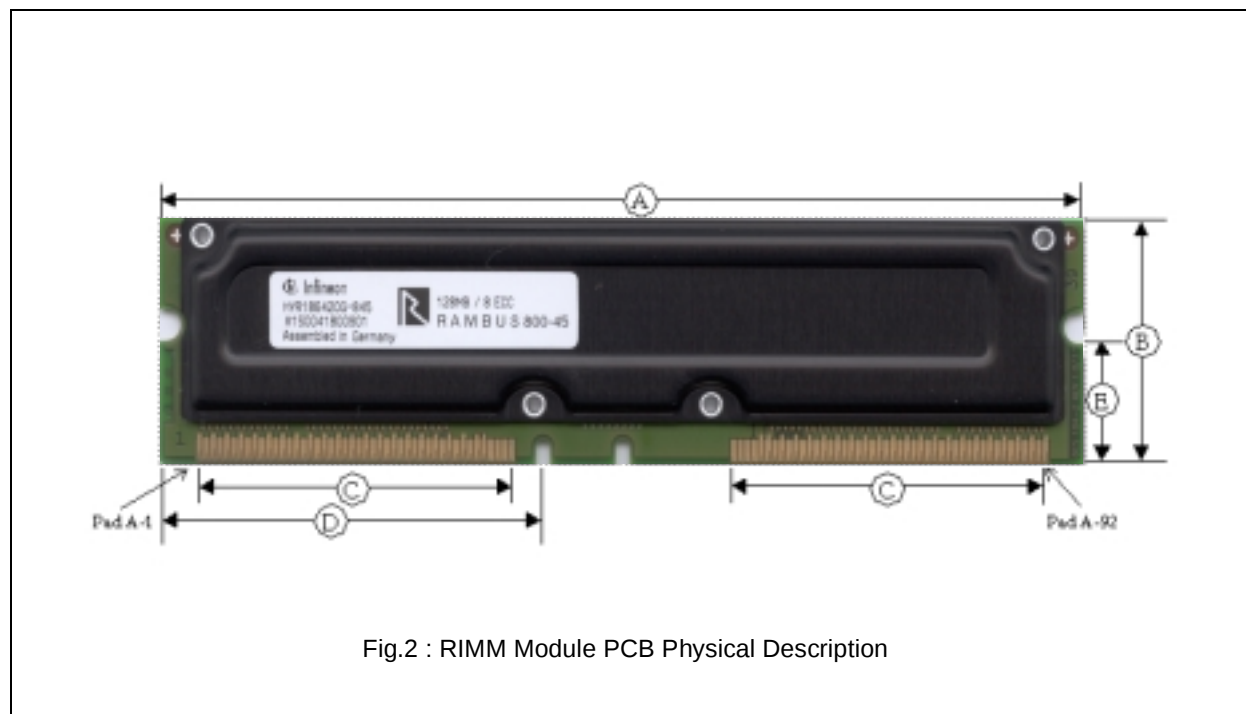
## RIMM Module Current Profile

| $I_{DD}$  | RIMM Module Capacity:<br>No. of 144 Mbit RDRAMs:             |       | 64/72 MB<br>4 | 128/144 MB<br>8 | 256/288 MB<br>16 | Unit |
|-----------|--------------------------------------------------------------|-------|---------------|-----------------|------------------|------|
|           | RIMM Modules Power<br>Conditions <sup>a)</sup>               | Freq. | max.          | max.            | max.             |      |
| $I_{DD1}$ | One RDRAM in Read <sup>b)</sup> ,<br>balance in NAP mode     | -800  | 585           | 600             | 635              | mA   |
|           |                                                              | -711  | 530           | 545             | 580              | mA   |
|           |                                                              | -600  | 460           | 475             | 510              | mA   |
| $I_{DD2}$ | One RDRAM in Read <sup>b)</sup> ,<br>balance in Standby mode | -800  | 875           | 1275            | 2075             | mA   |
|           |                                                              | -711  | 805           | 1185            | 1945             | mA   |
|           |                                                              | -600  | 720           | 1080            | 1800             | mA   |
| $I_{DD3}$ | One RDRAM in Read <sup>b)</sup> ,<br>balance in Active mode  | -800  | 1025          | 1625            | 2825             | mA   |
|           |                                                              | -711  | 955           | 1535            | 2695             | mA   |
|           |                                                              | -600  | 870           | 1430            | 2550             | mA   |
| $I_{DD4}$ | One RDRAM in Write,<br>balance in Active mode                | -800  | 645           | 660             | 695              | mA   |
|           |                                                              | -711  | 580           | 595             | 630              | mA   |
|           |                                                              | -600  | 505           | 520             | 555              | mA   |
| $I_{DD5}$ | One RDRAM in Write,<br>balance in Standby mode               | -800  | 935           | 1335            | 2135             | mA   |
|           |                                                              | -711  | 855           | 1235            | 1995             | mA   |
|           |                                                              | -600  | 765           | 1125            | 1845             | mA   |
| $I_{DD6}$ | One RDRAM in Write,<br>balance in Active mode                | -800  | 1085          | 1685            | 2885             | mA   |
|           |                                                              | -711  | 1005          | 1585            | 2745             | mA   |
|           |                                                              | -600  | 915           | 1475            | 2595             | mA   |

a) Actual power will depend on individual memory controller and usage pattern. Power does not include Refresh Current.

b) I/O power is a function of % 1's to add I/O power for 50% 1's for a x 16 need to add 257mA or 290mA for x18 ECC module for the following:  $V_{DD} = 2.5V$ ,  $V_{TERM} = 1.8V$ ,  $V_{REF} = 1.4V$  and  $V_{DIL} = V_{REF} = 0.5V$ .

The following defines the RIMM module dimensions. All units are in millimeters.

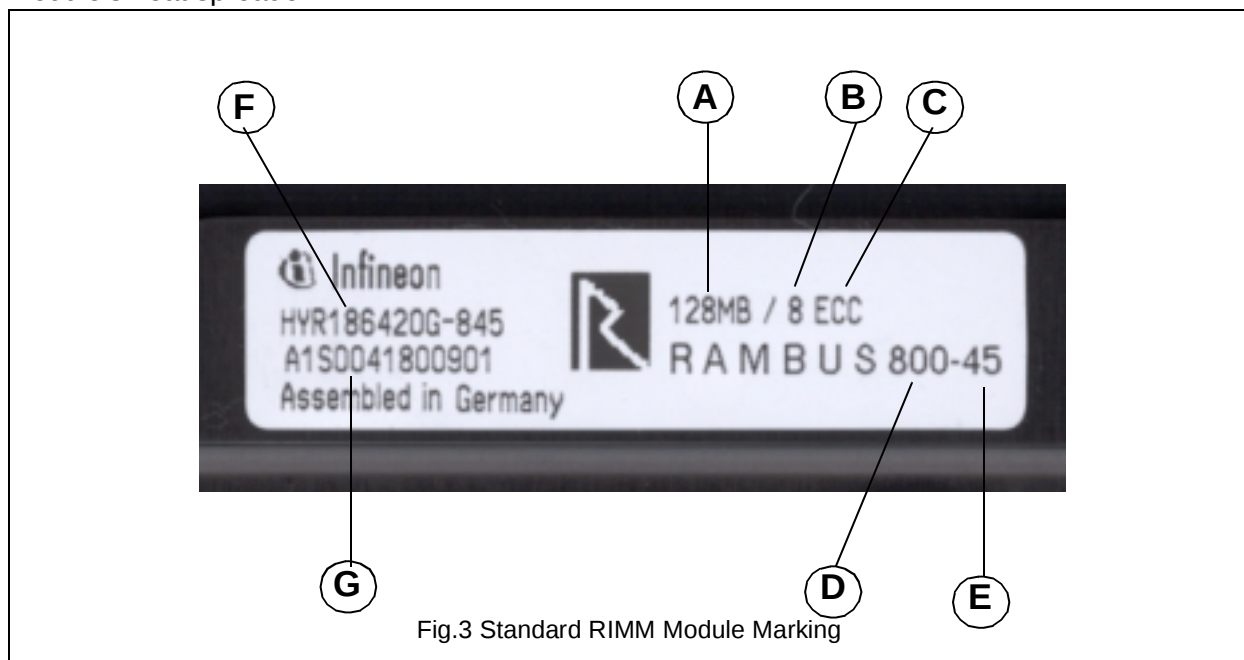


**RIMM Module PCB Physical Description**

| Dimension | Description                                                                      | Limit Values    |                 |                 | Unit     |
|-----------|----------------------------------------------------------------------------------|-----------------|-----------------|-----------------|----------|
|           |                                                                                  | min.            | nom.            | max.            |          |
| A         | PCB length                                                                       | 133.20<br>5.244 | 133.35<br>5.250 | 133.50<br>5.256 | mm<br>in |
| B         | PCB height                                                                       | —               | —               | 31.75<br>1.25   | mm<br>in |
| C         | Center-center pad width from pad A1 to A46, A47 to A92, B1 to B46 or B47 to B92  | —               | —               | 45.00<br>1.770  | mm<br>in |
| D         | Spacing from PCB left edge to connector key notch                                | 55.10<br>2.169  | 55.175<br>2.172 | 55.25<br>2.175  | mm<br>in |
| E         | Spacing from contact pad PCB edge to side edge retainer notch                    | —               | —               | 17.78<br>0.700  | mm<br>in |
| F         | PCB thickness                                                                    | 1.17<br>0.046   | 1.27<br>0.050   | 1.37<br>0.054   | mm<br>in |
| G         | Heat spreader thickness from PCB surface (one side) to heat spreader top surface | —               | —               | 3.02<br>0.119   | mm<br>in |

## Standard RIMM Module Marking

The RIMM modules available from INFINEON Technologies will be marked per Figure 3 below. This marking will help OEMs and users identify the Rambus RIMM modules when used in specific system applications. This will assist OEMs or users to specify and correctly verify if the correct RIMM modules are installed in their systems. In the diagram, a label is shown attached to the RIMM module's heat spreader.



## Standard RIMM Module Marking

|   | Label Field            | Description                                                                    | Marked Text                            | Unit          |
|---|------------------------|--------------------------------------------------------------------------------|----------------------------------------|---------------|
| A | Module Memory Capacity | Number of 8-bit or 9-bit MBytes of RDRAM storage in RIMM module                | 256MB, 128MB, 64MB                     | MB            |
| B | Number of RDRAMs       | Number of RDRAM devices contained in the RIMM module                           | 16, 8, 4                               | RDRAM devices |
| C | ECC Support            | Indicates whether the RIMM module supports 8-bit (no ECC) or 9-bit (ECC) Bytes | blank = 8-bit Byte<br>ECC = 9-bit Byte | –             |
| D | Memory Speed           | Data transfer speed for RDRAM RIMM module                                      | 800, 711, 600                          | MHz           |
| E | $t_{\text{RAC}}$       | Row Access Time                                                                | -45, -53                               | ns            |
| F | Part Number            | INFINEON part number                                                           |                                        |               |
| G | Manufacturing Code     | Date Code etc.                                                                 |                                        |               |

## Attention please !

As far as patents or other rights of third parties are concerned, liability is only assumed for components, not for applications, processes and circuits implemented within components or assemblies. This information describes the type of components and shall not be considered as assured characteristics. Terms of delivery and rights to change design reserved.

For questions on technology, delivery and prices please contact INFINEON Technologies Offices in Munich or the INFINEON Technologies Sales Offices and Representatives worldwide.

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest INFINEON Technologies office or representative.

### Packing

Please use the recycling operators known to you. We can help you - get in touch with your nearest sales office. By agreement we will take packing material back, if it is sorted. You must bear the costs of transport. For packing material that is returned to us unsorted or which we are not obliged to accept, we shall have to invoice you for any costs incurred.

### **Components used in life-support devices or systems must be expressly authorized for such purpose!**

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