54AC/74AC299 • 54ACT/74ACT299

8-Input Universal Shift/Storage Register With Common Parallel I/O Pins

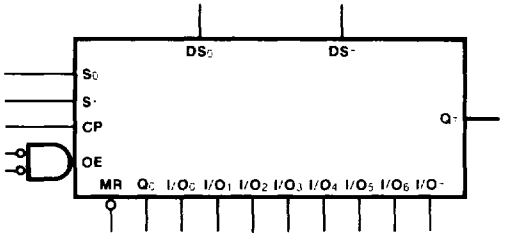
Description

The 'AC/'ACT299 is an 8-bit universal shift/storage register with 3-state outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs are provided for flip-flops Q_0, Q_7 to allow easy serial cascading. A separate active LOW Master Reset is used to reset the register.

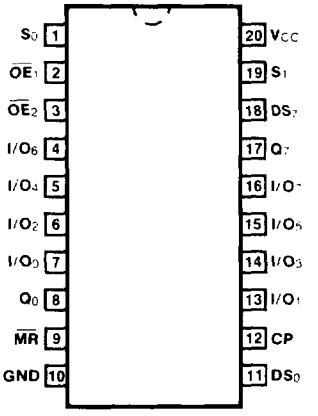
- **Common Parallel I/O for Reduced Pin Count**
- **Additional Serial Inputs and Outputs for Expansion**
- **Four Operating Modes: Shift Left, Shift Right, Load and Store**
- **3-State Outputs for Bus-Oriented Applications**
- **Outputs Source/Sink 24 mA**
- **'ACT299 has TTL-Compatible Inputs**

Ordering Code: See Section 6

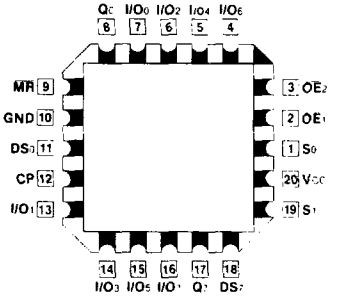
Logic Symbol



Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC

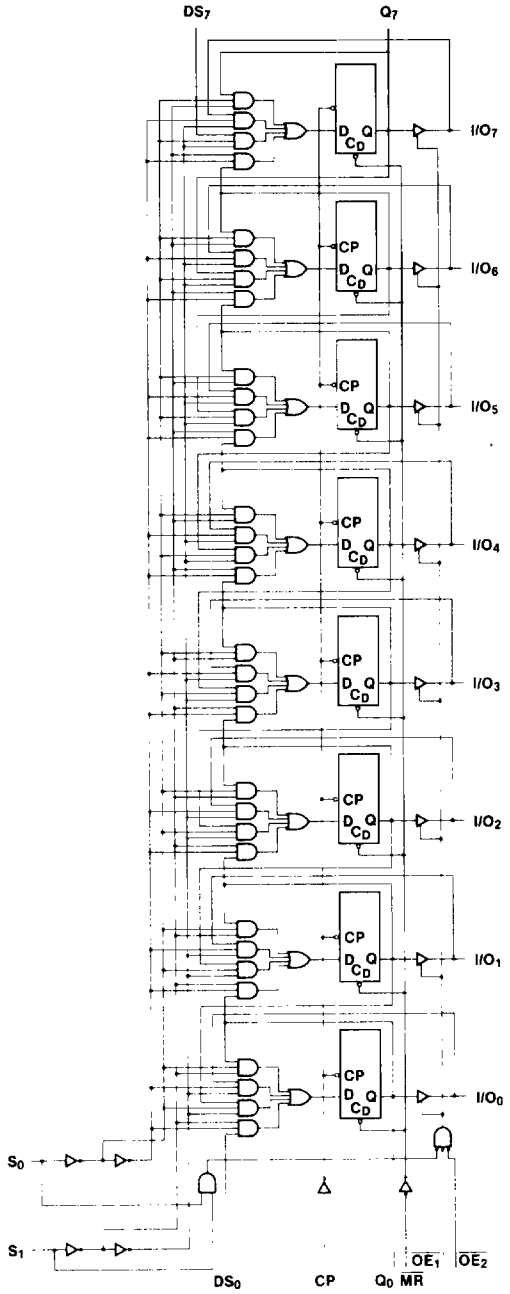


Pin Assignment for LCC

Pin Names

CP	Clock Pulse Input
DS_0	Serial Data Input for Right Shift
DS_7	Serial Data Input for Left Shift
S_0, S_1	Mode Select Inputs
$\overline{MR}$	Asynchronous Master Reset
$\overline{OE}_1$, $\overline{OE}_2$	3-State Output Enable Inputs
I/O_0 - I/O_7	Parallel Data Inputs or 3-State Parallel Outputs
Q_0, Q_7	Serial Outputs

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Functional Description

The 'AC/'ACT299 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift left, shift right, parallel load and hold operations. The type of operation is determined by S_0 and S_1, as shown in the Truth Table. All flip-flop outputs are brought out through 3-state buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q_0 and Q_7 are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on $\overline{MR}$ overrides the Select and CP inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

A HIGH signal on either $\overline{OE}_1$ or $\overline{OE}_2$ disables the 3-state buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The 3-state buffers are also disabled by HIGH signals on both S_0 and S_1 in preparation for a parallel load operation.

Truth Table

Inputs				Response
$\overline{MR}$	S_1	S_0	CP	
L	X	X	X	Asynchronous Reset; Q_0 - Q_7 = LOW
H	H	H	⌐	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	H	⌐	Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	H	L	⌐	Shift Left; $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	L	L	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Transition

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT299)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Input Frequency	3.3 5.0		55 130						MHz	3-3
t_{PLH}	Propagation Delay CP to Q_0 or Q_7	3.3 5.0		31.0 12.0						ns	3-6
t_{PHL}	Propagation Delay CP to Q_0 or Q_7	3.3 5.0		30.0 13.0						ns	3-6
t_{PLH}	Propagation Delay CP to I/O_n	3.3 5.0		28.0 11.0						ns	3-6
t_{PHL}	Propagation Delay CP to I/O_n	3.3 5.0		28.0 12.0						ns	3-6
t_{PLH} HL	Propagation Delay $\overline{MR}$ to ~~I/O_n~~ Q_0 to Q_7	3.3 5.0		33.0 14.0						ns	3-6
t_{PHL}	Propagation Delay $\overline{MR}$ to I/O_n	3.3 5.0		31.0 13.0						ns	3-6
t_{PZH}	Output Enable Time $\overline{OE}$ to I/O_n	3.3 5.0		24.0 10.0						ns	3-7
t_{PZL}	Output Enable Time $\overline{OE}$ to I/O_n	3.3 5.0		24.0 10.0						ns	3-8
t_{PHZ}	Output Disable Time $\overline{OE}$ to I/O_n	3.3 5.0		25.0 13.0						ns	3-7
t_{PLZ}	Output Disable Time $\overline{OE}$ to I/O_n	3.3 5.0		24.0 12.0						ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

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AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW S_0 or S_1 to CP	3.3 5.0	12.0 5.0				ns	3-9
t_h	Hold Time, HIGH or LOW S_0 or S_1 to CP	3.3 5.0	0 0				ns	3-9
t_s	Setup Time, HIGH or LOW I/O_n, DS_0 or DS_7 to CP	3.3 5.0	6.0 3.0				ns	3-9
t_h	Hold Time, HIGH or LOW I/O_n, DS_0 or DS_7 to CP	3.3 5.0	0 0				ns	3-9
t_w	CP Pulse Width, HIGH or LOW	3.3 5.0	9.0 4.0				ns	3-6
t_w	$\overline{MR}$ Pulse Width, LOW	3.3 5.0	7.0 4.0				ns	3-6
t_{rec}	Recovery Time, $\overline{MR}$ to CP	3.3 5.0	0 0				ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Input Frequency	5.0		125						MHz	3-3
t_{PLH}	Propagation Delay CP to Q_0 or Q_7	5.0		11.0						ns	3-6
t_{PHL}	Propagation Delay CP to Q_0 or Q_7	5.0		12.0						ns	3-6
t_{PLH}	Propagation Delay CP to I/O_n	5.0		10.0						ns	3-6
t_{PHL}	Propagation Delay CP to I/O_n	5.0		12.0						ns	3-6
t_{PLH}	Propagation Delay $\overline{MR}$ to Q_0 or Q_7	5.0		14.0						ns	3-6
t_{PHL}	Propagation Delay $\overline{MR}$ to I/O_n	5.0		13.0						ns	3-6
t_{PZH}	Output Enable Time $\overline{OE}$ to I/O_n	5.0		10.0						ns	3-7
t_{PZL}	Output Enable Time $\overline{OE}$ to I/O_n	5.0		10.0						ns	3-8
t_{PHZ}	Output Disable Time $\overline{OE}$ to I/O_n	5.0		12.0						ns	3-7
t_{PLZ}	Output Disable Time $\overline{OE}$ to I/O_n	5.0		11.0						ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW S_0 or S_1 to CP	5.0	5.0				ns	3-9
t_h	Hold Time, HIGH or LOW S_0 or S_1 to CP	5.0	0				ns	3-9
t_s	Setup Time, HIGH or LOW I/O_n, DS_0 or DS_7 to CP	5.0	3.0				ns	3-9
t_h	Hold Time, HIGH or LOW I/O_n, DS_0 or DS_7 to CP	5.0	0				ns	3-9
t_w	CP Pulse Width HIGH or LOW	5.0	4.0				ns	3-6
t_w	$\overline{MR}$ Pulse Width, LOW	5.0	4.0				ns	3-6
t_{rec}	Recovery Time, $\overline{MR}$ to CP	5.0	0				ns	3-9

*Voltage Range 5.0 is 5.0 V ± 0.5 V

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Capacitance

Symbol	Parameter	54/74AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance		pF	$V_{CC} = 5.5$ V