COBRA Device
COnstant Bit Rate ATM Adaptation Layer 1
TXC-05427B

DATA SHEET

FEATURES

- Four-channel AAL1 segmentation and reassembly
- Unstructured and Structured services
- Clock recovery, SRTS or adaptive FIFO mechanism
- Synchronous clocking mode
- Internal FIFO has programmable length for cell delay variation tolerance.
- Partially-filled cells segmentation and reassembly
- UTOPIA Level 1 compliant cell I/O interface
- Selectable AMI/B8ZS/HDB3 line coding
- Pseudo-random number pattern generator and analyzer (2^{15}-1, 2^{20}-1, QRSS)
- AIS generator
- Line coding violation monitor and counter
- Loss of signal detection monitor
- Line and cell loopback
- Serial port for control of line interface devices
- Motorola/Intel microprocessor interface
- IEEE 1149.1 boundary scan
- Low-power CMOS
- Single +5V power supply
- 160-pin plastic quad flat package

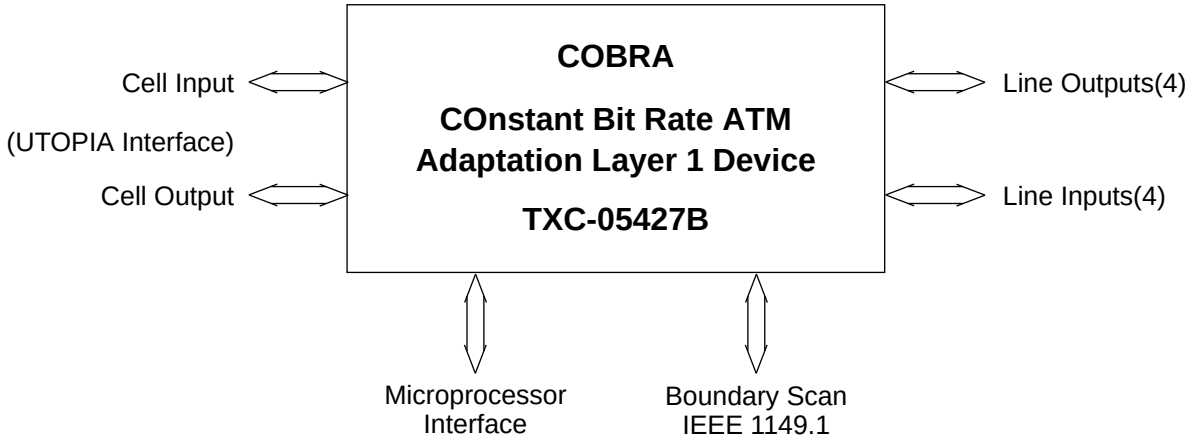
DESCRIPTION

COBRA (COnstant Bit Rate ATM Adaptation Layer 1) is a four-channel VLSI device that implements all of the functions needed for circuit emulation over ATM. Both Unstructured service (e.g., 1544 kbit/s and 2048 kbit/s) and Structured service (e.g., n x 64 kbit/s) are supported. COBRA offers three clock modes: internal clock recovery based on the Synchronous Residual Time Stamp (SRTS), clock recovery based on the FIFO fill level (adaptive FIFO), and an external clock mode. Internal data storage allows cell delay variation tolerance of more than one millisecond for data rates up to 2048 kbit/s.

COBRA connects directly to PCM line interface devices and to UTOPIA Level 1 compliant devices.

APPLICATIONS

- T1/E1 ATM circuit emulation
- Fractional T1/E1: n x 64 kbit/s service
- PBX
- Video transmission over ATM



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INTRODUCTION

COBRA (COnstant Bit Rate ATM Adaptation Layer 1 Device) is an AAL1 processor for interfacing four constant bit rate lines into and out of an ATM network supporting Structured and Unstructured services. Each channel can operate from 16 kbit/s to 8.448 Mbit/s, serving a wide variety of constant bit rate services.

COBRA supports four independent channels with separate clocking and mapping methods. COBRA supports Unstructured data service (e.g., 1544 kbit/s and 2048 kbit/s) and Structured data service (i.e., n x 64 kbit/s). In the Unstructured service mode, though primarily intended for T1/E1 circuit emulation, COBRA will support nominal bit rates up to 8.448 Mbit/s with appropriate scaling of system reference and SRTS clock frequencies. In Structured service mode, COBRA supports n x 64 kbit/s bit rates. In each of these service modes, COBRA can optionally recover the source clock using either the SRTS mechanism or the adaptive FIFO centering mechanism. It is also possible to operate COBRA in synchronous clocking mode with an external clock source.

For lower speed transmissions such as voice, it may be desirable to send out partially-filled cells. For example, a 64 kbit/s voice line will require nearly 6 milliseconds to fill a cell. This delay could impact transmission quality. Higher speed applications will see much less delay. COBRA supports partially-filled cells, in both Unstructured and Structured service modes. The number of real payload bytes contained in each cell is a parameter programmed independently for each channel. Note that while this method reduces transmission delay for sending ATM cells, it also reduces the total usable bandwidth of the ATM system.

COBRA's ATM interface conforms to the Universal Test and Operations Physical Interface for ATM (UTOPIA) standard set by the ATM Forum. The interface can be configured to be either UTOPIA Level 1 compliant cell level flow control or synchronous FIFO mode.

The line interfaces conform to existing standards, including encoding/decoding for connection to standard transmission lines such as T1 (DS1) and E1. The line interfaces are flexible, allowing the device to connect to most industry-standard line interface devices. COBRA incorporates serial port control pins to control line interface devices and other external components.

COBRA provides a microprocessor interface that is compatible with Motorola and Intel type microprocessors. Each of the four channels has a set of event flags and diagnostic features. The diagnostic features include signal loopback at critical points and pseudo-random test pattern generation and checking. The event registers and performance counters that are accessible via the microprocessor include:

- Loss of Signal
- Pseudo Random Number Loss of Lock
- Received Cell HEC Error, Loss of Cell Sequence, Loss of Structure Pointer
- Transmit/Receive side FIFO Overflow/Underflow
- Coding Violation Count, Discarded Cell Count, Inserted Cell Count

AAL1 PROTOCOL OVERVIEW

The AAL1 protocol, as specified by the standards bodies (e.g., ITU-T, ANSI), identifies the functions necessary to adapt Constant Bit Rate (CBR) traffic into ATM cells. Two types of AAL1 services have been defined. The following are brief descriptions for the Unstructured and Structured modes of ATM Adaptation Layer 1 (AAL1):

> **Unstructured** -- the mapping of a standard transmission line such as T1 (DS1) in North America and E1 in Europe. Higher rates are also covered. The standard transmission format (including framing and control information) is carried over an ATM network as a bit-

stream with an associated service clock so that it can be transparently reconstructed at the distant end by the receiving terminals.

Structured -- the mapping of an octet-based continuous signal such as a voice line into ATM. It is defined to handle a wide range of speeds that can range from 16 kbit/s encoded voice up to 6 Mbit/s encoded video, and higher. Frame boundaries of the Structured CBR signal are periodically transported over an ATM network using a structure pointer.

The AAL1 protocol header occupies the first byte of each cell body. In Unstructured service, each cell will then contain exactly 376 bits (47 bytes) of user data. An extra byte is taken once every eight cells when using Structured service. Structure boundary information is carried in this byte, indicating the first byte of the next structure. Altogether, when using Structured service, 7 out of 8 cells carry 47 bytes, and the remaining cell contains 46 bytes, yielding 375 user data bytes per 8-cell cycle.

Unstructured Service

Cell formation with Unstructured service is a simple matter of collecting 376 sequential incoming bits (47 bytes) which form the payload of a cell, as shown in Figure 1. As soon as the bits are received, the AAL1 protocol header and ATM headers are appended and the cell is launched toward its destination.

The AAL1 protocol header has two fields: sequence number, and sequence number protection. A simple cyclic modulo-8 count is placed into the sequence count field when cells are created, giving a simple means of ensuring both that cells are received in sequence, and of detecting lost or misinserted cells. Along with the count is a Convergence Sublayer Indication (CSI) bit, carrying control information dependent on service type. The Sequence Number Protection field contains a 3-bit CRC, generated over the sequence number field, plus a parity bit generated over the seven bits of CSI, sequence number and CRC bits. The series of CSI bits in four odd-numbered cells of an eight-cell cycle form a number that represents Synchronous Residual Time Stamp (SRTS). The four-bit SRTS value is a measure of the accumulated phase of the network reference clock as measured by the source signal.

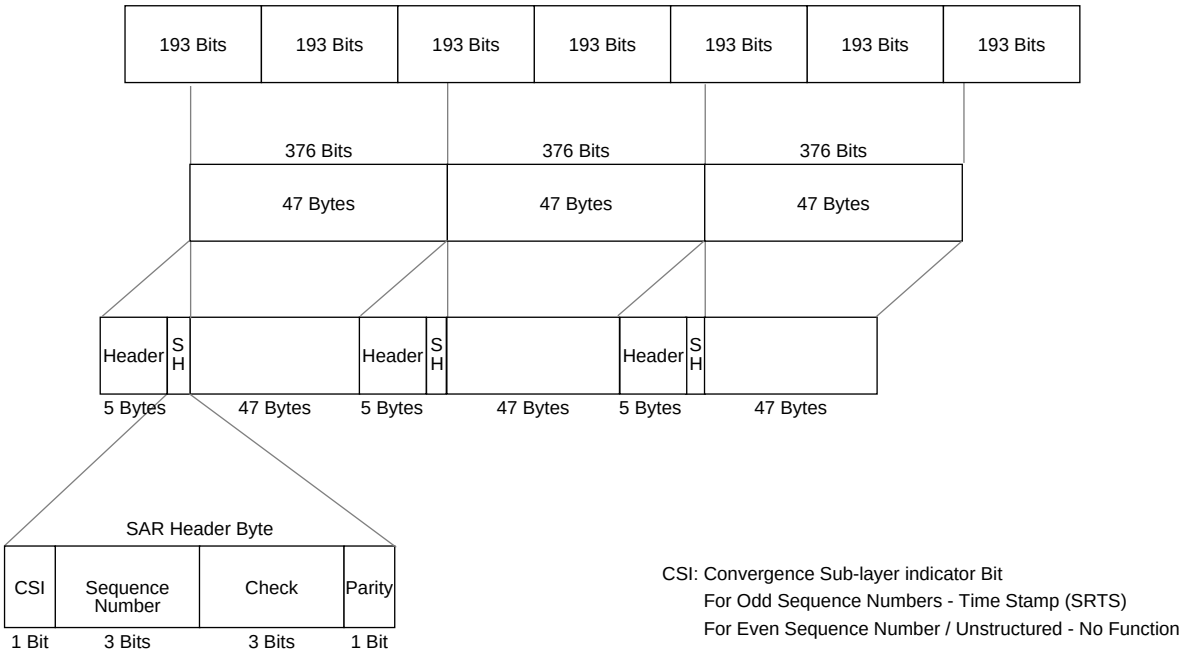


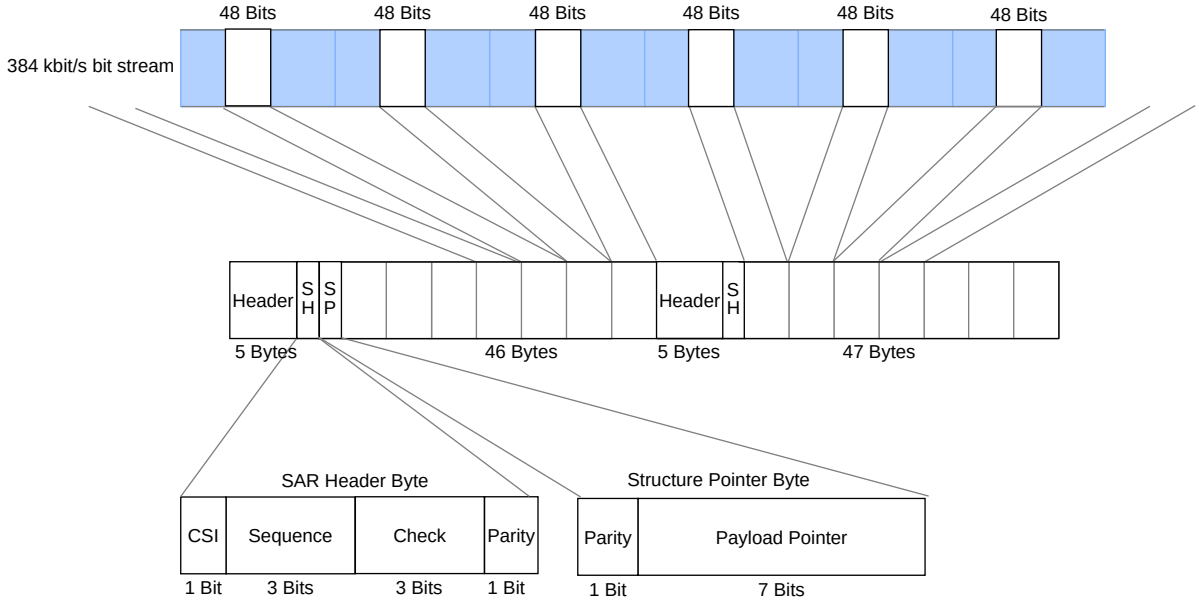
Figure 1. Unstructured AAL1 Segmentation of T1 Superframe

The SRTS values are extracted at the destination and are used for clock recovery. In certain applications the SRTS mechanism may not be used. Clock recovery at the destination end will be done only by use of received cell arrival times, a technique called adaptive clock recovery.

Structured Service

When using Structured service the same AAL1 protocol header format as defined for Unstructured service is used, but cell formation proceeds in an eight-cell cycle. For seven out of the eight cells, the payload consists of 47 bytes, byte-aligned (Structured service transfers bytes, not just bits). One cell in eight also contains a one-byte structure pointer. A seven-bit value is carried in bits 6 through zero, and an even parity in bit 7 (the MSB of the byte).The literal meaning of a pointer is the count of bytes from the pointer to the first byte of the next structure. If the value is zero, the very next byte, the first payload byte of this cell, is the first byte of the next structure. The presence of 1 in the CSI bit during one of the four even-numbered cells (0,2,4,6) indicates that the cell carries a structure pointer in its second byte position.

Cell formation with Structured service is a simple matter of collecting 46 / 47 octets which form the payload of a cell, as shown in Figure 2. For various applications, the structure size may be smaller than the size of a cell, or may be larger than a cell size, or may even be larger than eight cells, but there is only one structure pointer for every eight cells. If the structure size is small, less than or equal to 93 bytes, then a structure boundary will always occur within the first or second cell. In this case, the structure pointer will always occur in the cell having sequence number zero. Structure sizes from 94 through 375 bytes will always have at least one structure boundary within every 8-cell cycle, but structure sizes in excess of 375 bytes may not. A simple global rule is made for structure pointer placement. The structure pointer goes in the first even-numbered cell in an 8-cell cycle which immediately precedes a structure boundary. This results in a pointer in cell zero for a structure sized less than 94 bytes, or a pointer which may occur in any even-numbered cell for larger structure sizes, less than 375 bytes. For structure sizes over 375 bytes, a pointer may not occur within a particular 8-cell cycle. In this case, a pointer is inserted having a special pointer value of 127, indicating that a structure boundary does not lie within this cycle, but is at some later point. This guarantees that a constant number of data bytes is present in every eight cells.



CSI: Convergence Sub-layer indicator Bit
For Odd Sequence Numbers - Time Stamp (SRTS)
For Even Sequence Numbers - Structure Pointer Presence Indicator

Figure 2. Structured AAL1 Segmentation of 384 kbit/s Video Conference Signal

When more than one structure is contained in an 8-cell sequence, the structure pointer is used to indicate the proper position of the first structure boundary. The receiving device must then "flywheel" forward from this synchronizing point, delineating structures based on its knowledge of structure size. In the absence of errors, succeeding received structure pointers will be redundant, simply indicating that the structure boundary is in the position it is calculated to be from the previous pointer.

CLOCK RECOVERY

For both Unstructured and Structured services, clocking is critical because the source of these continuous signals may use a reference frequency different from those used by the ATM system. Two different mechanisms are available to assure that the received signal conforms to the source signal:

Synchronous Residual Time Stamp (SRTS) -- where the output clock rate is adjusted by a factor which is transmitted as part of the cell control information.

Adaptive -- where the output clock rate is adjusted by monitoring the length of the received queue of ATM cells and maintaining it at a constant level.

RELEVANT STANDARDS

The following standards provide information relevant to the COBRA device. Copies may be obtained from the organizations listed in the section entitled Standards Documentation Sources:

- B-ISDN ATM Adaptation Layer (AAL) Specification, Types 1 and 2: ITU-T I.363.X, Working Draft, November 1994
- Broadband ISDN - ATM Adaptation Layer for Constant Bit Rate Services Functionality and Specification: ANSI T1.630 1993
- Asynchronous Transfer Mode (ATM) and ATM Adaptation Layer (AAL) Protocols Generic Requirements: Bellcore GR-001113, Issue 1, July 1994
- ATM Forum Circuit Emulation Service Interoperability Specification, ATM Forum, June 1995
- ETSI prETS DE/NA - 52617, Annex D on cell sequencing
- Broadband Switching System Generic Requirements: Bellcore GR-001110-CORE, Issue 1, September 1994

BLOCK DIAGRAM

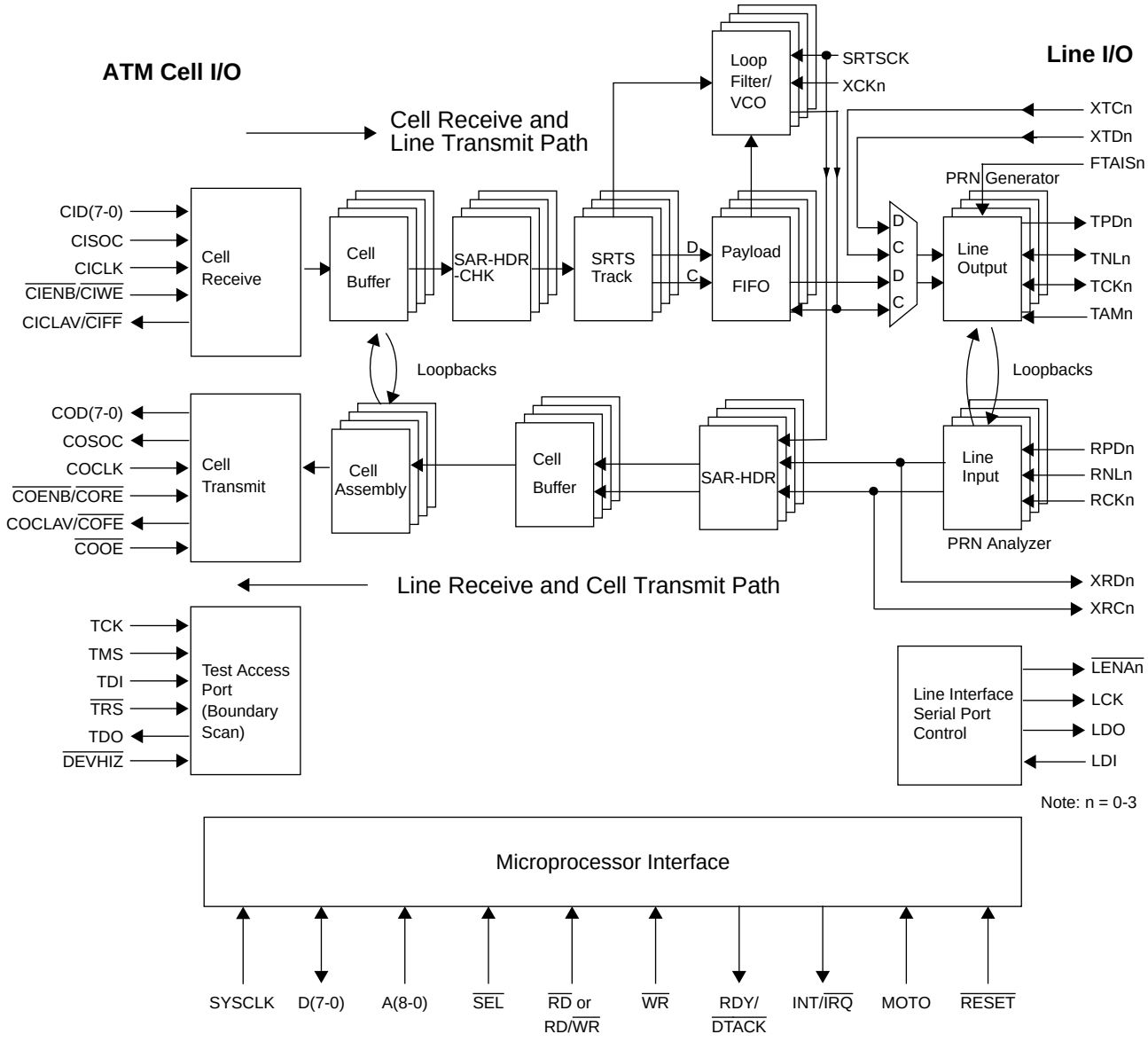


Figure 3. COBRA TXC-05427B Block Diagram

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BLOCK DIAGRAM DESCRIPTION

COBRA is a VLSI device supporting four independent channels for AAL1 segmentation and reassembly. A simplified block diagram of COBRA is shown in Figure 3. The channel number is shown as n (0, 1, 2 or 3) and this digit is used as a suffix in pin symbols (e.g., RCKn), and in symbols for bits in the per channel registers of the memory map (e.g., RLENn), to identify the associated channel. Please refer to the Pin Descriptions, Memory Map and Memory Map Descriptions sections for detailed information on pins and memory map bits.

LINE INPUT INTERFACE

The line input interface consists of clock and data pins to be connected to the external line transceiver or framer device. In Unstructured service, data is received on the line input interface without regard to the byte alignment of data. In Structured service, byte and structure alignment is provided by a positive pulse on pin RNLn. The line input interface can be programmed to use either the rising or falling edge for sampling the data pins using control bits RLCINVn. The clock on pins RCKn need not be a continuous clock and gapping is allowed. This allows the clock to be gapped so that data is read in only for certain time slots. If the line receive data is an encoded signal, the Line Input block performs either AMI, B8ZS or HDB3 decoder functions. Positive rail data is received on pin RPDn and negative rail data on pin RNLn.

Line Decoding

The line decoding block may be configured into one of four modes using control bits LCn1-LCn0 (LCn). For Unstructured service all four modes can be used. For Structured service, only NRZ mode is applicable. If line decoding is used, the coding violation counter CVnF-CVn0 counts the number of coding violations detected. In HDB3 mode, the COBRA does not detect a coding violation if the two pulses preceding the last bipolar violation are 00 (i.e., 0 on both positive and negative rails) and treats them as zero substitution.

Loss of Signal Detection

The loss of signal detection mechanism used is dependent on the line coding method selected and is independent of the speed of the clock on the RCKn pin. Upon detection of loss of signal, the Line Input block provides all ones data to the AAL1 Segmentation function. As a result, during loss of signal condition, cells with all ones payload are generated. A LOS alarm bit CRLLOSn is set to 1 to indicate the current state of the alarm.

In B8ZS mode, loss of signal is declared when no 1 bit is observed in 104 clock periods. Loss of signal is cleared when 13 or more 1 bits are observed and no more than 15 consecutive zeros are observed in an interval of 104 clock periods. The 104-clock period interval uses a jumping window rather than a sliding window. As a consequence, it is possible that an external 104-clock period count may not match the COBRA internal count, and measurements, if needed, may have to be made over a 208-clock period interval.

In HDB3 mode, loss of signal is declared when no 1 bit is observed for a period of 255 contiguous pulse positions starting with the last receipt of a one. The loss of signal is cleared when 32 ones are detected over a period of 255 contiguous pulse positions starting with the receipt of a one.

There is no loss of signal defined for AMI mode. It is recommended that the LOS interrupt associated with the latched alarm bit LRLLOSn for the channel should be ignored or masked out in this mode.

In NRZ mode, when control bit STRUn is set to 0, a high on input pin RNLn indicates a loss of signal.

Serial Port Control

The Line Interface Serial Port Control block is a serial interface to control and manage external line transceivers operating in the host mode. This allows the system processor to have complete control of the line transceiver through the COBRA processor interface. The interface consists of a data input pin LDI, data output pin LDO, a chip select pin LENAn, one for each transceiver, and a serial clock output pin LCK, common for all four channels. LCK is obtained from the SYSCLK input pin after dividing it by 16.

To perform a read operation, the host must write the register address into LRA7-LRA0 and write the line (channel) number into the LN1-LN0 control bits. The read operation is initiated by writing 0 into control bit LRW. The COBRA will assert the LENAn pin corresponding to the channel. The device will then serially output the register address on pin LDO in eight cycles of LCK. Following the address output, the COBRA will serially read data from pin LDI in the next eight cycles of LCK. When the COBRA completes the read operation, the result is stored in control bits LS7-LS0. The host must wait for 512 SYSCLK clock periods (do not change the address on the microprocessor address pins A8-0) for the operation on the serial interface to be completed before it can read the LS7-LS0 control bits.

To perform a write operation, the host must write the register address into LRA7-LRA0 and data into LD7-LD0, and then write the line (channel) number into control bits LN1-LN0. The write operation is initiated by writing 1 into control bit LRW. The COBRA will assert the LENAn pin corresponding to the channel. The device will then serially output the 8-bit register address on pin LDO followed by 8 bits of data in a total of 16 cycles of LCK. The host must wait for 512 SYSCLK clock periods (do not change the address on the microprocessor address pins A8-0) for the write operation on the serial interface to be completed.

Bypass Interface

This mode, selected using control bit EXTSIGn, is primarily intended for bypassing the AAL1 processing and to provide as outputs the line input clock and data (after line decoding, if used) on pins XRCn and XRDn. The line input data received on pins RPDn and RNLn is decoded and the NRZ data is output on pin XRDn. The line input clock RCKn is connected to the clock output pin XRCn.

Frame Pulse Input alignment

In Structured service, the line input interface accepts framed data from an external framer or a demultiplexing device. A high pulse on the input pin RNLn marks the first bit of the first byte of a structure. This pulse provides byte and structure alignment. The Line Input block resets its byte and structure alignment every time a high pulse occurs on the pin RNLn. For correct operation, a high pulse must occur on the RNLn pin every NNn + 1 bytes (where NNn refers to the number stored in the NNn9-NNn0 bits of the memory map). Upon a channel or device reset, AAL1 processing is not started until byte alignment is achieved.

AAL1 SEGMENTATION PROCESSING

Unstructured Service

Unstructured service mode is selected for channel n by setting the control bit STRUn to 0. For Unstructured service, data is received from the Line Input block without regard to byte alignment of data.

SAR Header Generation

The COBRA generates the SAR header shown in Figure 1. The sequence number counts modulo-8 with the initial sequence number being 0. The sequence number is incremented every time a new cell is generated for that channel. The CSI bit in even-numbered cells is set to 0. The CSI bits in odd-numbered cells carry the SRTS time stamp. The sequence number protection field constituting a 3-bit CRC and parity are computed.

SRTS Generation

The device generates a SRTS time stamp for each channel separately. The SRTS generation requires a network reference clock on the input pin SRTSCK. The device can accept a reference clock of speeds up to 78 MHz. Control bits REFDIVn2-REFDIVn0 are used to divide down the SRTSCK clock. They must be chosen such that the following expression is satisfied.

$$f_{RCKn} < (f_{SRTSCK} / 2^{REFDIVn}) < (2 \times f_{RCKn})$$

Figure 4 shows the SRTS time stamp generation circuitry. The resulting 4-bit code from the latch is inserted into the CSI bits of odd-numbered cells for that line. An SRTS code is generated for every eight cells' worth of data. Please refer to Figure 10 for additional retiming circuitry that is required external to the COBRA.

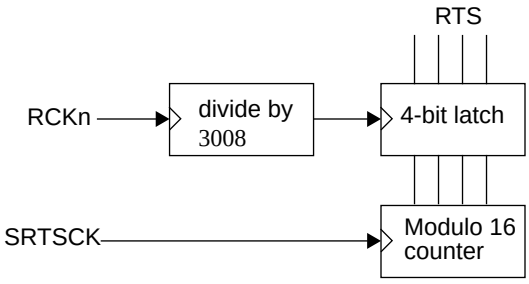


Figure 4. SRTS Generation Process

Payload Generation

The COBRA assembles data into the cell payload from the bit stream received from the Line Input block. If control bit PFILLn is set to 0, a cell contains 47 x 8 = 376 data bits. If PFILLn is set to 1, a cell contains (NFILLDn + 1) x 8 data bits (where NFILLDn is the number stored in bits NFILLDn5-NFILLDn0). If control bit PADBIS1 is set to 1, the rest of the cell payload is filled with dummy octets of all ones, otherwise it is filled with octets of all zeros. If control bits RLCn1-RLCn0 are set to 10, the cell payload is filled with an AIS signal of all ones. If RLCn1-RLCn0 are set to 11, the cell payload is filled with the data looped back from the Line Output block.

Structured Service

Structured service mode is selected for channel n by setting the control bit STRUn to 1. For Structured service, data is received from the Line Input block aligned to byte and structure boundaries. A structure pointer must be generated once every eight cells in one of the even-numbered cells.

SAR Header Generation

The COBRA generates the SAR header shown in Figure 2. The sequence number counts modulo-8 with the initial sequence number being 0. The CSI bit in odd-numbered cells is set to 0. The CSI bit in even-numbered cells is set to 1 if a structure pointer is carried in that cell.

Structure Pointer Generation

The COBRA generates a structure pointer based on the value NNn stored in control bits NNn9-NNn0. A structure pointer is generated every eight cells irrespective of whether a start or end of structure is present in the eight cell sequence. A pointer value of 93 is used whenever the end of the structure coincides with the end of the 93-octet block of a two-cell sequence and if the start of that structure is not in that two-cell sequence. If no start of structure or end of structure occurs within the eight cell sequence, then a dummy pointer with a value of 127 is inserted in cell number six. If partially filled cells are used, for structure pointer calculation purposes the dummy bytes are treated as part of the cell payload.

Payload Generation

The COBRA assembles data into the cell payload from the data bytes received from the Line Input block. When control bit PFILLn is set to 0, a cell contains 47 data bytes if a structure pointer is not inserted in that cell, otherwise it contains 46 bytes. When bit PFILLn is set to 1, every cell including the cell that contains the structure pointer contains (NFILLn + 1) data bytes. If control bit PADBIS1 is set to 1, the remaining bytes are filled with dummy octets of all ones, otherwise these bytes are all zeros. If control bits RLCn1-RLCn0 are set to 10, the cell payload is filled with an AIS signal of all ones. If RLCn1-RLCn0 are set to 11, the cell payload is filled with the data looped back from the Line Output block.

CELL HEADER GENERATION AND SCHEDULING

ATM Cell Header Generation

The 4-byte ATM cell header (excluding the HEC byte) is maintained in the per channel registers (Address 117H to 11AH for channel 0). Note that irrespective of the setting of the control bit NNIMODE, all four bytes of the ATM cell header are obtained from the control memory map. The COBRA computes the HEC byte and attaches it to the 48-byte payload with the 4-byte cell header to form the 53-byte cell. The HEC byte is always generated.

Routing Tag

The COBRA can attach up to seven bytes of routing tag to a cell. The control bits NRT2-NRT0 determine the number of routing tag bytes to be used (from 0 to 7). The control bit TAGMODE determines the position of the routing tag. If TAGMODE is set to 0, the routing tag is prefixed to the cell. If TAGMODE is set to 1, the routing tag is appended after the cell. Figure 5 shows the cell format with routing tag for different settings of the control bit TAGMODE.

Cell Buffers

The COBRA supports two cell buffers per channel in the cell output direction. As COBRA is used to provide CBR services, cells are generated periodically at a fixed rate for each channel. Since the bandwidth available from the cell output interface is significantly higher than the aggregate data rate of all four channels, two cell buffers per channel are sufficient. However, if the cell buffers overflow due to an extended blockage of the cell output interface, a latched event bit LCTOVF will be set to 1 unless the control bit INTPOS is set to 0. An interrupt is generated to indicate the alarm unless the mask bit MCTOVF is set to 1. If such an alarm occurs, all four channels must be reset by setting the control bits RLENn to 0 and then setting them back to 1 to resume normal operation.

Cell Scheduling

The cell scheduling mechanism determines which channel is to be serviced next. When the cell output interface is ready to transmit a cell, a simple round robin algorithm selects the channel to be serviced from all the channels that have cells ready to be sent. At least one full cell must be available for a channel to participate in the cell scheduling mechanism.

CELL OUTPUT INTERFACE

The Cell Output block transmits the cell out of the device. The interface is designed to operate in a shared environment with multiple devices sharing the cell output data bus. The interface can be configured into one of two modes. When the control bit UTOPIA is set to 1, the device implements the ATM Forum compliant Level 1 UTOPIA protocol. If UTOPIA is set to 0, the device acts like a read port of a synchronous FIFO. In both cases, the device will assert the COCLAV pin signal only when it has a full cell to send. As the device can attach a switch routing tag to an ATM cell, the cell may be extended up to a total of 60 bytes depending on the number of routing tag bytes selected. The start of cell signal is asserted coincident with the first byte of the extended cell. Figure 5 shows the format of the extended cell in different modes of the routing tag, which are selected using the TAGMODE and NRT2-NRT0 control bits to determine the placement of up to seven routing tag bytes, RT7-RT1.

TAGMODE = 0 NRT2-NRT0 = 111
RT7
RT6
RT5
RT4
RT3
RT2
RT1
GFC/VPI
VPI/VCI
VCI
VCI/PTI/CLP
HEC
Payload 1
• • •
Payload 48

TAGMODE = 1 NRT2-NRT0 = 111
GFC/VPI
VPI/VCI
VCI
VCI/PTI/CLP
HEC
Payload 1
• • •
Payload 48
RT7
RT6
RT5
RT4
RT3
RT2
RT1

Figure 5. Cell Format with Routing Tag

UTOPIA Mode

The device implements the slave interface (PHY-interface in UTOPIA terminology). When the COCLAV pin is asserted, the device is ready to transmit a complete cell. When the external device is ready to accept a cell the $\overline{\text{COENB}}$ pin must be asserted active low in response to an active high COCLAV pin signal. If the $\overline{\text{COENB}}$ signal is asserted prior to COCLAV becoming active, the COSOC pin signal is asserted active high one clock cycle after COCLAV is asserted high. The COCLAV signal remains asserted high during the transmission of the cell and is deasserted to low at a time based on the setting of the TCAVTH2-TCAVTH0 control bits. When the $\overline{\text{COENB}}$ pin is high, the data bus is tri-stated. In this mode, the $\overline{\text{COOE}}$ pin must be tied low.

FIFO Mode

When the control bit UTOPIA is set to 0, the cell output interface acts like a read port of a synchronous FIFO. The $\overline{\text{CORE}}$ pin is used as a read enable signal.

Cell Available Threshold

The control bits TCAVTH2-TCAVTH0 determine when the COCLAV pin signal is deasserted prior to the end of the cell. In FIFO mode, by setting the TCAVTH control bits, the deassertion of the COCLAV/COFE pin signal may be used as a FIFO almost-empty signal. In UTOPIA mode, these bits must be set to 0.

CELL INPUT INTERFACE

The cell input interface is designed to operate up to 25 MHz. The interface is designed to operate in a shared environment with multiple devices sharing the data bus. When the device is ready to accept a full cell, the pin CICLAV is asserted high.

UTOPIA Mode

When the control bit UTOPIA is set to 1, the cell input interface implements the slave side of the UTOPIA level 1 protocol. In this mode, the deassertion of the CICLAV pin signal indicates that four more bytes can be accepted by the device. The active low CIENB pin signal validates every byte on the cell input interface.

FIFO Mode

When the control bit UTOPIA is set to 0, the cell input interface acts like a write port of a synchronous FIFO. The CIWE signal acts like a write enable signal. Unlike the UTOPIA mode, the CICLAV/CIFF pin signal is asserted when at most two more bytes can be accepted by the device.

Start of Cell Synchronization

Cells at the input to the Cell Input block are delineated with a start of cell signal (CISOC input pin). If the enable signal pin CIENB is asserted low, and if the CISOC pin is asserted high, the COBRA starts receiving a new cell. If a new start of cell signal is received within 53 bytes of the previous start of cell, the COBRA drops the corrupted cell and starts receiving a new cell. This ensures that a corrupted cell does not enter the device.

ATM CELL HEADER LOOKUP

The COBRA supports both UNI and NNI modes. If the control bit NNIMODE is set to 1, NNI mode is selected. In this mode, the VPI field is 12 bits and 28 bits of the cell header are used for cell screening. If NNIMODE is set to 0 to select UNI mode, 24 bits of the cell header are used for cell screening. The most significant four bits (GFC) of the cell header are ignored and the VPI field is 8 bits.

If the HECENA control bit is set to 1, the incoming cell is checked for a valid HEC. If the HEC field is incorrect, the cell is discarded. No attempt is made to correct either single bit or multiple bit errors. If HEC checking is not needed, then the HECENA bit must be set to 0.

Cell Screening

A cell received from the Cell Input block is compared for a cell header match with the cell headers for all four channels. If there is a match, the cell is copied to the cell buffer of the appropriate channel. If NNIMODE is set to 0, 8 bits of VPI and 16 bits of VCI are used for a cell header match. If NNIMODE is set to 1, 12 bits of VPI and 16 bits of VCI are used for a cell header match. This type of cell screening function allows multiple COBRA devices to operate in a shared cell interface environment with each COBRA device accepting cells matching the programmed cell headers and discarding remaining cells. Note that the TLENn control bit for a channel must be set to 1 to enable that channel's programmed header to participate in the matching process. For example, if TLENn is set to 0 for all four channels, all incoming cells are discarded.

OAM Cell

The cell screening function matches only VPI and VCI. However, OAM F5 cells have the same VPI and VCI as the user data cells, and differ only in the PTI field. If the most significant bit of the PTI field of the received cell is zero, the received cell is accepted as a data cell. If the most significant bit of the PTI field is a one, the received cell is discarded. Hence, any OAM functionality that is required for circuit emulation must be performed external to the COBRA device.

Cell Buffers

When the cell screening mechanism detects a match, the cell is copied to a cell buffer of the appropriate channel. The device provides two cell buffers per channel. These buffers enable the cell input interface to accept data at the maximum rate. If both buffers are full, the CICLAV signal is deasserted until the device is ready to accept a full cell.

AAL1 REASSEMBLY PROCESSING

Unstructured Service

Sequence Number Processing

The sequence number processing function involves checking the AAL1 SAR header for errors in sequence number. If the sequence number is corrupted, the device attempts to correct it according to ITU-T I.363.x specifications. This verification results in declaring a cell as valid or invalid. A valid cell is defined as a cell with a sequence number which has no detected errors or which had an error that was corrected. The state machine constitutes two states: correction mode and detection mode. If the state machine transitions from one state to another an interrupt-related latched event bit LCSCTn is set to 1, if enabled by control bits INTPOS and/or INTNEG. In correction mode, single bit errors are corrected. In detection mode, all cells with detected errors are declared invalid.

The cell sequence number error status along with the incoming sequence number is passed through a second state machine which detects cell loss and/or mis-insertion. Two different sequence number tracking state machines are implemented and are selectable using control bit SCCHKn. Detected mis-inserted cells are discarded. Detected lost cells are compensated by inserting dummy cells. The 8-bit counters DCCTRn and ICCTRn count the number of cells discarded and the number of cells inserted, respectively. If the sequence number tracking state machine loses synchronization and/or if the payload FIFO Starvation or Overflow alarms are generated, the loss of cell sequence latched event bit LLOCSn will be set to 1 if enabled by control bits INTPOS and/or INTNEG, and an interrupt will result if it is not masked by control bit MLOCSn.

Two-Cell Mode (ETSI Mode, SCCHKn = 1)

This mechanism is based on the ETSI draft standard. The algorithm introduces a one cell delay before the delivery of received data, in order to correctly evaluate the existence of lost or mis-inserted cells. The algorithm is described by a state machine with five states. A decision is taken after the analysis of two consecutive cell sequence numbers. This means that when a cell is received, it is stored, waiting for the next cell before it is eventually processed. For further details, please refer to ETSI standard given in the Relevant Standards section.

One-Cell Mode (Low Latency Mode, SCCHKn = 0)

Unlike the two-cell mode, this mechanism does not introduce a one cell delay. It takes a decision based on the incoming cell number. Figure 6 below shows the sequence number tracking state machine in the one-cell mode. Upon reset, the state machine starts in the OUT-OF-SYNC state. If 8 consecutive sequence numbers are valid and in sequence, the state machine enters the SYNC state. While in SYNC state, if cell loss is detected (the state machine is expecting sequence number n+1 and the received cell is n+X where X > 1), dummy cells are inserted. In SYNC state, upon receiving an invalid cell, the state machine transitions to INVALID state. The

received invalid cell is discarded. While in INVALID state, if another invalid cell is received, the state machine transitions to OUT-OF-SYNC state. When the sequence tracking state machine enters OUT-OF-SYNC state, the loss of cell sequence alarm is generated. While the sequence tracking state machine is in OUT-OF-SYNC state, an AIS signal of all ones is output on the line.

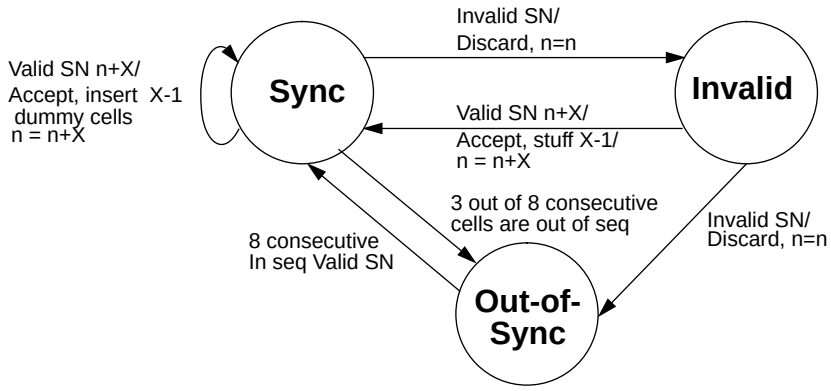


Figure 6. Cell Sequence Tracking State Machine if SCCHKn = 0

Dummy Cell Insertion on Detected Cell Loss

The sequence tracking state machines described above detect cell loss conditions. The sequence tracking state machine generates dummy cells with all ones in the payload to compensate for detected cell loss. This procedure guarantees bit count and bit sequence integrity on the line.

SRTS Time Stamp Reassembly

The CSI bits from cells with sequence numbers 1, 3, 5 and 7 are extracted to form the received SRTS time stamp. If SRTS clock recovery is used, this time stamp is provided to the clock recovery function.

Structured Service

For Structured service, in addition to the sequence number processing, the AAL1 reassembly process is required to frame to the incoming structure pointer.

Sequence Number Processing

The sequence number tracking modes described in the previous section are also applicable for Structured service. Lost cells are also indicated to the Structure Pointer processing tracking state machine.

Structure Pointer Processing

The Structure Pointer tracking state machine delineates structure boundaries based on the incoming structure pointer. The state machine has 3 states and maintains a count of the expected structure pointer. Upon reset, the state machine starts in the START state. The expected structure pointer is reset to the incoming structure pointer. The device then computes locally the next structure pointer value. If the incoming structure pointer value matches the locally computed value, the device enters the SYNC state. While in SYNC state, if a mis-match is detected, the device enters the ERROR state. While in the ERROR state, if another mis-match is detected the state machine enters the START state, which causes the expected structure pointer value to be reset. When a state machine transitions to the START state, the loss of structure pointer latched event bit LLOSPn will be set to 1 if enabled by control bits INTPOS and/or INTNEG, and an interrupt will result if it is not masked by control bit MLOSPn.

When structure alignment is achieved, the frame alignment signal is stored along with the data in the payload FIFO. A frame alignment signal is internally generated for every NNn + 1 bytes of cell payload.

Payload FIFO

Cells received from the sequence number and structure pointer processing unit are stored into an internal FIFO. This FIFO can be configured to be of length up to 16 cells using the control bits FIFLENn7-FIFLENn0. This storage allows cells to arrive with variable delays. If the cell delay variation (CDV) exceeds the value supported by the FIFO, eventually a FIFO underflow or overflow alarm occurs.

When a channel is enabled by setting the TLENn bit to 1, the FIFO read pointer is set to the start address of the FIFO. The FIFO write pointer is set to the center of the FIFO. Thus, one CDV's worth of arbitrary data is output before the receive data is played out.

Underflow

When there is no data in the payload FIFO for a channel, an underflow event bit CFUFn is set to 1 to provide a current indication of the underflow. As soon as an underflow event occurs, the device starts an internal 8-bit counter. This counter counts the number of octets inserted onto the line while the underflow persists. When cells start arriving, and if the counter has not rolled over, a number of bytes equal to the value of the counter is discarded from the incoming data. If the underflow event is exited due to arrival of cells before the counter overflows, the counter is reset. If the counter rolls over prior to the arrival of cells, a starvation alarm condition is declared. During underflow, the COBRA outputs an AIS signal of all ones on the line.

Starvation

If an underflow event persists for 256 bit periods, a current starvation alarm indication bit (CSTRVAn) is set to 1. When a starvation alarm event occurs, the channel must be reset by setting the TLENn bit to 0 and then setting it back to 1. This causes the sequence number and structure pointer tracking state machines, and the FIFO read and write pointers, to be reset. The device then attempts to synchronize to incoming cell sequence numbers and realign to the incoming structure pointer. During the synchronization period, the COBRA outputs an AIS signal of all ones on the line.

Overflow

When the payload FIFO is full and data from the incoming cell is ready to be placed into the FIFO, a current overflow indication bit (CFOVFn) is set to 1. When an overflow event occurs, the channel must be reset by setting the TLENn bit to 0 and then setting it back to 1. This causes the sequence number and structure pointer tracking state machines, and the FIFO read and write pointers, to be reset. The device then attempts to synchronize to incoming cell sequence numbers and realign to the incoming structure pointer.

Frame Slips

In Structured service, if there is a mis-match between source and destination frequencies, an occasional slip may need to be performed. Under command of the host software, the device can perform a slip. To delete a frame (NNn + 1 bytes), the control bit DELFRn must be written with 1. When the device completes deleting NNn + 1 bytes of data from the payload FIFO, the status bit FRDONEn is set to 1. This bit is cleared on a read. To delete another frame, the DELFRn bit must first be written to 0 (after detecting that the previous frame slip operation is completed by reading 1 in the FRDONEn bit) and then written to 1.

Similarly, the host software can request that a frame's worth of data to be inserted. This is achieved by writing 1 into the INSFRn control bit. When the COBRA finishes inserting a frame's worth of data, the FRDONEn bit is set to 1.To insert another frame, the INSFRn bit must first be written to 0 (after detecting that the previous frame slip operation is completed by reading 1 in the FRDONEn bit) and then written to 1.

Clock Recovery

Each channel of COBRA is provided with a highly-programmable clock recovery loop capable of supporting either SRTS or adaptive clock recovery, or a hybrid of the two modes. Four sections comprise the loop, shown in Figure 7: FIFO length section, SRTS section, loop filter and Digitally-Controlled Oscillator (DCO). There are a number of loop control registers for setting various gains and offsets. The following subsections detail loop operation and give examples of typical applications.

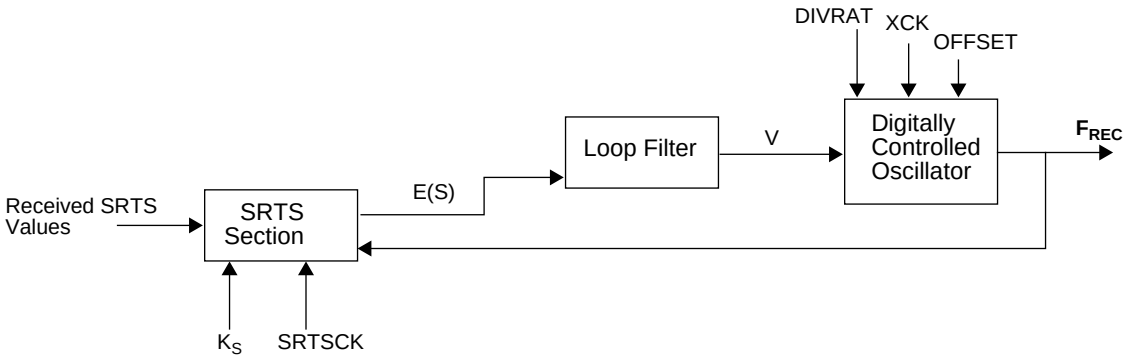


Figure 7. Clock Recovery Loop

The SRTS section recovers the SRTS values generated by the source terminal. The FIFO length, loop filter and DCO sections are used for clock recovery based on the Synchronous Residual Time Stamp algorithm. Optionally, an adaptive FIFO mechanism can be used to recover the clock based on the depth of the FIFO only.

Digitally Controlled Oscillator

The variable frequency element of the loop is a DCO which is driven by an external clock (XCK) of frequency f_{XCK}. The DCO generates a frequency f_{REC}, which is a function of f_{XCK}, and is directly settable by a digital control word V. That is, for a specific frequency of f_{XCK}, the DCO output frequency is determined by the value of V. The frequency sensitivity to input V is:

$$f_{REC} = f_{XCK} / [(N + 0.5) + V(2^{-19})]$$

which may be rearranged to the binomial form:

$$f_{REC} = [f_{XCK} / (N+0.5)] \times \{ 1 + [V(2^{-19}) / (N + 0.5)] \}^{-1}$$

and is approximately equal to:

$$f_{REC} = [f_{XCK} / (N+0.5)] \times \{ 1 - [V(2^{-19}) / (N + 0.5)] \}$$

$$f_{REC} = [f_{XCK} / (N+0.5)] - \{ f_{XCK} \times [V(2^{-19}) / (N + 0.5)^2] \}$$

where V is the decimal equivalent of the control word, V, and N is the internal scale factor, which are set as described below.

The DCO center frequency f_{NOM} is:

$$f_{NOM} = f_{XCK} \times V \times (2^{-19}) / (N+0.5)^2$$

and the equivalent DCO gain per count of control input V is thus:

$$K_o = f_{XCK} \times (2^{-19}) / (N+0.5)^2 \text{ Hz}$$

An internal scale factor for f_{XCK} is set by control bit DIVRATn. When DIVRATn=0, then factor N=31, and the frequency on input pin XCK must be nominally 31.5 times the frequency being recovered. DIVRATn=1 sets N=9, and XCK must be 9.5 times the nominal recovered frequency. For instance, for T1 clock recovery, DIVRATn=0 and XCK is 48.636 MHz. The DCO gain for this case is 0.09349 Hz per count. For E1 clock recovery DIVRATn=0 and XCK is 64.512 MHz, so the DCO sensitivity is 0.124 Hz per count. The sensitivity to the 16-bit direct control input OFFSET (LTOFFnF-LTOFFn0) is exactly the same as the sensitivity to control input V: the two are simply added.

The frequency of the signal on XCK need not be exact: it is not locked to the recovered frequency, but simply drives the DCO. The pull range of the DCO is +/- 212 counts, or +/- 382 Hz, for T1 operation. Since the maximum range of a T1 signal is +/-200 Hz, this leaves a maximum of +/-182 Hz, or +/- 118 ppm tolerance for f_{XCK}. Typically, f_{XCK} should be held to +/- 50 ppm tolerance.

Loop Filter

The loop filter is internally contained and has no control inputs. It accepts error outputs E(S) from the SRTS section and E(F) from the FIFO length measurement section and produces DCO control signal V.

SRTS Clock Recovery

The essential components used in SRTS clock recovery are the DCO and loop filter, and a group of components which make an SRTS error measurement. SRTS-only clock recovery operation requires an accurate network reference clock that is referenced to Primary Reference Source (PRS) and must be a stratum-1 clock. This clock input is connected to pin SRTSCK and is scaled internally by a divider set by control bits REFDIVn3-REFDIVn0. The frequency of the signal on pin SRTSCK is divided by 2 raised to the power contained in REFDIVn, interpreted as a binary value from 0 through 15. The resulting SRTS clock has frequency f_{SRTS}. If, for instance, SRTSCK has a frequency of 19.44 MHz, and T1 clock recovery is to be performed, then REFDIVn must be set at 0011 (decimal 3) to produce the required f_{SRTS} = 2.43 MHz SRTS reference clock frequency.

For normal SRTS-only operation, the loop is a first order phase-locked loop (PLL). Aside from the DCO and SRTS clock programming, the only variable is the loop gain K_s, set by register value KSn3-KSn0. The SRTS measurement gain sensitivity is:

$$K_{sm} = K_s \times \{ 1 - [(f_{SRTS} \times 3008/f_s), \text{modulo-16}] \}$$

where f_s is the source frequency to be recovered.

The loop bandwidth is the product of the DCO sensitivity K_o and K_{sm}:

$$f_B = K_o \times K_{sm}$$

$$f_B = [f_{XCK} \times (2^{-19}) / (N+0.5)^2] \times K_s \times \{ 1 - [(f_{SRTS} \times 3008/f_s), \text{modulo-16}] \}$$

For the T1 operation described above, and for K_s=1, the loop bandwidth is 0.178 Hz.

Adaptive Clock Recovery

Please refer to TranSwitch Application Note AN-523, entitled "An Adaptive Clock Recovery Scheme for Constant Bit Rate Applications using the TranSwitch COBRA Device (TXC-05427B), document number TXC-05427B-AN1.

External Clock

In this mode, selected by setting control bit CLKn to 1, clock recovery is not performed in the device. Instead, the line output clock pin TCKn is an input. Data is read out of the FIFO using this clock. Note that in this mode, if Structured service is used, the frame alignment pin TNLn also becomes an input.

LINE OUTPUT INTERFACE

The line output interface sends data from the payload FIFO to the line. The clock signal is an output if the internal clock recovery option is used. In this case, the clock that is output from COBRA is a continuous clock of frequency that is being recovered. For synchronous circuit emulation applications, clock is an input and is used to read payload data from the FIFO. This clock need not be a continuous clock and may be gapped. For interface flexibility, a control bit (TLCINVn) is provided for inverting the active edge of the clock. If TLCINVn is set to 1, the rising edge of TCKn is the active edge. Data is output on the active edge and input data is sampled on the active edge.

Line Coding

The Line Output block provides positive/negative rail data or NRZ signals. AMI, B8ZS or HDB3 line coding can be selected for rail data by setting control bits LCn1-LCn0.

Activity Monitor

The COBRA provides an input line activity monitor pin, TAMn. Many line interface devices provide a line activity monitor output, such as a Driver Performance Monitor (DPM) pin, which may be connected to TAMn. The status of this pin can be monitored through the COBRA microprocessor interface. If a high is detected on the TAMn pin, a loss of activity current status bit CTLLOAn is set to 1. The loss of activity latched event bit LTLLOAn will be set to 1 if enabled by control bits INTPOS and/or INTNEG, and an interrupt will result if it is not masked by bit MTLLOAn. It is only a status interrupt and no other processing is performed. AAL1 processing is not interrupted.

Frame Alignment

In Structured service with internal clock recovery, the COBRA outputs a frame alignment pulse every NNn+1 bytes on pin TNLn. A high pulse on this pin marks the first bit of the first byte of a structure. However, if external clocking is used (STRUn = 1, CLKn = 1), the frame pulse is an input to the device on pin TNLn. In this case, the COBRA flywheels the incoming frame alignment signal on pin TNLn with the internally generated frame pulse. If a frame pulse is not seen on the input when the device is expecting it, the COBRA freezes that byte and continues to play the same byte until the next frame pulse match occurs.

AAL1 Bypass Interface

This mode, selected using control bit EXTSIGn, is intended to connect to a cell relay service. The COBRA device is primarily performing the line encoding function. NRZ data received on pin XTDn is encoded and is output on pins TPDn and TNLn. The input clock XTCn is used to derive the output clock TCKn.

DIAGNOSTIC FUNCTIONS

Loopback

The COBRA supports both line and cell loopback. The loopback function is provided for diagnostic purposes. To support loopback, both transmit and receive directions of a channel must be enabled by setting TLENn and RLENn bits to 1.

Line Loopback

The COBRA supports loopbacks in both directions at the line interface. All four channels can be independently configured to be in line loopback. Figure 8 shows the datapath for one of the channels.

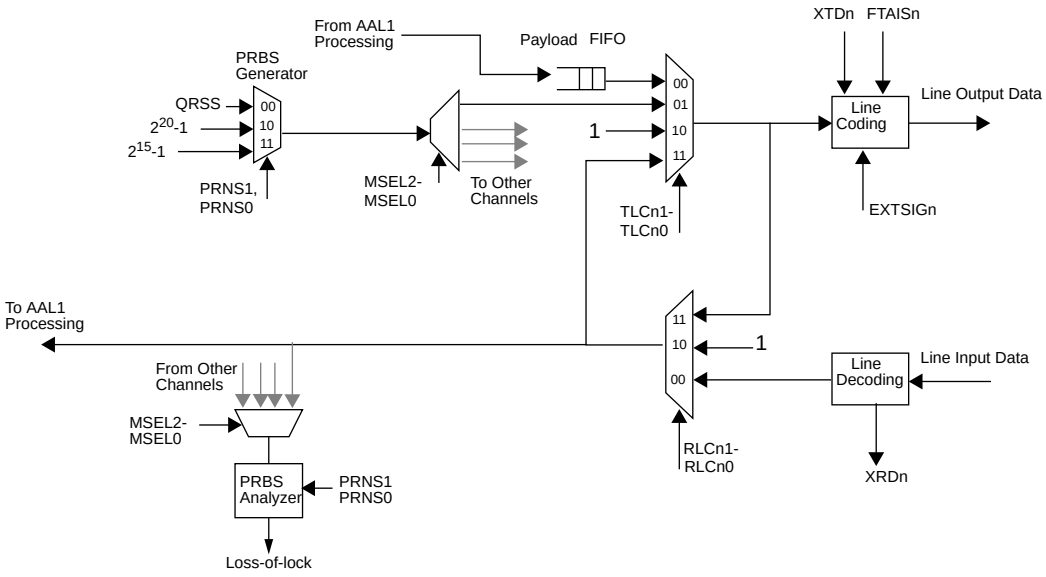


Figure 8. Line Loopback Data Flow

Line Input to Line Output Loopback

When the TLCn1 and TLCn0 control bits are set to 11, the line input data and clock are looped back to the line output. The line input data is first decoded and then looped back to the Line Output block. The Line Output block encodes the signal and then sends it out on the output pins. While data loopback is continuing, the AAL1 segmentation process is also performed, resulting in generation of cells. If the channel that is looped back is programmed to be in Structured service mode (STRUn = 1), then data received on the RPDn pin is looped back. Data received on the RNLn is ignored. Also, the TNLn pin is set low.

Line Output to Line Input Loopback

When the RLCn1 and RLCn control bits are set to 11, clock and encoded data from the Line Output block are looped back to the Line Input block. The Line Input block decodes the data. While the data is looped back, encoded serial data will continue to be supplied at the output pins of the device.

Cell Loopback

The COBRA supports loopbacks in both directions at the cell interface. Unlike line loopback, only one channel can be configured to be looped back at any time. Precedence is given to the lower numbered channel if multiple channels are placed into cell loopback mode. AAL1 processing continues to be performed for other channels that are not in loopback.

Cell Input to Cell Output Loopback

When control bit RLPBKn is set to 1, cells received for that channel are looped back to the cell output interface. When this loopback is used, AAL1 reassembly for that channel is not performed. Due to the handshaking requirements of the UTOPIA protocol, this loopback is not a pin-to-pin loopback.

Cell Output to Cell Input Loopback

When control bit TLPBKn is set to 1, cells generated for that channel are looped back to the cell input interface. Cells generated for the channel that is looped back are not provided on the cell output interface. Cells generated for other channels continue to be sent as output on the cell output interface.

PRBS Generator and Analyzer

The COBRA device has a built in pseudo-random binary sequence (PRBS) number generator and analyzer. The control bits PRNS1-PRNS0 select one of 3 different pseudo-random number patterns. As there is only one PRBS generator and one PRBS analyzer, only one channel can be connected to the generator and analyzer at any time. Control bits MSEL2-MSEL0 are used to select the channel that is connected to the PRBS generator and analyzer.

The Line Input blocks have a common (2^{15}- 1), (2^{20} - 1) and QRSS (2^{20} - 1 with zero suppression) pseudo-random pattern analyzer for testing and diagnostic purposes. If PRBS is enabled, the pseudo-random number loss of lock is declared when 30 bits out of 1000 bits are received in error. The loss of lock state is cleared when a specific 24-bit pattern is received, as indicated in the following table:

PRNS1-PRNS0	PRBS Polynomial	PRBS Pattern to exit Loss of Lock
00	QRSS (2^{20} - 1) with zero suppression	FFFFFE
01	Reserved. Do not use.	
10	2^{20} - 1	FFFFF0
11	2^{15}- 1	0001FF

Counters

The COBRA provides several counters per channel to support diagnostic and management functions. During normal AAL1 SAR processing, if line coding is enabled and if control bit MSEL2 is set to 0, CVnF-CVn0 is a 16-bit counter that counts the number of coding violations encountered. When the MSEL2 bit is set to 1, the counter CVnF-CVn0 does not count the number of coding violations. To read a 16-bit counter, the register containing the lower byte (7-0) of the counter must be read first. This will cause the lower byte to be read properly, and the upper byte to be latched. The upper byte must then be read. The 8-bit counter DCCTRn7-DCCTRn0 is incremented every time a cell is discarded in the sequence number tracking state machine. The 8-bit counter ICCTRn7-ICCTRn0 is incremented every time a cell is inserted for detected cell loss in the sequence number processing. All counters are non-saturating and roll over to zero from maximum count. A counter may be cleared to zero by performing a write operation for its register. The contents of the data bus are not important for this write to clear operation. However, any updates to the counters that occur during the clearing process may be lost.

MICROPROCESSOR INTERFACE

The microprocessor interface provides access to the control registers that are used for device configuration, the status and alarm registers, and the performance counters. COBRA supports Motorola and Intel compatible microprocessors with interrupt capability.

Interrupts

The COBRA provides chip level (global) interrupts and per channel interrupts, based on latched event bits, each of which is provided with a mask bit which disables the interrupt when set to 1. To process an interrupt, the host software must first read address register 008H. This polling register indicates whether it is a chip level interrupt (bit GCMS) or a channel interrupt (bits CMS3-CMS0). If it is a chip level interrupt, the register at address 009H contains the latched event bits. If it is a channel interrupt, the latched bits of the indicated channel must be read (registers 101H, 131H, 161H and 191H for channels 0, 1, 2 and 3, respectively). There are three registers for each of the per channel alarms: Mask Register, Latched Event Register and a Current Status Register. For global alarms, only the Mask Register and the Latched Event Register are available. The Current Status indicator bits are set to 1 only for the duration of the alarm. The Latched Event indicator bits remain set to 1 until they are reset to 0 automatically when their register is read, and they may be used to detect if any alarm events have occurred since the register was last read.

Two control bits in the common memory segment, bit 1 in Address 00BH (INTPOS) and bit 0 in Address 00BH (INTNEG), govern the setting of the bits in the Latched Event Register. When both of these bits are set to 0, occurrence of an alarm does not set a latched event bit. When INTPOS is 1 and INTNEG is 0, the latching to 1 will occur at the start of an alarm occurrence (i.e., on the positive transition of the Current Status indication bit, from 0 to 1). When INTPOS is 0 and INTNEG is 1, the latching to 1 will occur at the end of an alarm status (i.e., on the negative transition of the Current Status indication bit, from 1 to 0). When INTPOS and INTNEG are both set to 1, latching to 1 will occur on both positive and negative transitions. Latched event registers are automatically reset to 00H when they are read, terminating the interrupt caused by any 1 bit(s) they contained.

Polling Register in Common Memory

A read-only polling register is located in the common memory segment at address 008H. Bits 4-1 (CMS3-CMS0) correspond to channels 3-0, and bit 0 (GCMS) provides a global indication. Each bit is set to 1 whenever any one or more of its associated (8) per channel or (3) global latched event indication bits is set to 1, and is set to 0 otherwise. Reading the polling register permits the microprocessor to identify the source of a hardware interrupt caused by setting of a latched event bit.

Mask Registers for Interrupt Control

The Mask Registers are used to control the generation of a hardware interrupt to the microprocessor upon the occurrence of alarms (latched events). There is an 8-bit read/write mask register for each of the global and per channel sets of event alarm indications described above. The per channel mask registers are located at address 1X2H in the four per channel memory segments, where X=3n and n is the channel number (n=0-3), as shown in the Memory Map section. The global mask register is located at address 00AH in the common memory segment, but only three bits (2-0) are used, one for each of the global alarms. An interrupt is generated whenever an event bit in the latched event registers transitions from 0 to 1, provided that the alarm is not masked by the associated mask bit having been set to 1. When a particular alarm is not applicable for a given mode (for example, loss of structure pointer alarm in Unstructured service) that alarm must be masked and the Latched Event and Current Status bits for that alarm must be ignored.

Global Latched Event Register in Common Memory

The global event read-only register is located in the common memory segment at address 009H. Each of three bits (2-0) of this register corresponds to one of three different global event alarm indications, as shown in the Memory Map Description section. The bits in register 009H are latched bits, which are all reset to 0 when the register is read, and which thereafter may be individually set and latched to 1 when the corresponding alarm first experiences a transition of a type enabled by the settings of the INTPOS and INTNEG control bits.

Status and Event Registers in Per Channel Memory

Two 8-bit Current Status and Latched Event read-only registers are provided for each channel in the memory map, which is directly addressable by the microprocessor. These registers are located at addresses 1X0H and 1X1H respectively in the four per channel memory segments, where X = 3n and n is the number of the channel (n = 0-3). For each channel, each bit of each register corresponds to one of eight different alarm indications for that channel, as shown in the Memory Map Descriptions section. The bits in register 1X0H are Current Status alarm bits, which are set to 1 when the alarm is active and are set to 0 when it is inactive. The bits in register 1X1H are Latched Event alarm bits, which are all reset to 0 when the register is read, and which thereafter may be individually set and latched to 1 when the corresponding alarm first experiences a transition of a type enabled by the settings of the INTPOS and INTNEG control bits.

Hardware and Software Reset

The COBRA device supports two types of reset: hardware reset through pin $\overline{\text{RESET}}$ and software reset through register address 007H. An active low hardware reset signal on the $\overline{\text{RESET}}$ pin resets all channels and state machines. The complete memory map is reset, including configuration registers, current status registers, latched event registers and performance counters.

A software reset on all channels can be performed by writing 91H into the register address location 007H. This will result in a reset of all state machines, current status registers, latched event registers and performance counters. However, it does not reset the configuration registers. The device can be removed from software reset and placed into normal operation by writing any value other than 91H into register address location 007H. Reading this register location will return 01H if the device is in reset or 00H otherwise.

Each channel can be independently reset by writing 0 into the corresponding TLENn and RLENn bit. This resets all of the channel's state machines, current status registers and latched event registers but does not affect the configuration registers. To resume normal operation, 1 must be written to the TLENn and RLENn bits.

TEST ACCESS PORT

The Test Access Port provides an input pin ($\overline{\text{DEVHIZ}}$) for setting all device output pins (except RDY and TDO) to a high impedance state and it provides five other pins for the boundary scan capability described in the Boundary Scan section.

APPLICATIONS

UNSTRUCTURED SERVICE

Figure 9 shows an Unstructured service application when COBRA is used in a DS1/E1 circuit emulation mode. In this case, all control and framing bits are sent along with information bits, so no framing is required. There is no correlation between cell boundaries and the DS1/E1 frame structure. COBRA segments the incoming bit stream into 47-byte ATM cells. At the ATM receiving end, bits in the received cells are sent out steadily without regard to cell boundaries or DS1/E1 frame locations. Since the clock frequency is properly recovered, the terminating COBRA will always have the proper number of bits for transmission.

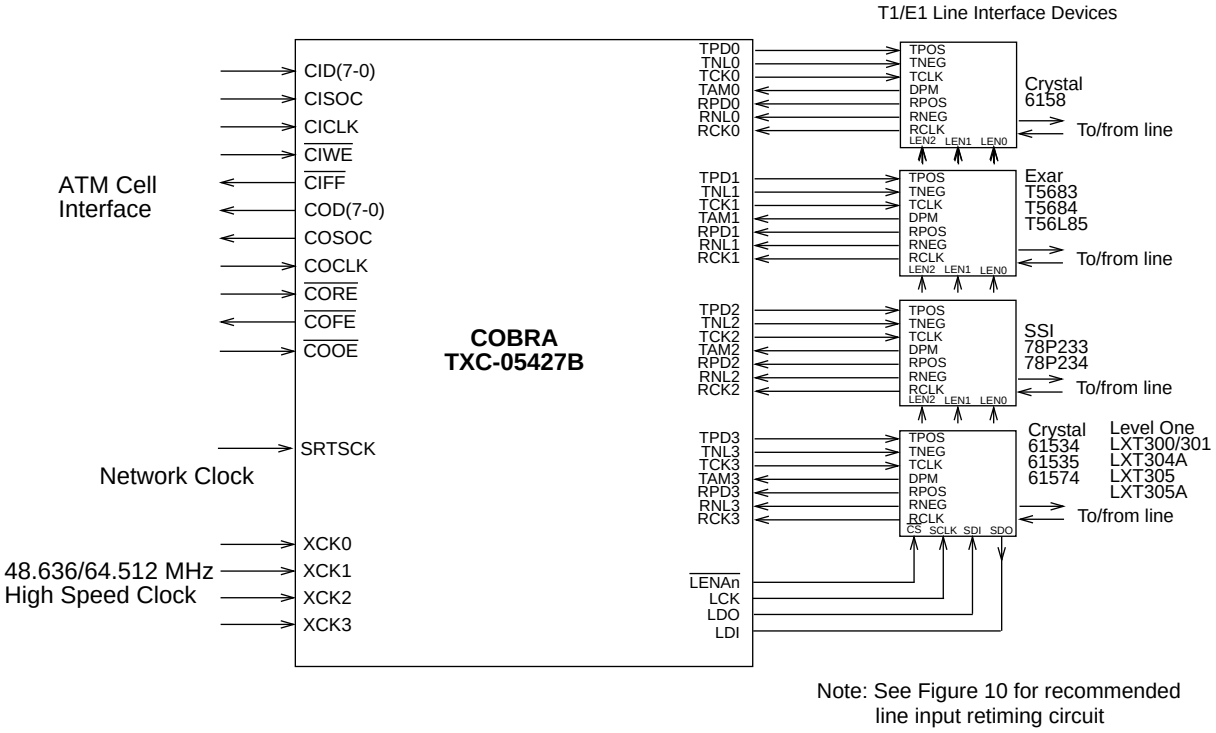


Figure 9. Unstructured Service Design Example

While Figure 9 illustrates a direct connection between the COBRA device and the line transceivers, some intermediate external retiming circuitry is required for the line input interface. The recommended circuit is shown in Figure 10.

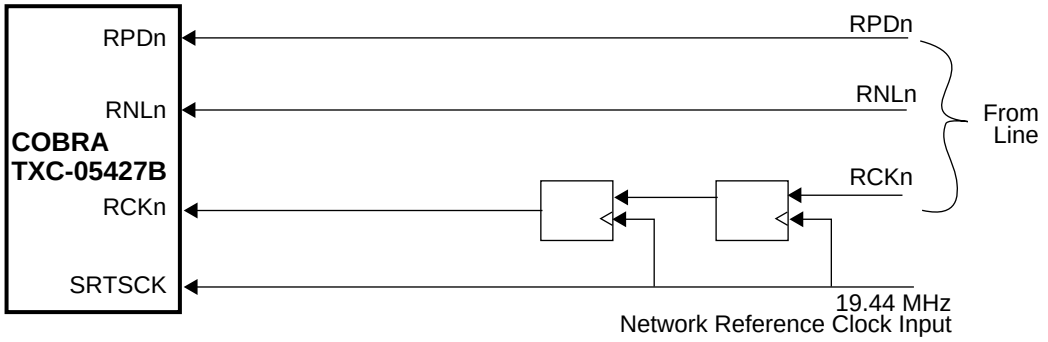
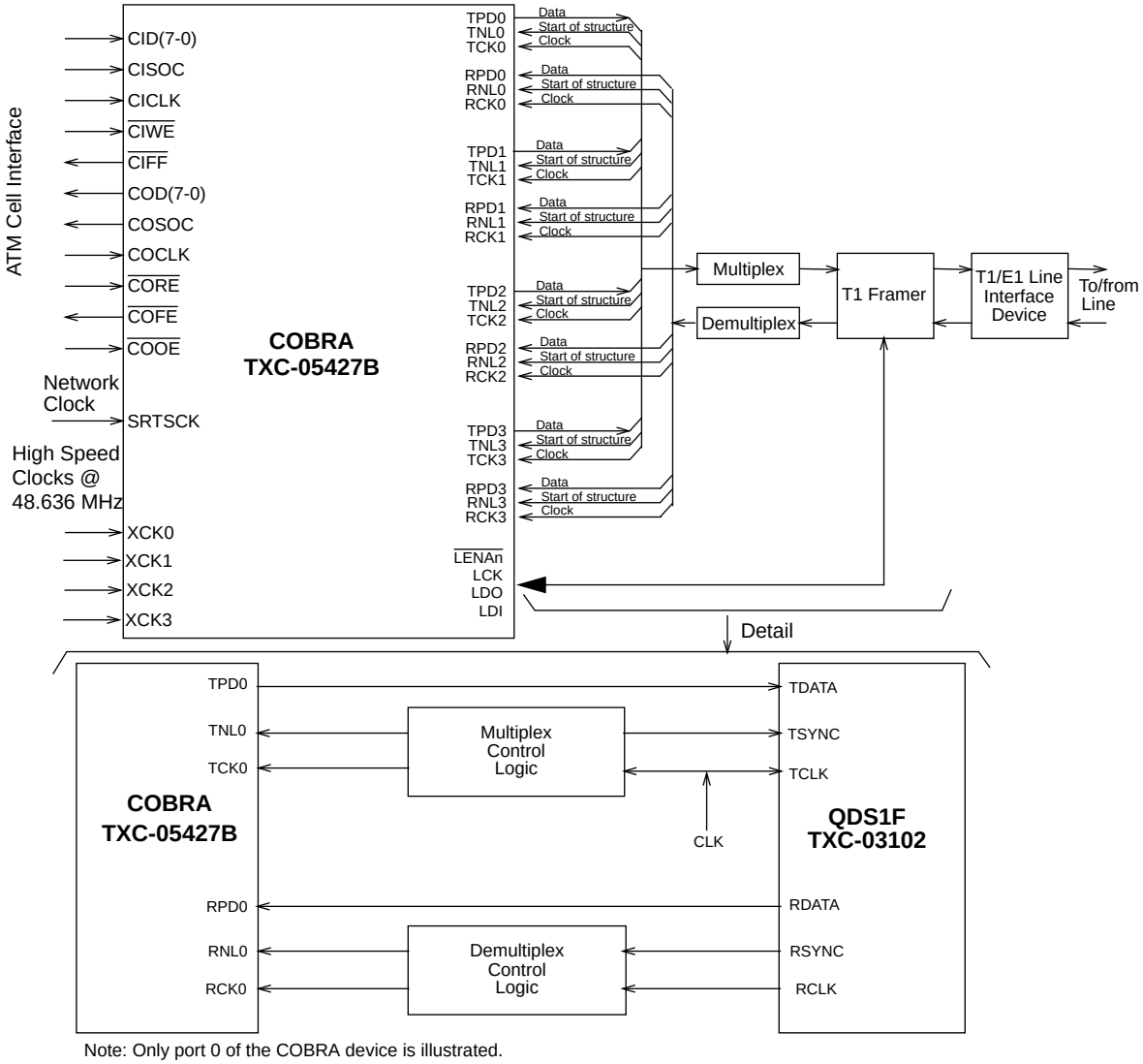


Figure 10. Unstructured Service Design Example - External Retiming Circuit

STRUCTURED SERVICE

Figure 11 shows a Structured service application in which the COBRA is used with TranSwitch's Quad DS1 Framer VLSI device. The Multiplex/Demultiplex logic may be used to take all 24 time slots from a single T1 frame and distribute them among the four ports of COBRA. For example, to provide 384 kbit/s service, six time slots may be fed to each of the line input ports. A more general application will require the number of time slots to be fed to each port to be programmable and it is the function of Demultiplex logic to gap the clock signal and provide the frame alignment signal on each of the ports. Further, it is the responsibility of the Multiplex logic to retrieve data from each of the ports of COBRA and combine these outputs to form the 24 time slots of a T1 frame.

In the example shown below, all 24 time slots except the framing bit are transported through a single channel to provide a 24 x 64 kbit/s service. The 24 time slot boundary is provided to COBRA on pin RNLn. The control bits NNn9-NNn0 are set to 23 to indicate a structure size of 24. Further, the COBRA is operating in External Clocking mode (CLKn = 1) so that TCKn and TNLn are input signals. The example shown provides basic Structured service without channel associated signalling.



Note: Only port 0 of the COBRA device is illustrated.

Figure 11. Structured Service Design Example

COBRA Line Input Timing

The QDS1F framer outputs RDATA on the falling edge of RCLK. The COBRA channel number 0 receives serial data from the QDS1F framer on the rising edge of RCK0. RCK0 is derived from RCLK by gapping at appropriate time instants. For this purpose, a modulo-193 counter, RCNT, is implemented in the Demultiplex control logic. This counter is incremented on the rising edge of RCLK. It is reset to 0 when RSYNC goes high. When counter RCNT is at 0, the next clock cycle of RCLK is gapped. This is to enable the COBRA to skip the framing bit. When RCNT is at 1, RNLn is set to 1 for one clock cycle on the falling edge of RCLK. This is to provide COBRA the start of structure indicator. The diagram in Figure 12 shows the timing relationship.

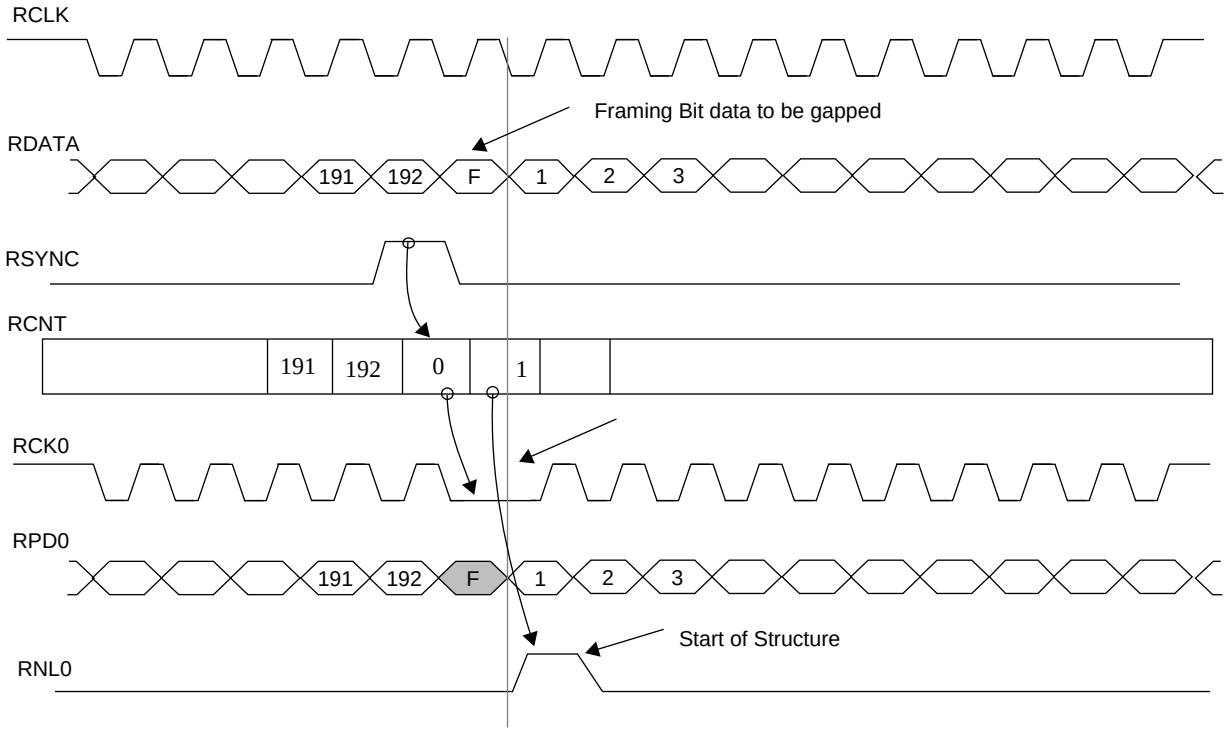


Figure 12. Structured Service - Line Input Timing

COBRA Line Output Timing

The line output data TPD0 is clocked out from COBRA on the falling edge of TCK0. The QDS1F framer receives data TDATA from the COBRA on the rising edge of TCLK. The data output from the COBRA must be frame aligned to the QDS1F framer TSYNC input. This is the function of the Multiplex control logic.

TCLK and TCKn are derived from a common system clock CLK. The frequency of CLK is 1.544 Mbit/s. However, since the COBRA device provides data for 24 time slots, excluding the framing bit, the COBRA clock input signal TCK0 must be gapped during the framing bit position to enable the QDS1F to insert the framing bit. For this purpose, a modulo-193 counter TCNT is implemented in the Multiplex control logic. This counter is incremented on the rising edge of CLK. When TCNT is at 192, the next clock cycle of TCKn is gapped to enable the QDS1F to insert the framing bit. When TCNT is at 0, TNLn is set to 1 on the next rising edge of CLK for one cycle. This is to provide the start of structure indication to COBRA. Another counter CNT_SYNC is implemented to provide superframe alignment needed by the QDS1F. CNT_SYNC is a modulo-24 counter. When CNT_SYNC is at 0, TSYNC is set to 1 on the falling edge of CLK for one cycle. The diagram in Figure 13 shows the timing relationship.

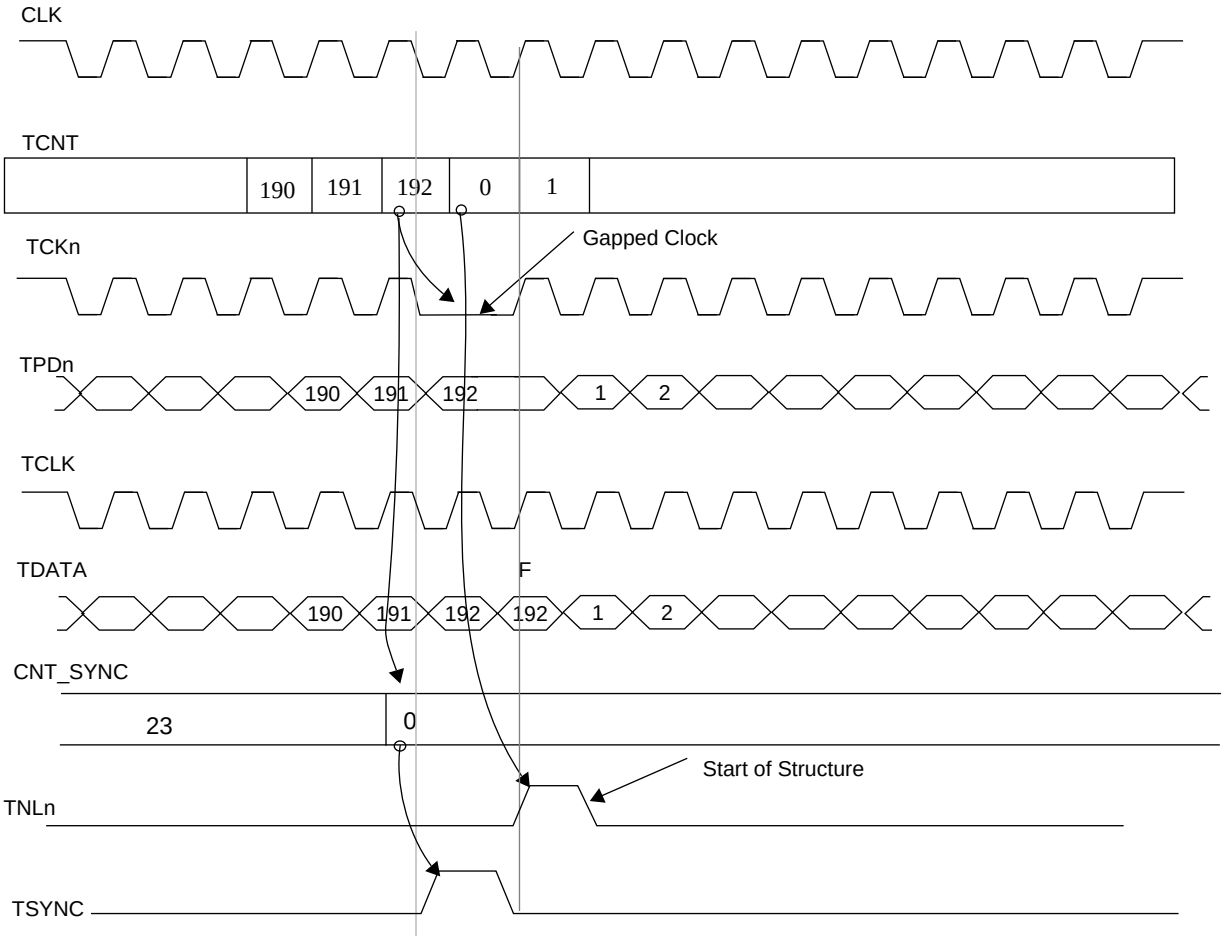


Figure 13. Structured Service - Line Output Timing

MULTIPLE COBRA DEVICES SHARING CELL INTERFACE

Figure 14 shows the interface between an ATM switching device (the TranSwitch CUBIT) and two COBRA devices. The important thing to note is that multiple COBRA devices can share the data bus of the cell interface. However, some glue logic is needed to arbitrate access to the interface by multiple COBRA devices. The CUBIT device acts as a master on the cell interface and the COBRA devices act as slaves. The COBRA devices are configured to be in UTOPIA mode and the COOE pin is tied low.

Cell Output Interface

In the cell output direction, each COBRA will assert its COCLAV output pin if it has a cell to send. Since each COBRA device tri-states its own COD(7-0) and COSOC pins until the COENB pin is asserted low, multiple COBRA devices can share the bus waiting for COENB to be asserted. The glue logic will read COCLAV from each of the COBRA devices and generate a single cell available (CLAV) signal to the CUBIT indicating if any of the COBRA devices has a cell to send. When the CUBIT is ready to receive a cell, it will generate an enable signal, CIENB. This enable signal must then be used by the glue logic to assert the COENB pin of the appropriate COBRA. A simple round-robin scheduling mechanism can be used.

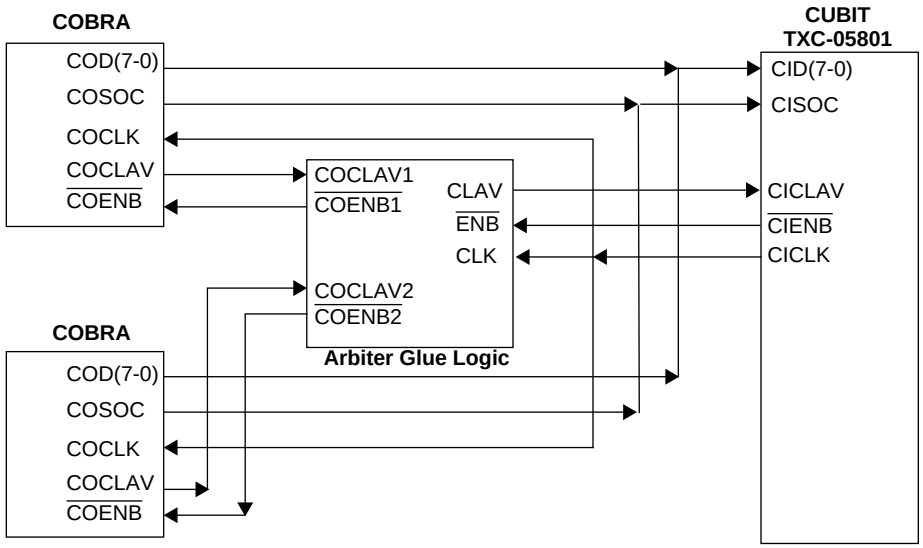
Cell Input Interface

The important issue to note on this interface is that each COBRA device can receive all cells from the CUBIT and will process only those cells that match the cell headers programmed internal to the device. Other cells are simply discarded. No extra lookup is required to identify which COBRA must receive a particular cell. However, due to the internal FIFO fill status of each COBRA, a particular COBRA may not be ready to accept a cell.

In the cell input direction, each COBRA will assert its CICLAV output signal if it has space to accept a cell. To avoid a need for additional FIFO memory external to the CUBIT, the glue logic may generate a cell available signal (CLAV) to the CUBIT only when all COBRA devices are ready to accept a cell. When the CUBIT is ready to transfer a cell, the glue logic can use its COENB output to generate the write enable signal CIWE to all COBRA devices.

The cell delay variation that may result due to the waiting time for CICLAV signals to be asserted from all COBRA devices is insignificant. Further, the CUBIT's outlet FIFO provides additional storage.

Cell Output Interface



Cell Input Interface

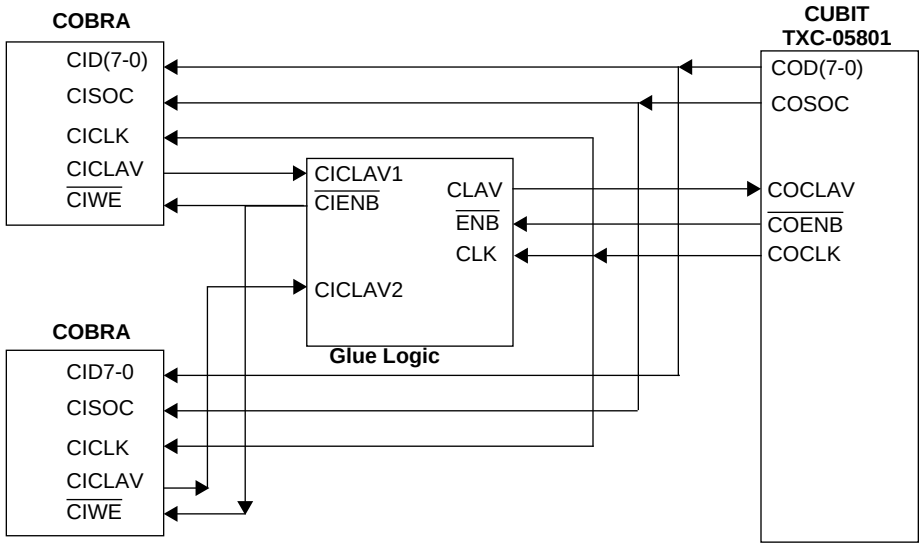


Figure 14. CUBIT Interface Design Example

SOFTWARE INITIALIZATION

The following example illustrates the initialization procedure that may be used by the device driver software to configure the COBRA device. The example is for an Unstructured service with external clocking on channel 0, with a partial fill of 24 bytes per cell.

On power-up, the device must first be reset by using the $\overline{\text{RESET}}$ pin, before performing initialization.

Operation	Address*	Data*	Comments
write	007	91	Reset COBRA.
write	007	00	Move from reset state to normal operating state.
write	00A	00	Enable all global interrupts.
write	00B	03	Generate interrupts on start and end of alarm indications (INTPOS=1, INTNEG=1).
write	00C	04	Disconnect PRBS generator and analyzer; select UNI mode; select all ones pattern for the dummy bytes of a partially filled cell.
write	00D	02	Select UTOPIA; no routing tag; disable HEC checking.
write	102	04	Enable all interrupts for channel 0 except interrupt on loss of structure pointer; LLOSP0 is masked since it is Unstructured service.
write	103	00	Disable channel 0 until configuration is finished; use NRZ mode; select falling edge as the active edge of the receive and transmit line clocks for channel 0.
write	104	00	Select normal AAL1 segmentation and reassembly operation for channel 0.
write	105	57	Select partial fill with NFILLD05-NFILLD00 = 23 decimal, indicating 24 data bytes per cell for channel 0.
write	106	00	Structure size is ignored for channel 0.
write	107	00	
write	108	10	Select Unstructured service; low latency mode sequence number checking; disable clock recovery; select external clocking (all for channel 0).
write	109	00	Set SRTS gain factor to 0 for channel 0.
write	10A	08	Select the half FIFO length to be 8 cells for channel 0.
write	10B-10D	00	These control bits are ignored since clock recovery is not used in this example for channel 0.
write	110-116	00	These control bits are ignored since routing tag is not used in this example for channel 0.
write	117	01	GFC =0; VPI=12H, VCI=2334H, PTI=0, CLP=0 (all for channel 0)
write	118	22	
write	119	33	
write	11A	40	
write	103	60	Enable channel 0 for segmentation and reassembly operation

* (Hexadecimal)

PIN DIAGRAM

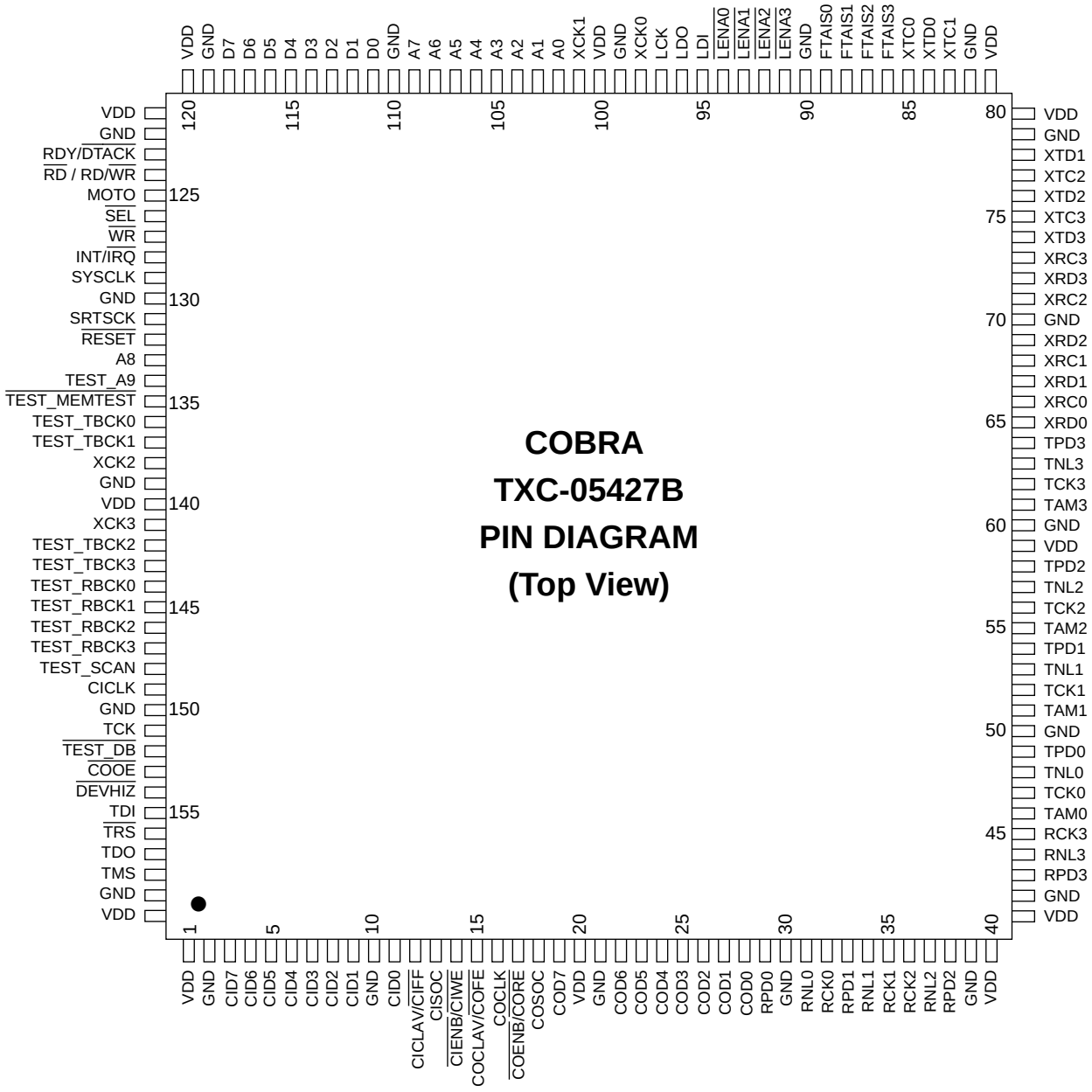


Figure 15. COBRA TXC-05427B Pin Diagram

PIN DESCRIPTIONS

POWER SUPPLY AND GROUND

Symbol	Pin No.	I/O/P*	Name/Function
VDD	1, 20, 40, 41, 59, 80, 81, 100, 120, 121, 140, 160	P	**V_{DD}:** +5 volts supply voltage, +/- 5%.
GND	2, 10, 21, 30, 39, 42, 50, 60, 70, 79, 82, 90, 99, 110, 119, 122, 130, 139, 150, 159	P	**Ground:** Zero volts reference.

*Note: I = Input; O = Output; P = Power; (T) = Tri-state

CELL INTERFACE SIGNALS

Symbol	Pin No.	I/O/P	Type *	Name/Function
CICLK	149	I	CMOS	**Cell Input Clock:** This clock input is used to write data into COBRA on the Cell Input interface. The frequency of this clock must be greater than three times the highest frequency of the four receive line clocks RCKn.
CID(7-1) CID0	3-9 11	I	TTL	**Cell Input Data Bus:** The cell input data bus carries the ATM cell octets that are written into COBRA. CID(7-0) are sampled on the falling edge of CICLK. CID0 is the LSB.
CISOC	13	I	TTL	**Cell Input Start of Cell:** The cell input start of cell signal marks the first byte of a cell. CISOC is sampled on the falling edge of CICLK.
CICLAV / $\overline{\text{CIFF}}$	12	O(T)	CMOS 4mA	**Cell Input Cell Available:** If UTOPIA = 1, COBRA will assert this signal high if it can accept a complete cell. At most four more bytes can be written into the FIFO after this signal is de-asserted low. This signal is output on the falling edge of CICLK. **Cell Input FIFO Full:** In synchronous FIFO mode (control bit UTOPIA = 0), COBRA will assert this signal low if the cell interface internal FIFO is full. At most two more bytes can be written into the FIFO after this signal is asserted low. This signal is output on the falling edge of CICLK.
$\overline{\text{CIENB}}$ / $\overline{\text{CIWE}}$	14	I	TTL	**Cell Input Enable:** Cell Input Enable if UTOPIA = 1 (active when low). This signal is sampled on the falling edge of CICLK. **Cell Input Write Enable:** Cell input write enable if UTOPIA = 0 (active when low). This signal is sampled on the falling edge of CICLK.
COCLK	16	I	CMOS	**Cell Output Clock:** This clock input is used to read data out from the cell output interface. The frequency of this clock must be greater than three times the highest frequency of the four transmit line clocks TCKn.

* Note: See Input, Output and I/O Parameters section for Type definitions.

Symbol	Pin No.	I/O/P	Type	Name/Function
COD7 COD(6-0)	19 22-28	O(T)	CMOS 4mA	**Cell Output Data Bus:** The cell output data bus carries the ATM cell octets and the routing tag that are read from COBRA. COD(7-0) are valid on the rising edge of COCLK. COD0 is the LSB.
COSOC	18	O(T)	CMOS 4mA	**Cell Output Start of Cell:** This cell output start of cell signal marks the first byte of a data transfer. This signal is asserted high during the first byte of a 53-byte cell if routing tags are not used. If routing tags are used and prefixed, this signal is asserted during the first byte of a routing tag. This signal is output on the rising edge of COCLK.
COCLAV / $\overline{\text{COFE}}$	15	O(T)	CMOS 4mA	**Cell Output Cell Available:** This signal is asserted high when COBRA has at least one complete cell to transfer. This signal is output on the rising edge of COCLK. **Cell Output FIFO Empty:** Cell FIFO empty indication if UTOPIA = 0. This signal is active when low. This signal is output on the rising edge of COCLK.
$\overline{\text{COENB}}$ / $\overline{\text{CORE}}$	17	I	TTL	**Cell Output Enable:** Cell Output Enable if UTOPIA = 1. This signal is active when low. This signal is sampled on the falling edge of COCLK. When this signal is high, COD(7-0) and COSOC pins are tri-stated. **Cell Output Read Enable:** Cell output read enable if UTOPIA = 0. This signal is active when low. This signal is sampled on the falling edge of COCLK. This signal does not tri-state the COD(7-0) and COSOC pins.
$\overline{\text{COOE}}$	153	I	TTL	**Cell Output Operation Enable:** This pin must be tied low when UTOPIA=1. When UTOPIA=0 and HECENA =0, this signal may be set high to tri-state the COD(7-0) and COSOC pins.

LINE INTERFACE PORT SIGNAL

Symbol	Pin No.	I/O/P	Type	Name/Function
RPD0 RPD1 RPD2 RPD3	29 33 38 43	I	TTL	**Receive Line Positive Rail Data/NRZ Data:** Serial positive rail input for the internal decoder when line coding is used. This pin provides the NRZ data when NRZ mode is selected. RPD0 is for channel 0, etc. See Note 1.
RNL0 RNL1 RNL2 RNL3	31 34 37 44	I	TTL	**Receive Line Negative Rail Data:** Serial negative rail input for the internal decoder when line coding is used. In NRZ and Unstructured mode, this pin provides the LOS indication. In NRZ and Structured service mode, this pin is the start of structure (first bit in the Structured frame) indicator. RNL0 is for channel 0, etc. See Note 1.

Note 1: See Figure 16, which is located after these pin description tables, for the effect of control bits on this pin.

Symbol	Pin No.	I/O/P	Type	Name/Function
RCK0 RCK1 RCK2 RCK3	32 35 36 45	I	TTL	**Receive Line Clock:** Rail or NRZ data is clocked into COBRA using the RPDn/RNLn signal leads on the falling edge of this clock when control bit RLCINV is 0. Rail or NRZ data is clocked in on the rising edge when control bit RLCINV is 1. RCK0 is for channel 0, etc. See Note 1.
TPD0 TPD1 TPD2 TPD3	49 54 58 64	O(T)	CMOS 2mA	**Transmit Line Positive Rail Data/NRZ Data:** Serial positive rail output when line coder is enabled. This pin is the serial NRZ output in the NRZ mode. TPD0 is for channel 0, etc. See Note 1.
TNL0 TNL1 TNL2 TNL3	48 53 57 63	I/O	TTL/ CMOS 2 mA	**Transmit Line Negative Rail Data:** This pin provides a negative rail interface from the internal coder when the line coder is enabled. In the NRZ, Structured service, and internal clock recovery mode, this pin is the start of structure (first bit in the Structured frame) indicator output. In the NRZ, Structured service and external clock mode, this pin is the start of structure indicator input. See Note 1.
TCK0 TCK1 TCK2 TCK3	47 52 56 62	I/O	TTL/ CMOS 2mA	**Transmit Line Clock:** If internal clock recovery is used, this pin is an output, else an input. Line data on TPDn/TNLn pins are clocked out on the falling edge of TCKn when control bit TLCINV is set to 0; otherwise they are clocked out on the rising edge of TCKn. See Note 1.
TAM0 TAM1 TAM2 TAM3	46 51 55 61	I/O	TTL/ CMOS 2mA	**Transmit Signal Activity Monitor:** Under normal operation, this pin is an input transmit signal activity monitor. When this signal goes high, a microprocessor interrupt is generated, indicating loss of activity on the line. Output mode is reserved for internal chip testing.
XRD0 XRD1 XRD2 XRD3	65 67 69 72	I/O	TTL/ CMOS 2 mA	**External Receive Line Data:** When EXTSIGn is set to 1, this pin outputs the data derived from the incoming serial line interfaces (i.e., RPDn/RNLn). AAL1 segmentation is not performed in this case. This output is updated on the rising edge of XRCn. Input mode is reserved for internal chip testing.
XRC0 XRC1 XRC2 XRC3	66 68 71 73	I/O	TTL/ CMOS 2 mA	**External Receive Line Clock:** When control bit EXTSIGn is set to 1, this lead outputs the clock derived from the incoming serial line interface clock. XRDn is updated on the rising edge of this clock. Input mode is reserved for internal chip testing.
XTD0 XTD1 XTD2 XTD3	84 78 76 74	I	TTL	**External Transmit Line Data:** When control bit EXTSIGn is set to 1, this external input is the source of transmitted line data signal. This signal is sent to the serial transmit lines (i.e., TPDn/TNLn). This input is sampled on the rising edge of XTCn.

Note 1: See Figure 16, which is located after these pin description tables, for the effect of control bits on this pin.

Symbol	Pin No.	I/O/P	Type	Name/Function
XTC0 XTC1 XTC2 XTC3	85 83 77 75	I	TTL	**External Transmit Line Clock:** When control bit EXTSIGn is set to 1, this external input clock is the source for transmitted clock signal. This clock is output onto the serial transmit clock (TCKn).
FTAIS0 FTAIS1 FTAIS2 FTAIS3	89 88 87 86	I	TTL	**Force Transmit AIS:** A high on this pin causes all ones AIS signal to be transmitted on the line output when the control bit EXTSIGn is set to 1.

CLOCK RECOVERY CLOCKS

Symbol	Pin No.	I/O/P	Type	Name/Function
SRTSCK	131	I	CMOS	**Network Reference Clock**: This clock is used to generate the SRTS time stamp. The frequency of this clock is dependent on the serial input clock, e.g., 2.43 MHz for DS1/E1 operation. This clock is divided by a factor defined by control bits REFDIVn (raised to the power of 2) and then used as the network reference clock. This clock must be a stratum 1 reference clock for accurate clock recovery when using SRTS.
XCK0 XCK1 XCK2 XCK3	98 101 138 141	I	CMOS	**Recovery Loop Clock:** This clock is used by the SRTS clock recovery loop. The clock frequency is 31.5 times the serial line clock frequency if control bit DIVRATn **=** 0 or 9.5 times the serial clock frequency if DIVRATn = 1. For example, for DS1 frequency of 1.544 MHz, XCKn is 48.636 MHz when DIVRATn **=** 0. The clock frequency tolerance is +/- 50 ppm and the clock duty cycle requirement is (50 +/- 10) %.

SERIAL LINE CONTROL

Symbol	Pin No.	I/O/P	Type	Name/Function
$\overline{\text{LENA0}}$ $\overline{\text{LENA1}}$ $\overline{\text{LENA2}}$ $\overline{\text{LENA3}}$	94 93 92 91	O(T)	CMOS 2 mA	**Line Interface Enable:** This active low signal enables the serial port on the external line interface device. When asserted, data can be written to, or read from, the line interface.
LCK	97	O(T)	CMOS 2 mA	**Line Interface Port Serial Channel Clock:** This signal is used to shift data to and from the line interface serial port. LCK clock rate is SYSCLK divided by 16.

Symbol	Pin No.	I/O/P	Type	Name/Function
LDO	96	O(T)	CMOS 2 mA	**Line Interface Port Serial Channel Data Out:** This is the serial data output to the line interface device. This output is shared among the four channels. This output is updated on the falling edge of LCK. For most commercial line transceivers, the first bit is a Read/Write command and it is followed by seven address bits. The second byte is data. This output is tri-stated when there is no read/write activity on the serial port.
LDI	95	I	TTL	**Line Interface Port Serial Channel Data In:** This is the serial data input from the line interface device. This input is shared among the four channels. The input data is sampled on the falling edge of LCK. The data received on this pin can be read via the microprocessor interface.

MICROPROCESSOR BUS INTERFACE

Symbol	Pin No.	I/O/P	Type	Name/Function
A8 A7 A6 A5 A4 A3 A2 A1 A0	133 109 108 107 106 105 104 103 102	I	TTL	**Address:** These are address line inputs that are used by the microprocessor for accessing COBRA internal registers for a read/write cycle. A0 is the LSB. High is logic 1.
D7 D6 D5 D4 D3 D2 D1 D0	118 117 116 115 114 113 112 111	I/O(T)	TTL/ TTL 8 mA	**Data:** Bi-directional data lines used for transferring data between COBRA internal registers and an external microprocessor. D0 is the LSB. High is logic 1. These pins are tri-stated when SEL is high.
SYSCLK	129	I	CMOS	**System Clock:** This clock is used by the COBRA device to run the microprocessor interface block and internal state machines. Maximum SYSCLK clock rate is 25 MHz. The system clock rate must be greater than each of the line clocks (RCKn).
INT / IRQ	128	O(T)	TTL 4 mA	**Interrupt:** Intel Mode - A high on this output pin signals an interrupt request to the microprocessor. Motorola Mode - A low on this output pin signals an interrupt request to the microprocessor.

Symbol	Pin No.	I/O/P	Type	Name/Function
MOTO	125	I	TTL	**Motorola/Intel Microprocessor Select:** This pin defines the operating mode of the microprocessor port. A high selects the Motorola microprocessor compatible bus interface. A low selects the Intel microprocessor compatible bus interface.
$\overline{RD}$ / RD/ $\overline{WR}$	124	I	TTL	**Read or Read/Write:** Intel Mode - Active low read enable signal for microprocessor read cycle. Motorola Mode - A high signal is used to read COBRA internal registers, i.e., read cycle. A low signal is used to write to COBRA internal registers, i.e., write cycle.
RDY/ $\overline{DTACK}$	123	O(T)	OD TTL 8 mA	**Ready or Data Transfer Acknowledge:** Intel Mode - A high is an acknowledgment from the addressed RAM location that the transfer can be completed. A low indicates that COBRA cannot complete the transfer cycle, and microprocessor wait states must be generated. Motorola Mode - During a read bus cycle, a low signal indicates that the information on the data bus is valid. During a write bus cycle, a low signal acknowledges the acceptance of data.
$\overline{RESET}$	132	I	TTLp	**Device Reset:** This active low signal will reset the entire device.
$\overline{SEL}$	126	I	TTLp	**Select:** This signal enables the microprocessor interface and allows the transfer of information between COBRA and the microprocessor. The data bus pins D(7-0) are tri-stated when $\overline{SEL}$ is high.
$\overline{WR}$	127	I	TTL	**Write:** Intel Mode **-** Active low write enable signal for microprocessor write cycle. Motorola Mode - This pin is unused and should be connected to V_{DD}.

TEST ACCESS PORT SIGNALS

Symbol	Pin No.	I/O/P	Type	Name/Function
TCK	151	I	TTL	**IEEE 1149.1 Test Port Serial Scan Clock:** This signal is used to shift data into TDI on the rising edge, and out of TDO on the falling edge.
TMS	158	I	TTLp	**IEEE 1149.1 Test Port Mode Select:** TMS is sampled on the rising edge of TCK, and is used to place the test access port controller into various states as defined in IEEE 1149.1.
TDI	155	I	TTLp	**IEEE 1149.1 Test Port Serial Scan Data In:** Serial test instructions and data are clocked into this pin on the rising edge of TCK.
TDO	157	O(T)	TTL 4 mA	**IEEE 1149.1 Test Port Serial Scan Data Out:** Serial test instructions and data are clocked out of this pin on the falling edge of TCK.
$\overline{\text{TRS}}$	156	I	TTLp	**IEEE 1149.1 Test Port Reset Pin:** This signal will synchronously reset the test access port (TAP) controller. Upon power-up, $\overline{\text{TRS}}$ must be set low. This will set the device into boundary scan bypass mode i.e., normal operation.
$\overline{\text{DEVHIZ}}$	154	I	TTLp	**Device High Impedance:** This asynchronous input pin, when driven low, will place all of the COBRA output pins in a high impedance state, except for RDY and TDO.

*p indicates internal pull-up to VDD.

INTERNAL TEST SIGNALS

Symbol	Pin No.	I/O/P	Type	Name/Function
TEST_A9	134	I	TTL	**Manufacturing Test pin:** Connect to ground.
$\overline{\text{TEST\_MEMTEST}}$	135	I	TTL	**Manufacturing Test pin:** Connect to V_{DD}.
TEST_TBCK0 TEST_TBCK1 TEST_TBCK2 TEST_TBCK3	136 137 142 143	O(T)	CMOS 2 mA	**Manufacturing Test pin:** Do not connect this pin, leave it floating.
TEST_RBCK0 TEST_RBCK1 TEST_RBCK2 TEST_RBCK3	144 145 146 147	O(T)	CMOS 2 mA	**Manufacturing Test pin:** Do not connect this pin, leave it floating.
TEST_SCAN	148	I	TTL	**Manufacturing Test pin:** Connect to ground.
$\overline{\text{TEST\_DB}}$	152	I	TTLp	**Manufacturing Test pin:** Connect to V_{DD}.

Figure 16. Effect of Mode Control Bits on Line Interface Data and Clock Pins

PIN	Unstructured Service STRUn = 0				Structured Service STRUn = 1			
	Internal Clock Recovery CLKn = 0		External Clock CLKn = 1		Internal Clock Recovery CLKn = 0		External Clock CLKn = 1	
	LCn ≠ 00	LCn = 00	LCn ≠ 00	LCn = 00	LCn ≠ 00	LCn = 00	LCn ≠ 00	LCn = 00
TCKn	Clock Output		Clock Input		Clock Output		Clock Input	
TPDn	Positive Rail Data Output	NRZ Data Output	Positive Rail Data Output	NRZ Data Output	NRZ Data Output			
TNLn	Negative Rail Data Output	Unused	Negative Rail Data Output	Unused	Frame Output		Frame Input	
RCKn	Clock Input							
RPDn	Positive Rail Data Input	NRZ Data Input	Positive Rail Data Input	NRZ Data Input	NRZ Data Input			
RNLn	Negative Rail Data Input	LOSn Input	Negative Rail Data Input	LOSn Input	Frame Input			

Notes:
1. The signal pin and control bit symbol suffix "n" represents the associated channel number, 0 - 3.
2. LCn means the combination of bits LCn1 and LCn0.
3. ≠ means "not equal to".

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min *	Max *	Unit
Supply voltage	V_{DD}	-0.3	+7.0	V
DC input voltage	V_{IN}	-0.5	V_{DD} + 0.5	V
Operating junction temperature	T_J		+150	^oC
Storage temperature range	T_S	-55	+150	^oC

*Note: Operating conditions exceeding those listed in Absolute Maximum Ratings may cause permanent failure. Exposure to absolute maximum ratings for extended periods may impair device reliability.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal resistance - junction to ambient			32	$^oC/W$	0 ft/min linear airflow

RECOMMENDED OPERATING CONDITIONS AND POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
Ambient Operating Temperature, T_A	-40		+85	^oC	0 ft/min linear airflow
V_{DD}	+4.75	+5.0	+5.25	V	
I_{DD}			140	mA	
Power Dissipation, P_{DD}			735	mW	

INPUT, OUTPUT AND I/O PARAMETERS

INPUT PARAMETERS FOR CMOS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	V_{DD} x 0.7			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			V_{DD} x 0.3	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			+10	µA	V_{DD} = 5.25
Input capacitance		5.1		pF	

INPUT PARAMETERS FOR TTL

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	+2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			+0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			+10	µA	V_{DD} = 5.25
Input capacitance		5.1		pF	

INPUT PARAMETERS FOR TTLp, INPUT PADS WITH INTERNAL 25 µA PULL UP

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	+2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			+0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			+25	µA	V_{DD} = 5.25
Input capacitance		5.1		pF	

OUTPUT PARAMETERS FOR CMOS 2 mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.8			V	V_{DD} = 4.75; I_{OH} = -2.0
V_{OL}			+0.5	V	V_{DD} = 4.75; I_{OL} = 2.0
I_{OL}			+2.0	mA	
I_{OH}			-2.0	mA	
t_{RISE}		4.5		ns	C_{LOAD} = 15 pF
t_{FALL}		3.7		ns	C_{LOAD} = 15 pF

OUTPUT PARAMETERS FOR CMOS 4 mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.8			V	V_{DD} = 4.75; I_{OH} = -4.0
V_{OL}			+0.5	V	V_{DD} = 4.75; I_{OL} = 4.0
I_{OL}			+4.0	mA	
I_{OH}			-4.0	mA	
t_{RISE}		2.2		ns	C_{LOAD} = 15 pF
t_{FALL}		1.9		ns	C_{LOAD} = 15 pF

OUTPUT PARAMETERS FOR TTL 4 mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.8			V	V_{DD} = 4.75; I_{OH} = -4.0
V_{OL}			+0.4	V	V_{DD} = 4.75; I_{OL} = 4.0
I_{OL}			+4.0	mA	
I_{OH}			-4.0	mA	
t_{RISE}		4.5		ns	C_{LOAD} = 15 pF
t_{FALL}		1.8		ns	C_{LOAD} = 15 pF

OUTPUT PARAMETERS FOR TTL 8 mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.8			V	V_{DD} = 4.75; I_{OH} = -8.0
V_{OL}			+0.4	V	V_{DD} = 4.75; I_{OL} = 8.0
I_{OL}			+8.0	mA	
I_{OH}			-8.0	mA	
t_{RISE}		3.5		ns	C_{LOAD} = 15 pF
t_{FALL}		1.7		ns	C_{LOAD} = 15 pF

OUTPUT PARAMETERS FOR OPEN DRAIN (OD) TTL 8 mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OL}			+0.5	V	V_{DD} = 4.75; I_{OL} = 8.0
I_{OL}			+8.0	mA	
t_{FALL}		1.7		ns	C_{LOAD} = 15 pF

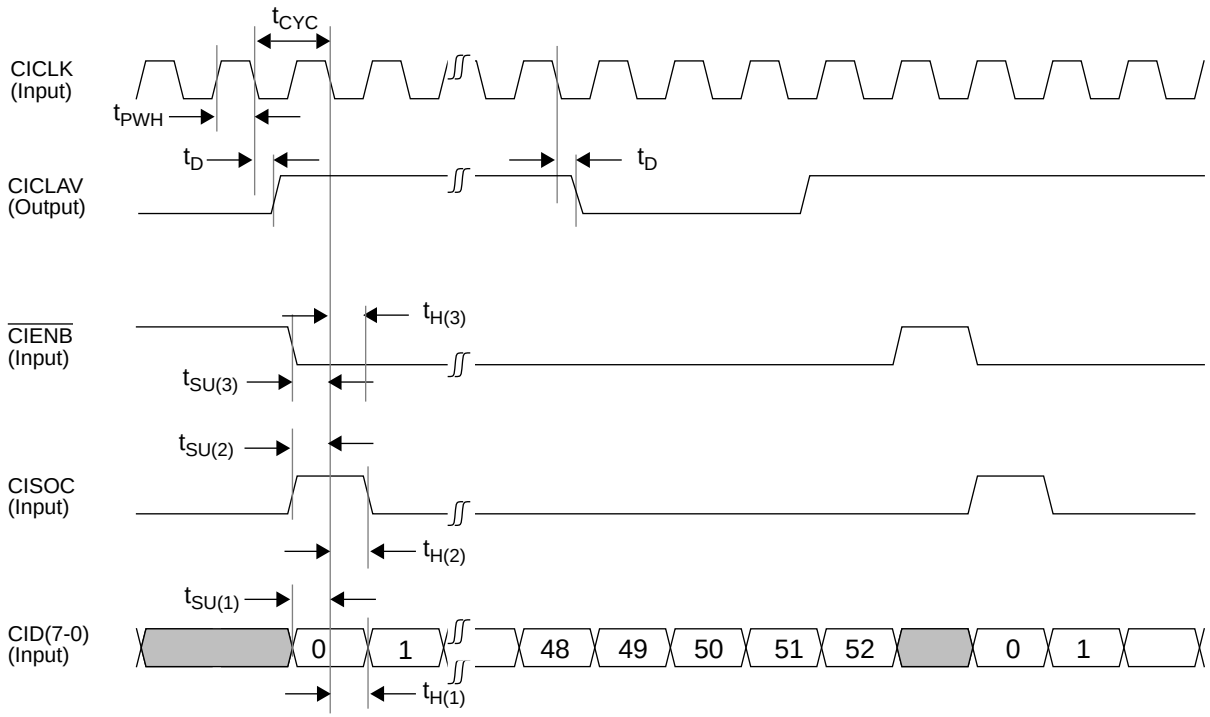
INPUT/OUTPUT PARAMETERS FOR TTL/CMOS 2mA

See tables above entitled Input Parameters for TTL and Output Parameters for CMOS 2mA.

TIMING CHARACTERISTICS

Detailed timing diagrams for COBRA are illustrated in Figures 17 through 29, with values of the timing intervals tabulated below each diagram. All output times are measured with a maximum 25 pF load capacitance. Timing instants (shown as vertical dashed lines) are all measured at voltage values of $(V_{IL} + V_{IH})/2$ for input signals and $(V_{OL} + V_{OH})/2$ for output signals.

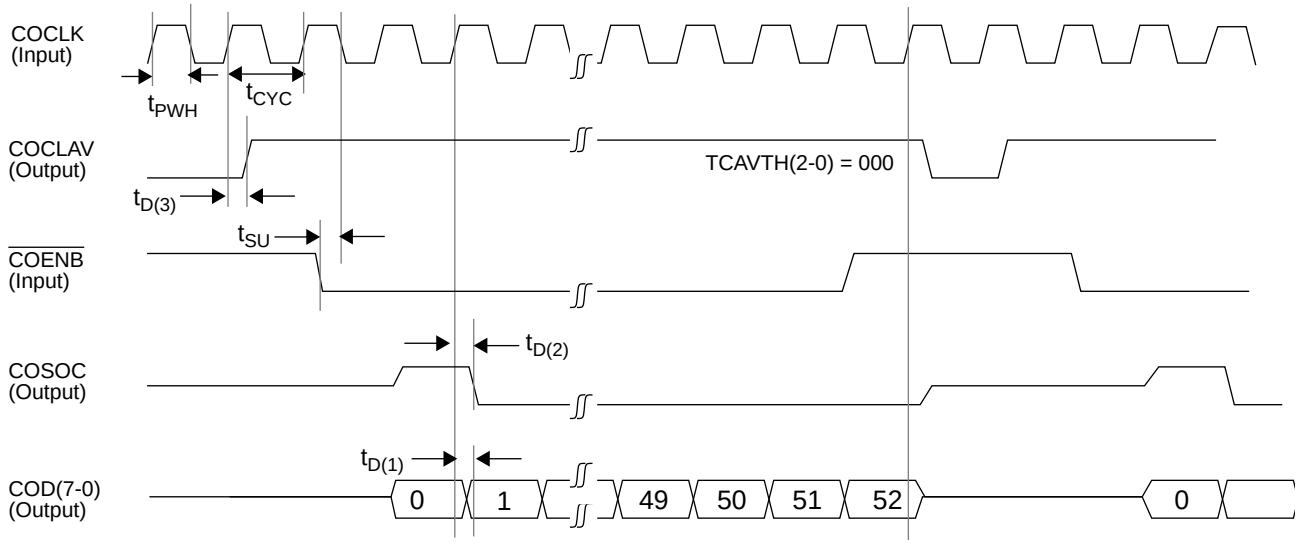
Figure 17. Cell Receive Timing (UTOPIA mode)



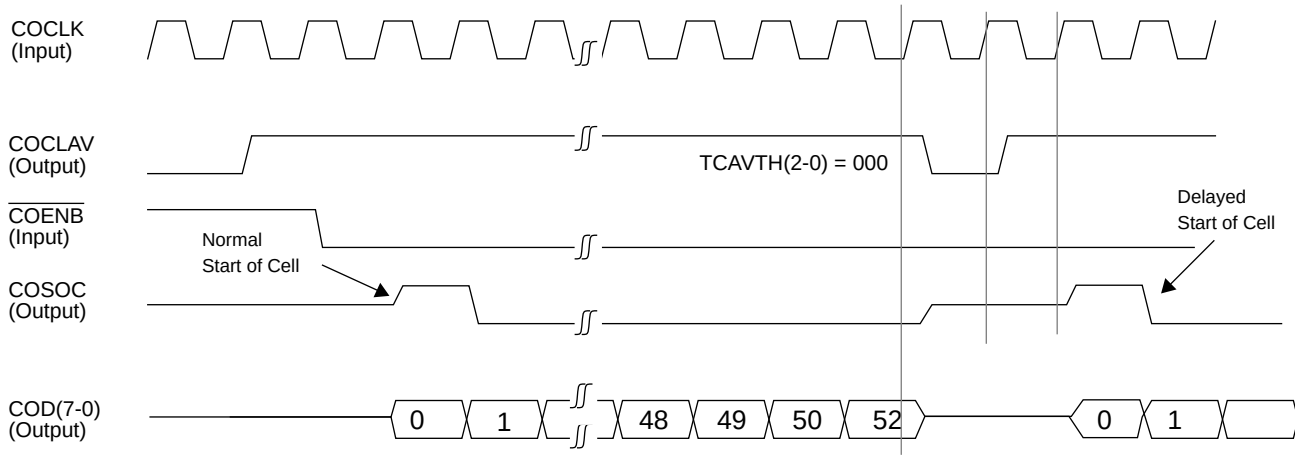
Parameter	Symbol	Min	Typ	Max	Unit
CICLK clock period	t_{CYC}	40			ns
CICLK duty cycle, t_{PWH}/t_{CYC}		40		60	%
CID(7-0) set-up time to CICLK↓	$t_{SU(1)}$	10			ns
CID(7-0) hold time after CICLK↓	$t_{H(1)}$	6			ns
CISOC set-up time to CICLK↓	$t_{SU(2)}$	10			ns
CISOC hold time after CICLK↓	$t_{H(2)}$	6			ns
$\overline{\text{CIENB}}$ set-up time to CICLK↓	$t_{SU(3)}$	10			ns
$\overline{\text{CIENB}}$ hold time after CICLK↓	$t_{H(3)}$	5			ns
CICLAV delay after CICLK↓	t_D	4		19	ns

Figure 18. Cell Transmit Timing (UTOPIA mode)

The following diagram illustrates the timing under normal UTOPIA conditions, where the $\overline{\text{COENB}}$ signal is asserted low after COCLAV goes high. Note that the setup time for $\overline{\text{COENB}}$ is specified with respect to the falling edge of COCLK.



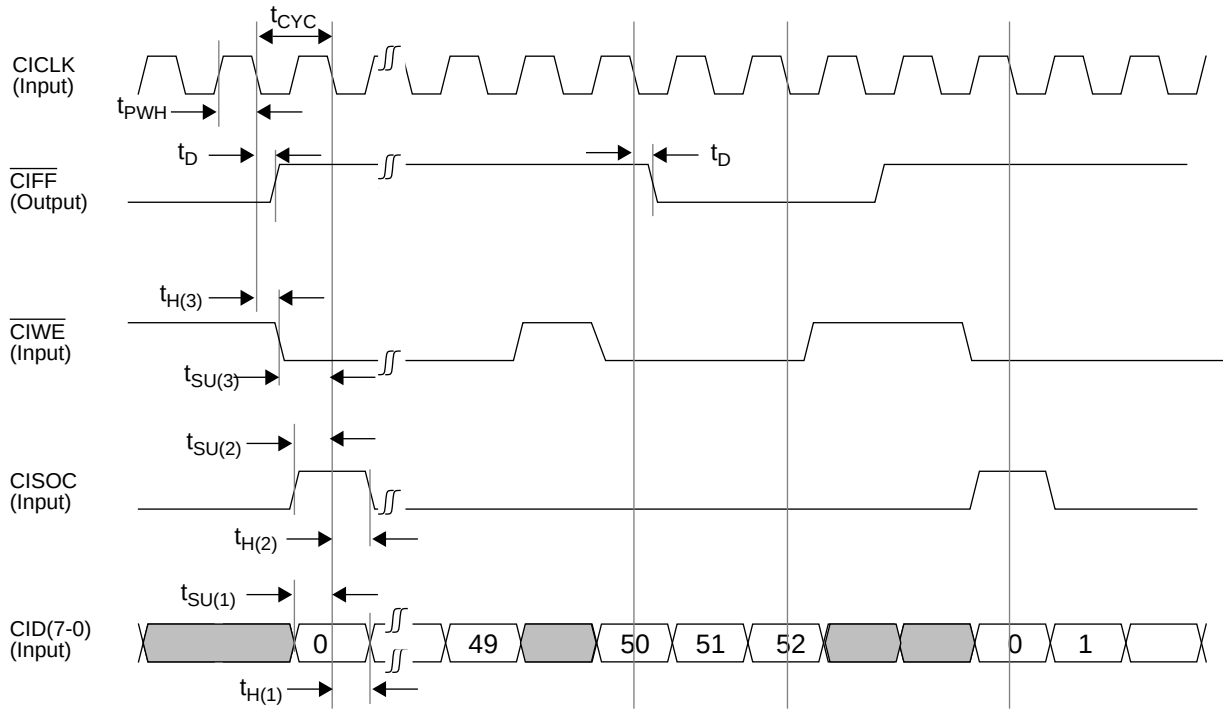
The following diagram shows the timing of COSOC and COD(7-0) if $\overline{\text{COENB}}$ is asserted active low prior to COCLAV being asserted high. During the second cell transfer, COSOC appears one cycle after COCLAV goes high. The timing parameters are the same as those shown in the diagram above.



Parameter	Symbol	Min	Typ	Max	Unit
COCLK clock period	t_{CYC}	40			ns
COCLK duty cycle, t_{PWH}/t_{CYC}		40		60	%
COD(7-0) data delay after COCLK↑	$t_{D(1)}$	1		19	ns
COSOC delay after COCLK↑	$t_{D(2)}$	1		19	ns
COCLAV delay after COCLK↑	$t_{D(3)}$	1		19	ns
$\overline{\text{COENB}}$ set-up time to COCLK↓	t_{SU}	10			ns

Note: If a prefixed routing tag is used, COSOC is asserted during the first byte of the routing tag.

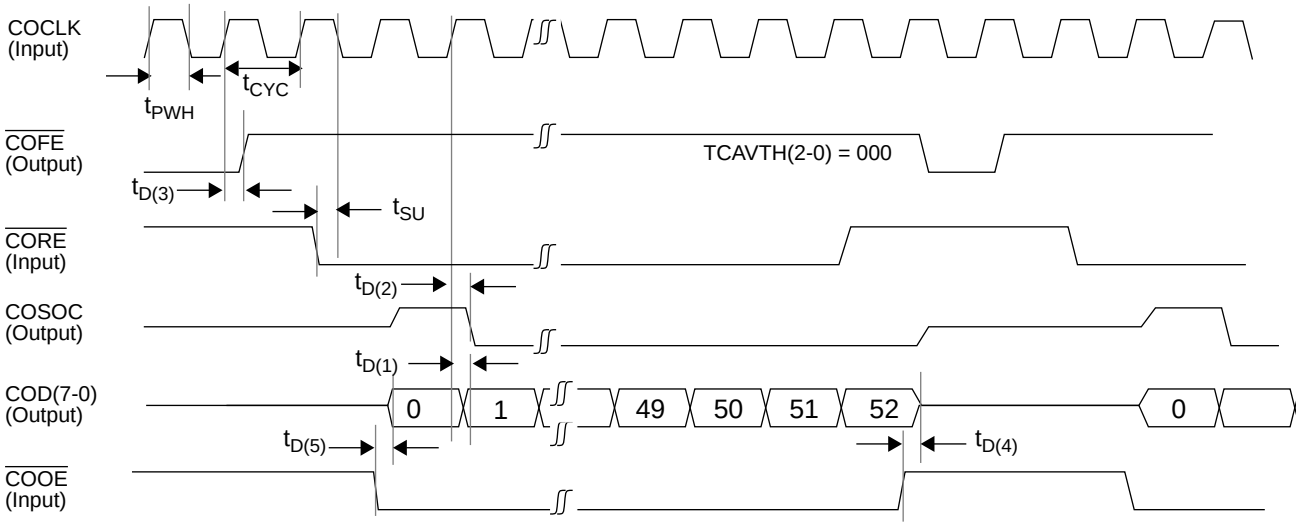
Figure 19. Cell Receive Timing (Synchronous FIFO mode)



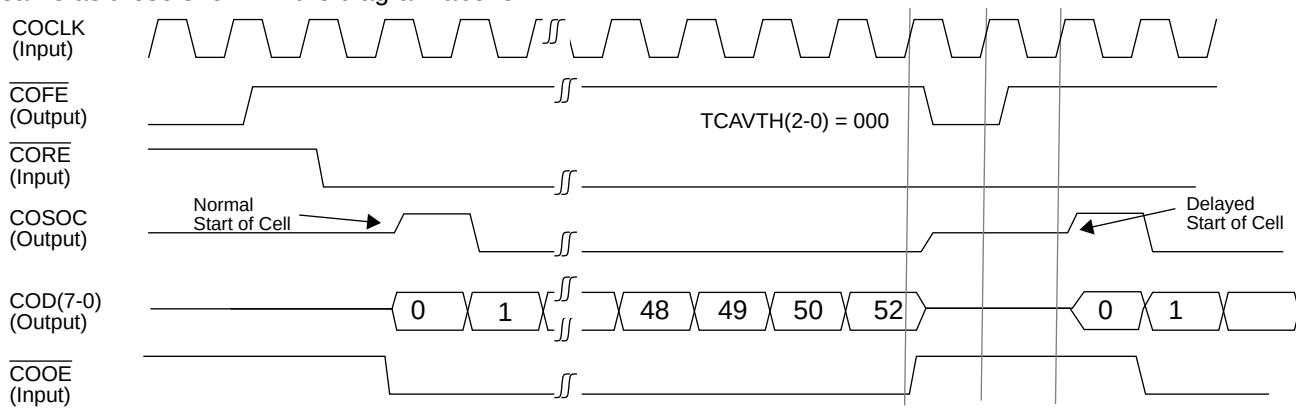
Parameter	Symbol	Min	Typ	Max	Unit
CICLK clock period	t_{CYC}	40			ns
CICLK duty cycle, t_{PWH}/t_{CYC}		40		60	%
CID(7-0) set-up time to CICLK↓	$t_{SU(1)}$	10			ns
CID(7-0) hold time after CICLK↓	$t_{H(1)}$	6			ns
CISOC set-up time to CICLK↓	$t_{SU(2)}$	10			ns
CISOC hold time after CICLK↓	$t_{H(2)}$	6			ns
$\overline{\text{CIWE}}$ set-up time to CICLK↓	$t_{SU(3)}$	10			ns
$\overline{\text{CIWE}}$ hold time after CICLK↓	$t_{H(3)}$	5			ns
$\overline{\text{CIFF}}$ delay after CICLK↓	t_D	4		19	ns

Figure 20. Cell Transmit Timing (Synchronous FIFO mode)

The following diagram illustrates the timing under normal conditions, where the $\overline{\text{CORE}}$ signal is asserted low after $\overline{\text{COFE}}$ goes high. Note that the setup time for $\overline{\text{CORE}}$ is specified with respect to the falling edge of COCLK.



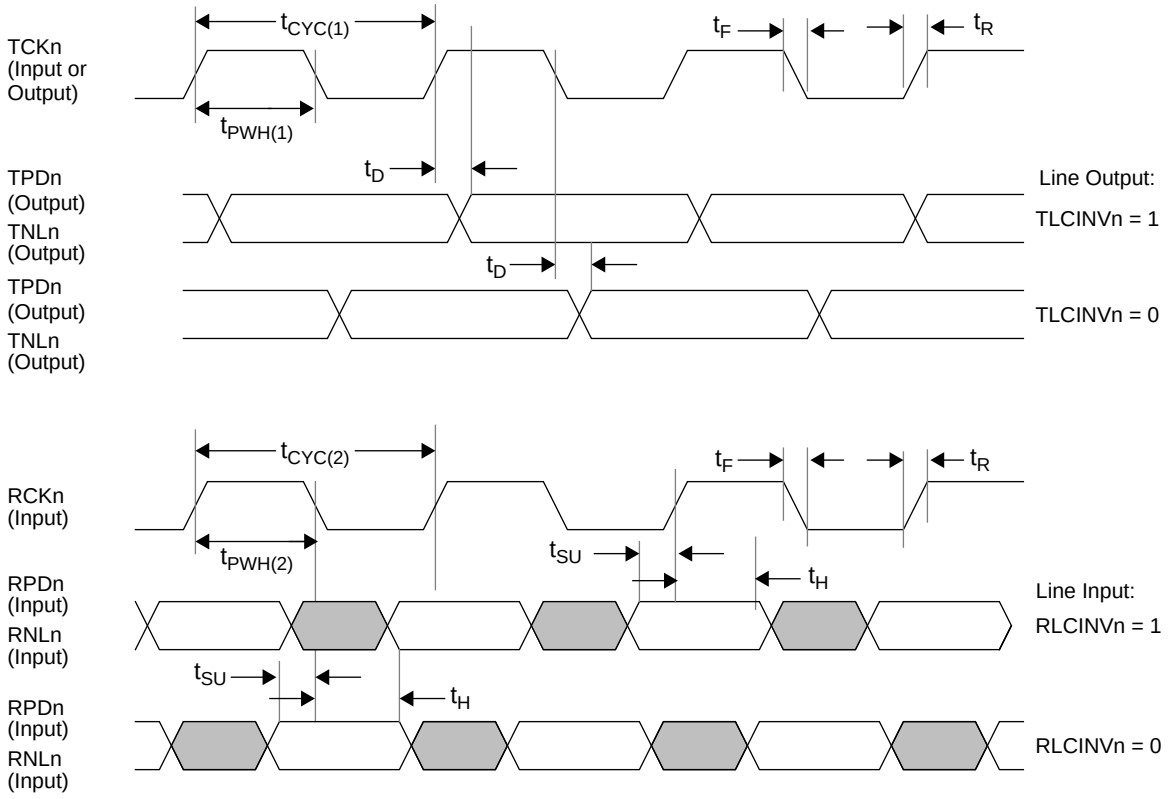
The following diagram shows the timing of COSOC and COD(7-0) if $\overline{\text{CORE}}$ is asserted active low prior to $\overline{\text{COFE}}$ being asserted high. COSOC appears one cycle after $\overline{\text{COFE}}$ goes high. The timing parameters are the same as those shown in the diagram above.



Parameter	Symbol	Min	Typ	Max	Unit
COCLK clock period	t_{CYC}	40			ns
COCLK duty cycle, t_{PWH}/t_{CYC}		40		60	%
COD(7-0) data delay after COCLK↑	$t_{D(1)}$	4		19	ns
COSOC delay after COCLK↑	$t_{D(2)}$	4		19	ns
$\overline{\text{CORE}}$ setup time to COCLK ↓	t_{SU}	10			ns
$\overline{\text{COFE}}$ Delay after COCLK↑	$t_{D(3)}$	1		19	ns
COD(7-0) data delay to high Z after $\overline{\text{COOE}}$↑	$t_{D(4)}$	1		19	ns
COD(7-0) data delay after $\overline{\text{COOE}}$↓	$t_{D(5)}$	1		19	ns

Note: If a prefixed routing tag is used, COSOC is asserted during the first byte of the routing tag.

Figure 21. Line I/O Timing for T1/E1 or Other Unstructured Signals

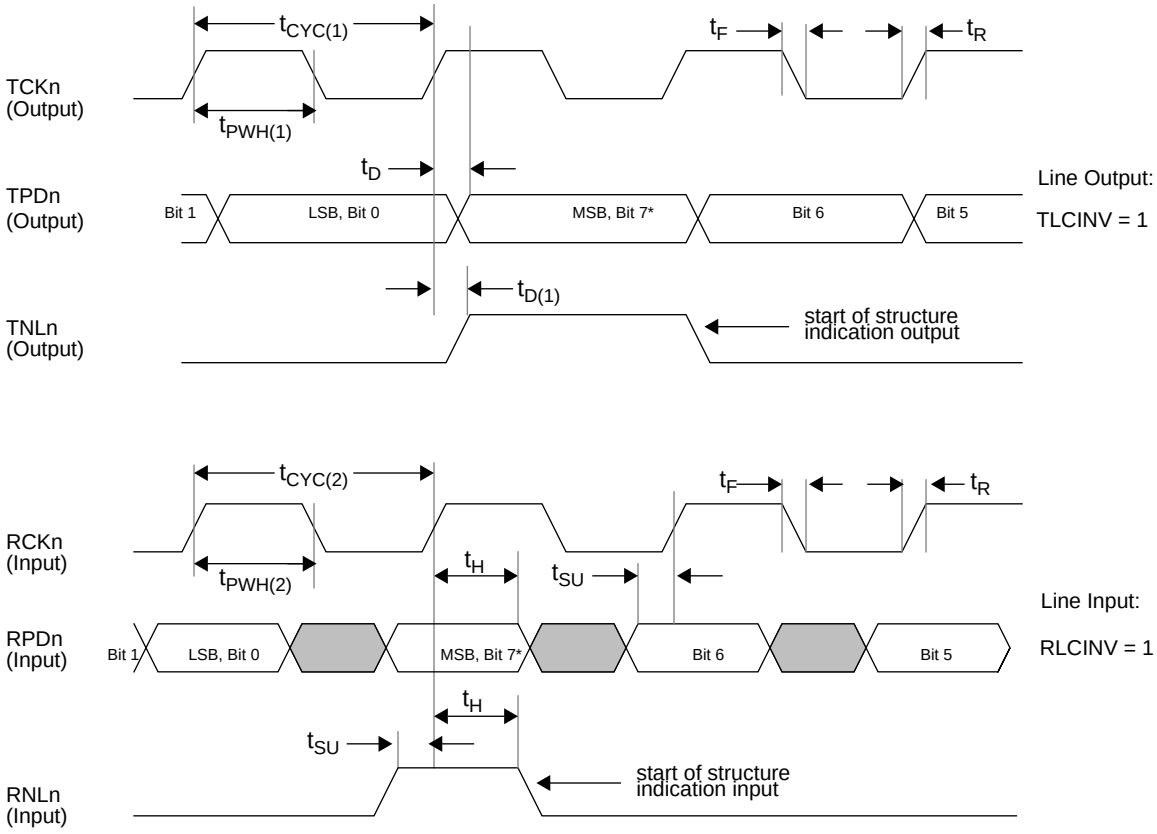


Parameter	Symbol	Min	Typ	Max	Unit
TCKn clock period	$t_{CYC(1)}$	117			ns
TCKn duty cycle, $t_{PWH(1)}/t_{CYC(1)}$		40		60	%
TPDn/TNLn delay after TCKn↑/↓ (Note 1)	t_D			24	ns
RCKn clock period	$t_{CYC(2)}$	117			ns
RCKn duty cycle, $t_{PWH(2)}/t_{CYC(2)}$		40		60	%
RPDn/RNLn setup time to RCKn↑/↓ (Note 2)	t_{SU}	10			ns
RPDn/RNLn hold time after RCKn↑/↓ (Note 2)	t_H	5			ns
TCKn, RCKn rise time (Note 3)	t_R		3		ns
TCKn, RCKn fall time (Note 3)	t_F		3		ns

Notes:

1. The active edge of TCKn may be selected via control bit TLCINVn, as shown in this diagram.
2. The active edge of RCKn may be selected via control bit RLCINVn, as shown in this diagram.
3. Rise and fall times are measured between 10% and 90% of the V_{IL}/V_{IH} or V_{OL}/V_{OH} range, as applicable.

Figure 22. Line I/O Timing in Structured Service, Internal Clocking Mode



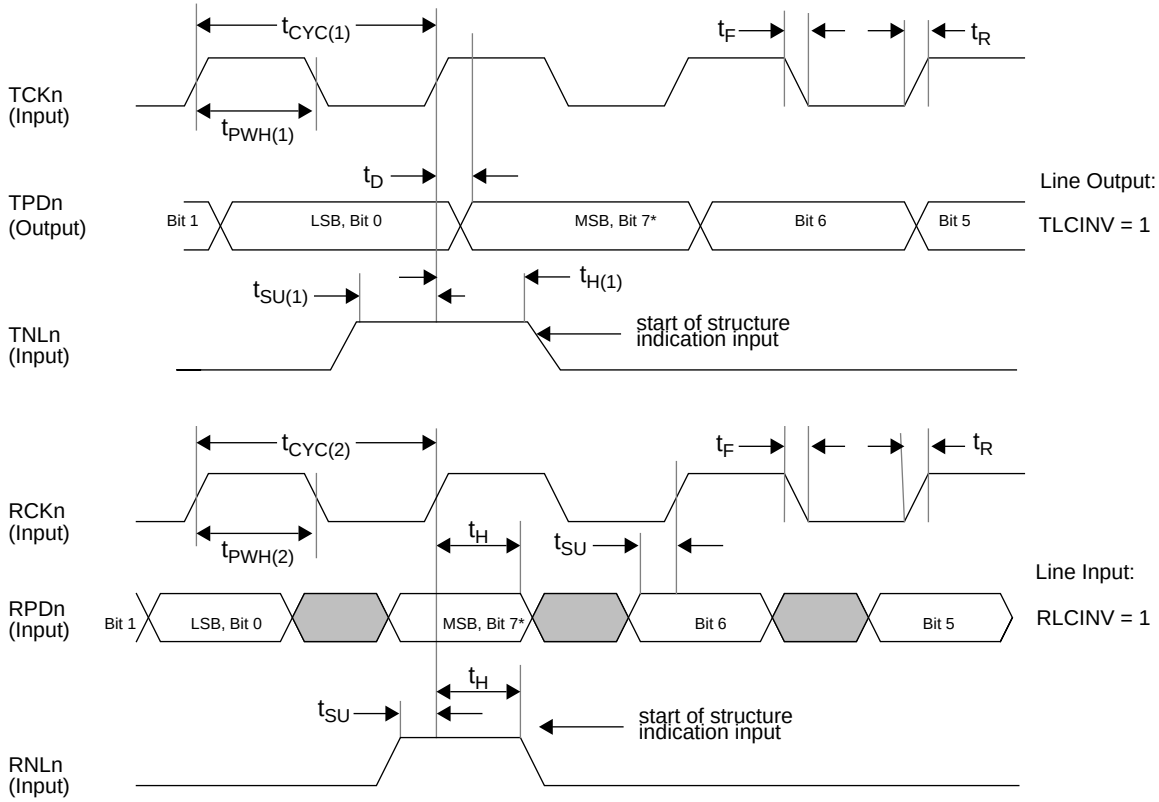
* MSB, Bit 7 is the first bit of the first byte of a structure.

Parameter	Symbol	Min	Typ	Max	Unit
TCKn clock period	$t_{CYC(1)}$	117			ns
TCKn duty cycle, $t_{PWH(1)}/t_{CYC(1)}$		40		60	%
TPDn data delay after TCKn↑ (Note 1)	t_D	1		24	ns
TNLn delay after TCKn↑ (Note 1)	$t_{D(1)}$	1		24	ns
RCKn clock period	$t_{CYC(2)}$	117			ns
RCKn duty cycle, $t_{PWH(2)}/t_{CYC(2)}$		40		60	%
RPDn data and RNLn setup time before RCKn↑ (Note 2)	t_{SU}	10			ns
RPDn data and RNLn hold time after RCKn↑ (Note 2)	t_H	5			ns
TCKn, RCKn rise time (Note 3)	t_R		3		ns
TCKn, RCKn fall time (Note 3)	t_F		3		ns

Notes:

1. The active edge of TCKn may be selected via bit TLCINVn; in this diagram, TLCINVn is set to 1 to select the rising edge.
2. The active edge of RCKn may be selected via bit RLCINVn; in this diagram, RLCINVn is set to 1 to select the rising edge.
3. Rise and fall times are measured between 10% and 90% of the V_{IL}/V_{IH} or V_{OL}/V_{OH} range, as applicable.

Figure 23. Line I/O Timing in Structured Service, External Clocking Mode



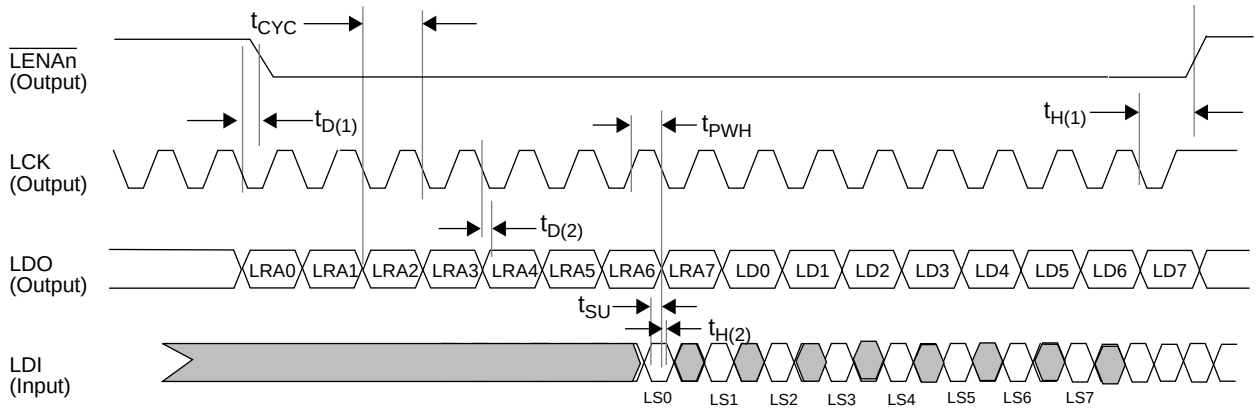
* MSB, Bit 7 is the first bit of the first byte of a structure.

Parameter	Symbol	Min	Typ	Max	Unit
TCKn clock period	$t_{CYC(1)}$	117			ns
TCKn duty cycle, $t_{PHW(1)}/t_{CYC(1)}$		40		60	%
TPDn data delay after TCKn↑ (Note 1)	t_D	1		24	ns
TNLn setup time before TCKn↑ (Note 1)	$t_{SU(1)}$	10			ns
TNLn hold time after TCKn↑ (Note 1)	$t_{H(1)}$	1			ns
RCKn clock period	$t_{CYC(2)}$	117			ns
RCKn duty cycle, $t_{PHW(2)}/t_{CYC(2)}$		40		60	%
RPDn data and RNLn setup time to RCKn/TCKn↑ (Note 1)	t_{SU}	10			ns
RPDn data and RNLn hold time after RCKn/TCKn↑ (Note 1)	t_H	5			ns
TCKn, RCKn rise time (Note 3)	t_R		3		ns
TCKn, RCKn fall time (Note 3)	t_F		3		ns

Notes:

1. The active edge of TCKn may be selected via bit TLCINVn; in this diagram, TLCINVn is set to 1 to select the rising edge.
2. The active edge of RCKn may be selected via bit RLCINVn; in this diagram, RLCINVn is set to 1 to select the rising edge.
3. Rise and fall times are measured between 10% and 90% of the V_{IL}/V_{IH} or V_{OL}/V_{OH} range, as applicable.

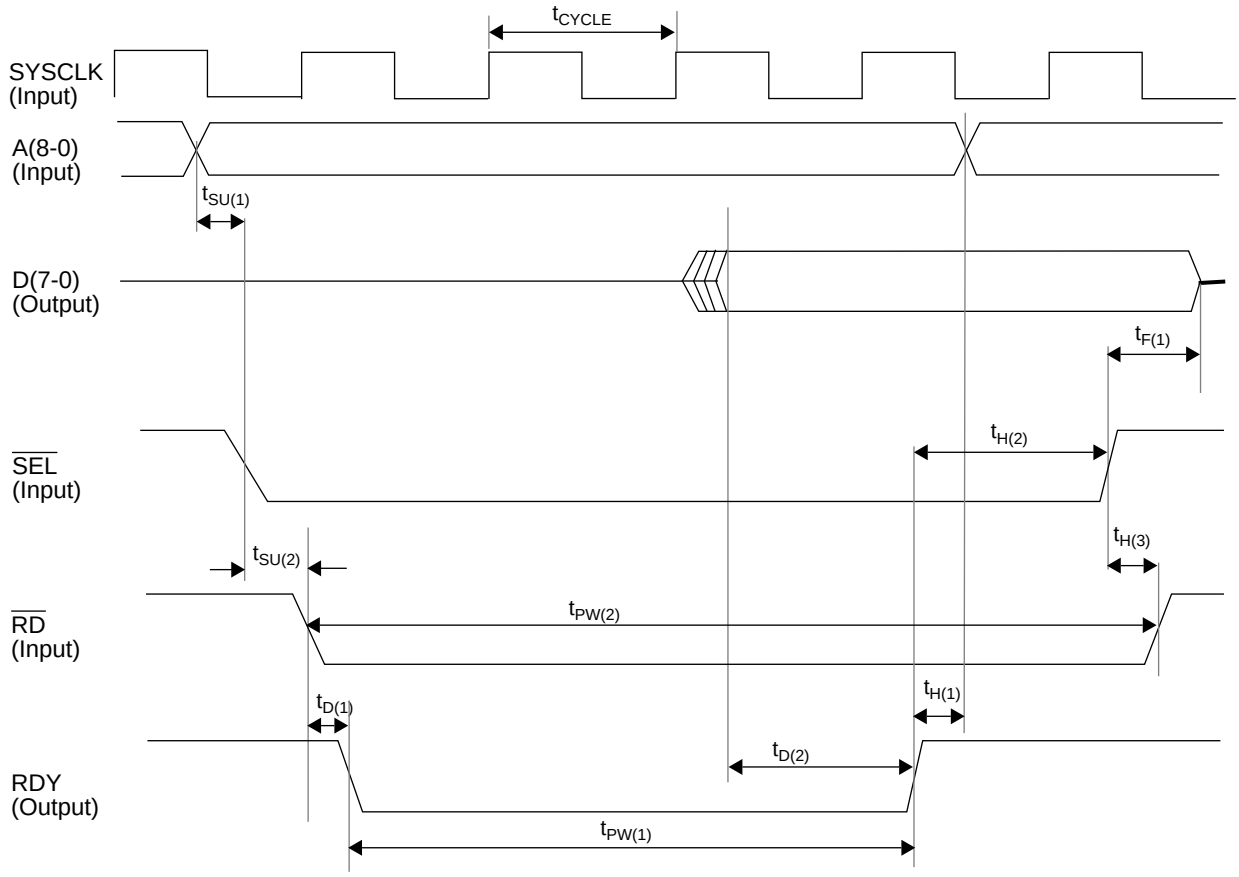
Figure 24. Serial Line Control Port Timing



Parameter	Symbol	Min	Typ	Max	Unit
LCK clock period	t_{CYC}	640 *			ns
LCK duty cycle, t_{PWH}/t_{CYC}		40		60	%
$\overline{\text{LENAn}}$ delay from to LCK↓	$t_{D(1)}$	10		14	ns
Delay from LCK↓ to LDO valid	$t_{D(2)}$	1		3	ns
LDI setup time to LCK↓	t_{SU}	10			ns
LDI hold time after LCK↓	$t_{H(2)}$	2			ns
$\overline{\text{LENAn}}$ hold time after 16th LCK↓	$t_{H(1)}$	2			ns

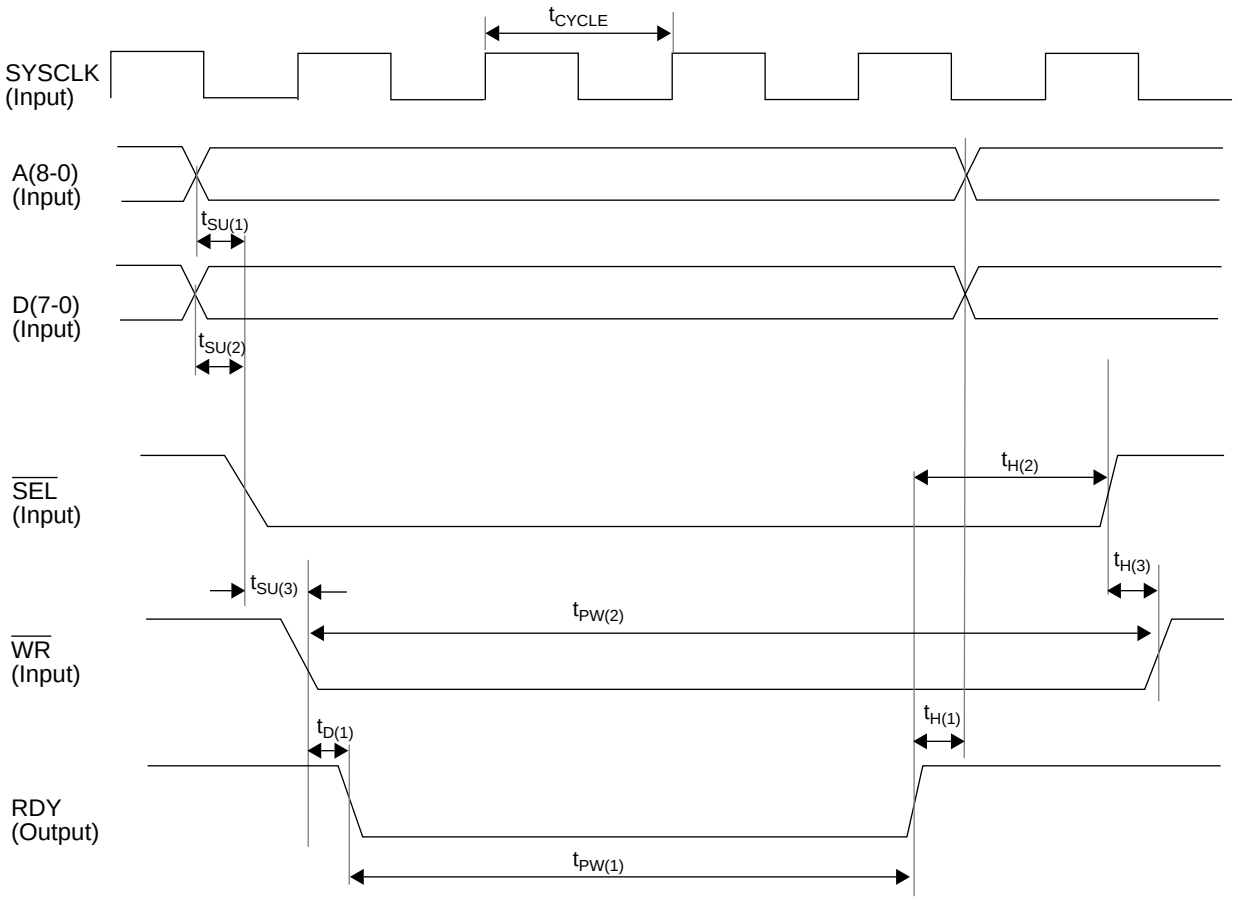
* LCK clock period is 16 times the clock period of SYSCLK, which is 40 nanoseconds minimum, corresponding to a maximum SYSCLK frequency of 25 MHz.

Figure 25. Microprocessor Read Timing, Intel Mode



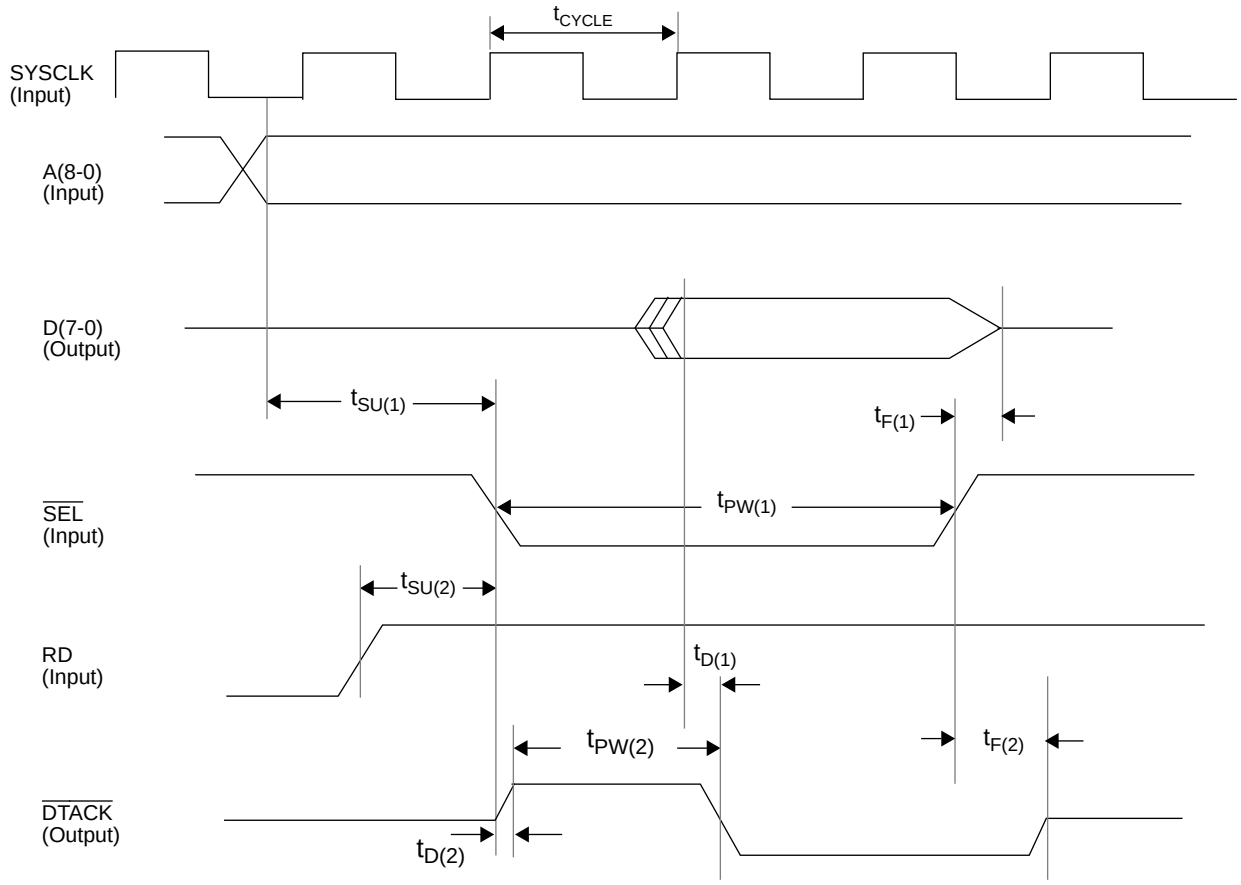
Parameter	Symbol	Min	Typ	Max	Unit
SYSCLK clock period	t_{CYCLE}	40			ns
A(8-0) set-up time to $\overline{SEL}\downarrow$	$t_{SU(1)}$	0			ns
$\overline{SEL}$ set-up time to $\overline{RD}\downarrow$	$t_{SU(2)}$	0			ns
RDY$\downarrow$ delay after $\overline{RD}\downarrow$	$t_{D(1)}$			5	ns
RDY$\uparrow$ delay after D(7-0) valid	$t_{D(2)}$	0			ns
RDY pulse width	$t_{PW(1)}$	0		25 * t_{CYCLE}	ns
$\overline{RD}$ pulse width	$t_{PW(2)}$	t_{CYCLE}			ns
A(8-0) hold time after RDY$\uparrow$	$t_{H(1)}$	0			ns
$\overline{SEL}$ hold time after RDY$\uparrow$	$t_{H(2)}$	0			ns
$\overline{RD}$ hold time after $\overline{SEL}\uparrow$	$t_{H(3)}$	0			ns
D(7-0) data float time after $\overline{SEL}\uparrow$	$t_{F(1)}$			16	ns

Figure 26. Microprocessor Write Timing, Intel Mode



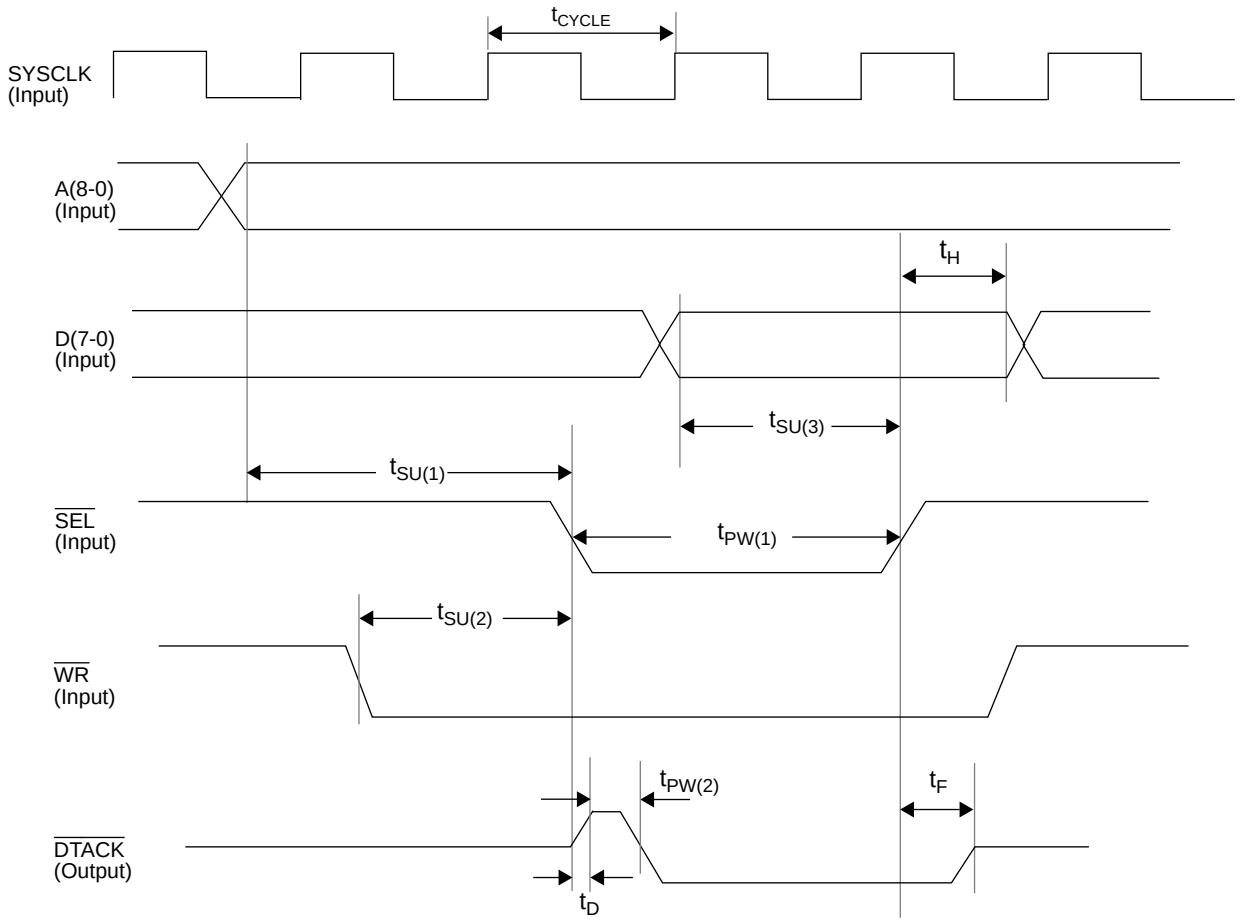
Parameter	Symbol	Min	Typ	Max	Unit
SYSCLK clock period	t_{CYCLE}	40			ns
A(8-0) address set-up time to $\overline{SEL}\downarrow$	$t_{SU(1)}$	0			ns
D(7-0) data set-up time to $\overline{SEL}\downarrow$	$t_{SU(2)}$	0			ns
$\overline{SEL}$ set-up time to $\overline{WR}\downarrow$	$t_{SU(3)}$	0			ns
RDY delay after $\overline{WR}\downarrow$	$t_{D(1)}$			5	ns
RDY pulse width	$t_{PW(1)}$	0		25 * t_{CYCLE}	ns
$\overline{WR}$ pulse width	$t_{PW(2)}$	t_{CYCLE}			
A(8-0) address & D(7-0) data hold after RDY$\uparrow$	$t_{H(1)}$	0			ns
$\overline{SEL}$ hold after RDY$\uparrow$	$t_{H(2)}$	0			ns
$\overline{WR}$ hold after $\overline{SEL}\uparrow$	$t_{H(3)}$	0			ns

Figure 27. Microprocessor Read Timing, Motorola Mode



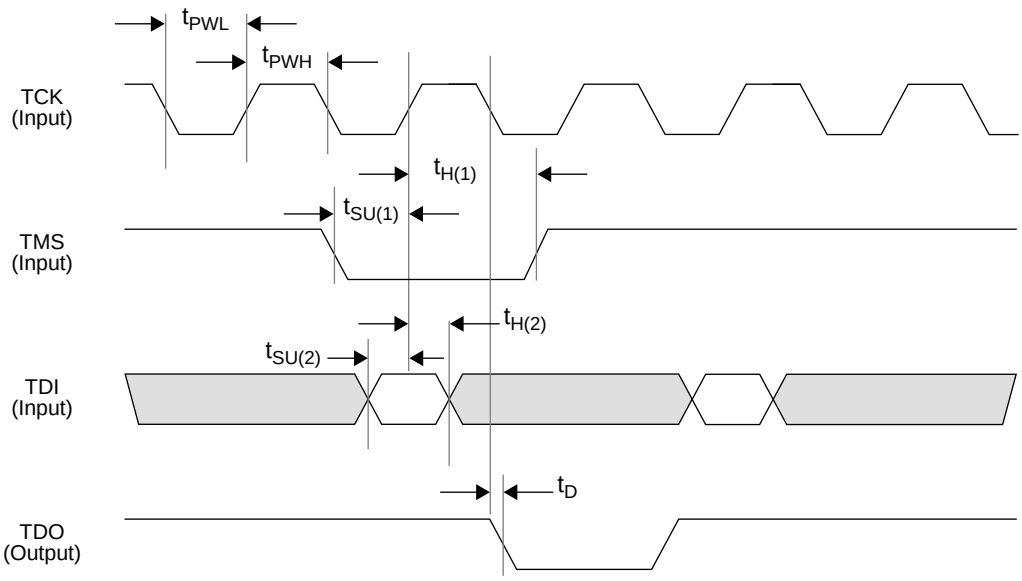
Parameter	Symbol	Min	Typ	Max	Unit
SYSCLK clock period	t_{CYCLE}	40			ns
A(8-0) address valid set-up time to $\overline{SEL}\downarrow$	$t_{SU(1)}$	0			ns
D(7-0) data output valid to $\overline{DTACK}\downarrow$	$t_{D(1)}$			4	ns
D(7-0) data float time after $\overline{SEL}\uparrow$	$t_{F(1)}$			5	ns
RD set-up time to $\overline{SEL}\downarrow$	$t_{SU(2)}$	5			ns
$\overline{SEL}$ pulse width	$t_{PW(1)}$	40			ns
$\overline{DTACK}$ pulse width	$t_{PW(2)}$			$3 * t_{CYCLE}$	ns
$\overline{DTACK}$ float time after $\overline{SEL}\uparrow$	$t_{F(2)}$			t_{CYCLE}	ns
$\overline{DTACK}$ delay after $\overline{SEL}\downarrow$	$t_{D(2)}$			t_{CYCLE}	ns

Figure 28. Microprocessor Write Timing, Motorola Mode



Parameter	Symbol	Min	Typ	Max	Unit
SYSCLK clock period	t_{CYCLE}	40			ns
A(8-0) address valid set-up time to $\overline{SEL}\downarrow$	$t_{SU(1)}$	0			ns
$\overline{WR}$ set-up time to $\overline{SEL}\downarrow$	$t_{SU(2)}$	5			ns
D(7-0) data valid set-up time before $\overline{SEL}\uparrow$	$t_{SU(3)}$	20			ns
D(7-0) data valid hold time after $\overline{SEL}\uparrow$	t_H	5			ns
$\overline{SEL}$ pulse width	$t_{PW(1)}$	40			ns
$\overline{DTACK}$ pulse width	$t_{PW(2)}$			t_{CYCLE}	ns
$\overline{DTACK}$ float time after $\overline{SEL}\uparrow$	t_F			t_{CYCLE}	ns
$\overline{DTACK}$ delay after $\overline{SEL}\downarrow$	t_D			t_{CYCLE}	ns

Figure 29. Boundary Scan Timing



Parameter	Symbol	Min	Max	Unit
TCK clock high time	t_{PWH}	50		ns
TCK clock low time	t_{PWL}	50		ns
TMS setup time before TCK↑	$t_{SU(1)}$	3.0		ns
TMS hold time after TCK↑	$t_{H(1)}$	2.0		ns
TDI setup time before TCK↑	$t_{SU(2)}$	3.0		ns
TDI hold time after TCK↑	$t_{H(2)}$	2.0		ns
TDO delay from TCK↓	t_D		7.0	ns

OPERATION

TEST ACCESS PORT

Introduction

The IEEE 1149.1 standard defines the requirements of a boundary scan architecture that has been specified by the IEEE Joint Test Action Group (JTAG). Boundary scan is a specialized scan architecture that provides observability and controllability for the interface pins of the device. As shown in Figure 30, one cell of a boundary scan register is assigned to each input or output pin to be observed or tested (bidirectional pins may have two cells). The boundary scan capability is based on a Test Access Port (TAP) controller, instruction and bypass registers, and a boundary scan register bordering the input and output pins. The boundary scan test bus interface consists of four input signals (Test Clock (TCK), Test Mode Select (TMS), Test Data Input (TDI) and Test Reset ($\overline{\text{TRS}}$)) and a Test Data Output (TDO) output signal.

The TAP controller receives external control information via a Test Clock (TCK) signal, a Test Mode Select (TMS) signal and a Test Port Reset ($\overline{\text{TRS}}$) signal, and it sends control signals to the internal scan paths. Detailed information on the operation of this state machine can be found in the IEEE 1149.1 standard. The serial scan path architecture consists of an instruction register, a boundary scan register and a bypass register. These three serial registers are connected in parallel between the Test Data Input (TDI) and Test Data Output (TDO) signals, as shown in Figure 30.

The boundary scan function can be reset and disabled by holding pin $\overline{\text{TRS}}$ low. When boundary scan testing is not being performed the boundary scan register is transparent, allowing the input and output signals to pass to and from the COBRA device's internal logic. During boundary scan testing, the boundary scan register may disable the normal flow of input and output signals to allow the device to be controlled and observed via scan operations. For applications that use an on-board microprocessor to operate the boundary scan function it should be noted that pin RDY/$\overline{\text{DTACK}}$ must be ignored during boundary scan tests.

Boundary Scan Operation

The maximum frequency the COBRA device will support for boundary scan is 10 MHz. The timing diagrams for the boundary scan interface leads are shown in Figure 29.

The instruction register contains three bits. The COBRA device performs the following three boundary scan test instructions:

The EXTEST test instruction (000) provides the ability to test the connectivity of the COBRA device to external circuitry.

The SAMPLE/PRELOAD test instruction (010) provides the ability to examine the boundary scan register contents without interfering with device operation.

The BYPASS test instruction (111) provides the ability to bypass the COBRA boundary scan and instruction registers.

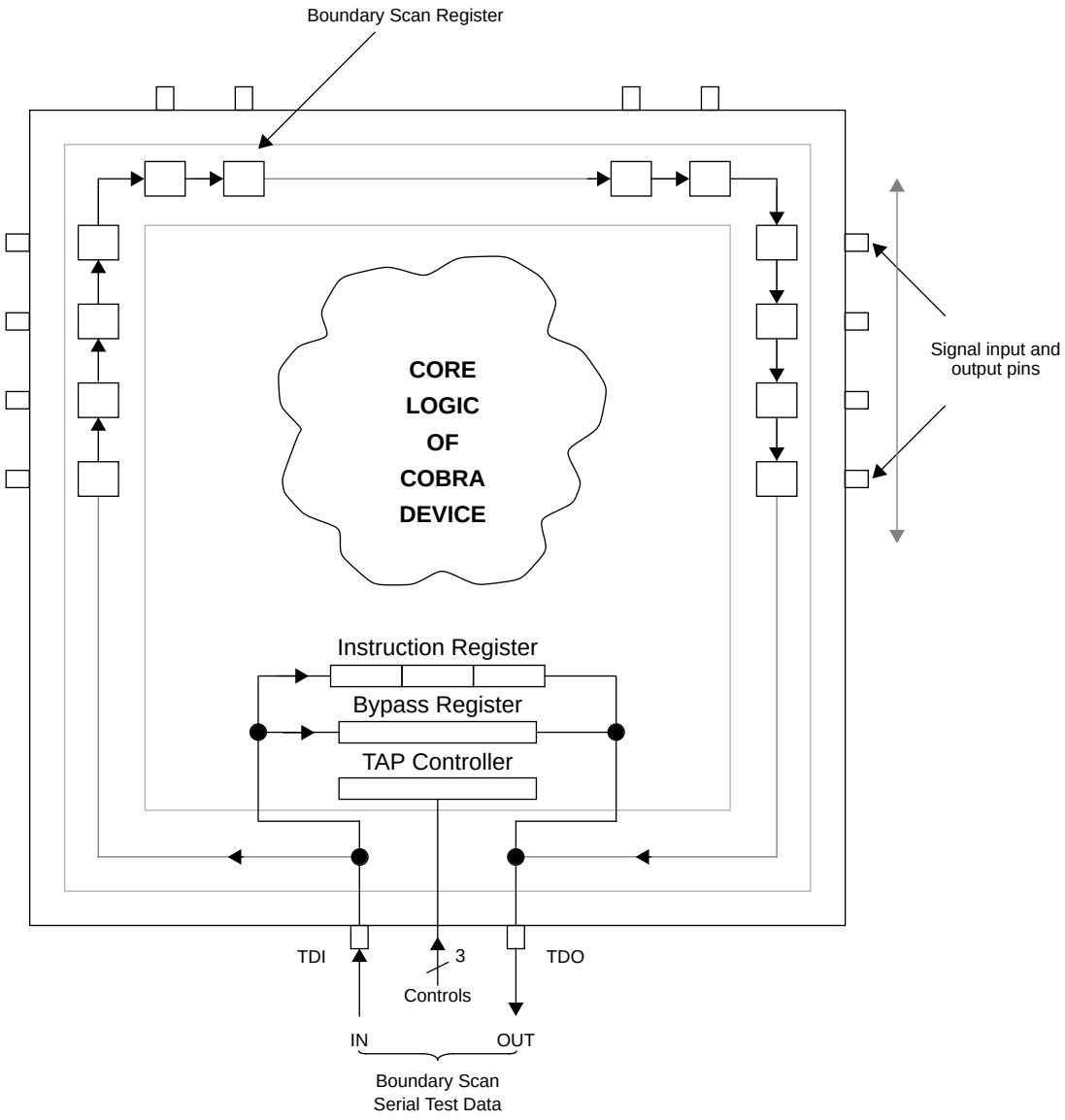
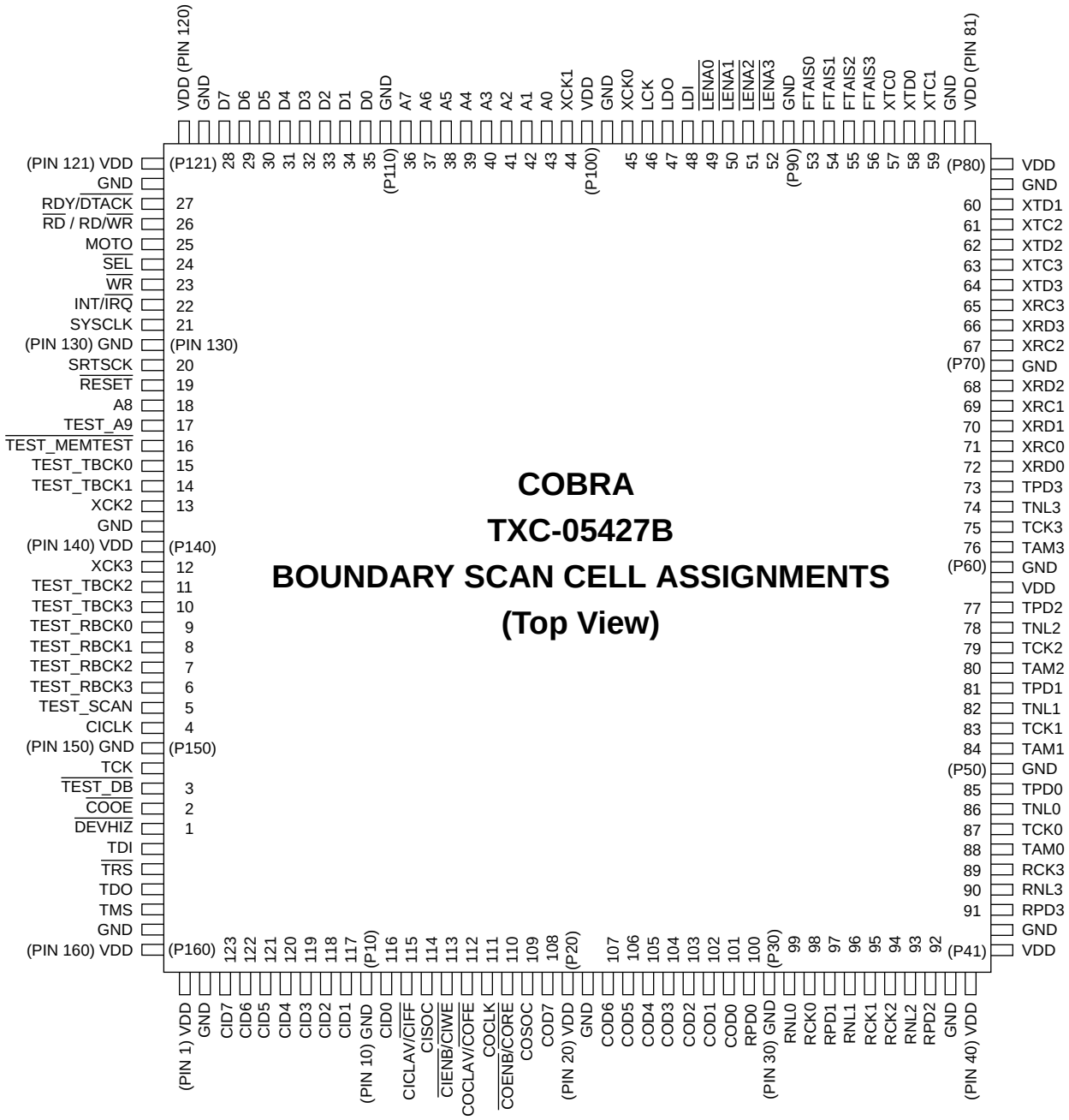


Figure 30. Boundary Scan Schematic

Boundary Scan Chain

Figure 31 illustrates the assignment of boundary scan cells to the signal input and output pins of the COBRA device. The plain numbers shown inside the device outline next to the signal-named pins are scan cell numbers. The numbers in parentheses, prefixed with "P", shown inside the device outline next to the signal-named pins are pin numbers.



Note: The plain numbers shown inside the device outline next to the signal-named pins are scan cell numbers.
The numbers in parentheses, prefixed with "P", shown inside the device outline next to the signal-named pins are pin numbers.

Figure 31. COBRA TXC-05427B Boundary Scan Cell Assignment to Pins

MEMORY MAP

OVERVIEW

Address Range (Hex)	Channel	Functions
000 - 0FF	Common	Device ID, reset, status; interrupt, configuration and serial port control
100 - 125	#0	Channel 0 status, control, performance monitoring, error counters
126 - 12F	All	Read and write pointers for Channels 0, 1, 2 and 3
130 - 15F	#1	Channel 1 status, control, performance monitoring, error counters
160 - 18F	#2	Channel 2 status, control, performance monitoring, error counters
190 - 1BF	#3	Channel 3 status, control, performance monitoring, error counters

COMMON MEMORY MAP

Address (Hex)	Mode*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
000	R	MID7 = 0	MID6 = 1	MID5 = 1	MID4 = 0	MID3 = 1	MID2 = 0	MID1 = 1	MID0 = 1
001	R	PN3 = 0	PN2 = 0	PN1 = 1	PN0 = 1	MID11 = 0	MID10 = 0	MID9 = 0	MID8 = 0
002	R	PN11 = 0	PN10 = 1	PN9 = 0	PN8 = 1	PN7 = 0	PN6 = 0	PN5 = 1	PN4 = 1
003	R	V3 = 0	V2 = 0	V1 = 0	V0 = 1	PN15 = 0	PN14 = 0	PN13 = 0	PN12 = 1
004	R	ML3 = 0	ML2 = 0	ML1 = 0	ML0 = 0	G3 = 0	G2 = 0	G1 = 0	G0 = 0
005		Reserved							
006		Reserved							
007	R/W	Reset7	Reset6	Reset5	Reset4	Reset3	Reset2	Reset1	Reset0
008	R	Reserved			CMS3	CMS2	CMS1	CMS0	GCMS
009	R(L)	Reserved					LCTOVF	LPNLOL	LHECERR
00A	R/W	Reserved					MCTOVF	MPNLOL	MHECERR
00B	R/W	Reserved						INTPOS	INTNEG
00C	R/W	MSEL2	MSEL1	MSEL0	TAGMODE	NNIMODE	PADBIS1	PRNS1	PRNS0
00D	R/W	TCAVTH2	TCAVTH1	TCAVTH0	NRT2	NRT1	NRT0	UTOPIA	HECENA
00E		Reserved							
00F		Reserved							
010	R/W	LRW	Reserved					LN1	LN0
011	R/W	LRA7	LRA6	LRA5	LRA4	LRA3	LRA2	LRA1	LRA0
012	R	LS7	LS6	LS5	LS4	LS3	LS2	LS1	LS0
013	R/W	LD7	LD6	LD5	LD4	LD3	LD2	LD1	LD0
014		Reserved							
015		Reserved							
016		Reserved							
017-0FF		Reserved							

* Modes: R - Read-Only, R(L) - Read-Only Latched Event Bit, R/W - Read or Write, R/WC - Read or Clear on Write cycle.
Note: "Reserved" bytes are not to be accessed. "Reserved" bits of R/W bytes are "Don't Care" but should be written to 0.

CHANNEL 0 MEMORY MAP

Address (Hex)	Mode*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
100	R	CSTRVA0	CFUF0	CCSCT0	CTLLOA0	CRLLOS0	CLOSP0	CLOCS0	CFOVF0
101	R(L)	LSTRVA0	LFUF0	LCSCT0	LTLLOA0	LRLLOS0	LLOSP0	LLOCS0	LFOVF0
102	R/W	MSTRVA0	MFUF0	MCSCT0	MTLLOA0	MRLLOS0	MLOSP0	MLOCS0	MFOVF0
103	R/W	SLOPE0	TLEN0	RLEN0	Reserved	TLCINV0	RLCINV0	LC01	LC00
104	R/W	RLPBK0	TLPBK0	Reserved	EXTSIG0	TLC01	TLC00	RLC01	RLC00
105	R/W	DIVRAT0	PFILL0	NFILLD05	NFILLD04	NFILLD03	NFILLD02	NFILLD01	NFILLD00
106	R/W	Reserved						NN09	NN08
107	R/W	NN07	NN06	NN05	NN04	NN03	NN02	NN01	NN00
108	R/W	SCCHK0	SRTS0	STRU0	CLK0	REFDIV03	REFDIV02	REFDIV01	REFDIV00
109	R/W	DELFR0	INSFR0	Reserved		KS03	KS02	KS01	KS00
10A	R/W	FIFLEN07	FIFLEN06	FIFLEN05	FIFLEN04	FIFLEN03	FIFLEN02	FIFLEN01	FIFLEN00
10B		Reserved							
10C	R/W	LTOFF0F	LTOFF0E	LTOFF0D	LTOFF0C	LTOFF0B	LTOFF0A	LTOFF09	LTOFF08
10D	R/W	LTOFF07	LTOFF06	LTOFF05	LTOFF04	LTOFF03	LTOFF02	LTOFF01	LTOFF00
10E		Reserved							
10F		Reserved							
110	R/W	RT077	RT076	RT075	RT074	RT073	RT072	RT071	RT070
111	R/W	RT067	RT066	RT065	RT064	RT063	RT062	RT061	RT060
112	R/W	RT057	RT056	RT055	RT054	RT053	RT052	RT051	RT050
113	R/W	RT047	RT046	RT045	RT044	RT043	RT042	RT041	RT040
114	R/W	RT037	RT036	RT035	RT034	RT033	RT032	RT031	RT030
115	R/W	RT027	RT026	RT025	RT024	RT023	RT022	RT021	RT020
116	R/W	RT017	RT016	RT015	RT014	RT013	RT012	RT011	RT010
117	R/W	GFC03	GFC02	GFC01	GFC00	VPI07	VPI06	VPI05	VPI04
118	R/W	VPI03	VPI02	VPI01	VPI00	VCI0F	VCI0E	VCI0D	VCI0C
119	R/W	VCI0B	VCI0A	VCI09	VCI08	VCI07	VCI06	VCI05	VCI04
11A	R/W	VCI03	VCI02	VCI01	VCI00	PTI02	PTI01	PTI00	CLP0
11B	R/WC	DCCTR07	DCCTR06	DCCTR05	DCCTR04	DCCTR03	DCCTR02	DCCTR01	DCCTR00
11C	R/WC	ICCTR07	ICCTR06	ICCTR05	ICCTR04	ICCTR03	ICCTR02	ICCTR01	ICCTR00
11D	R/WC	CV07	CV06	CV05	CV04	CV03	CV02	CV01	CV00
11E	R/WC	CV0F	CV0E	CV0D	CV0C	CV0B	CV0A	CV09	CV08
11F	R	Reserved							FRDONE0
120		Reserved							
121		Reserved							
122		Reserved							
123		Reserved							

Address (Hex)	Mode*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
124		Reserved							
125		Reserved							
126	R	RD07	RD06	RD05	RD04	RD03	RD02	RD01	RD00
127	R	WR05	WR04	WR03	WR02	WR01	WR00	RD09	RD08
128	R	RD13	RD12	RD11	RD10	WR09	WR08	WR07	WR06
129	R	WR11	WR10	RD19	RD18	RD17	RD16	RD15	RD14
12A	R	WR19	WR18	WR17	WR16	WR15	WR14	WR13	WR12
12B	R	RD27	RD26	RD25	RD24	RD23	RD22	RD21	RD20
12C	R	WR25	WR24	WR23	WR22	WR21	WR20	RD29	RD28
12D	R	RD33	RD32	RD31	RD30	WR29	WR28	WR27	WR26
12E	R	WR31	WR30	RD39	RD38	RD37	RD36	RD35	RD34
12F	R	WR39	WR38	WR37	WR36	WR35	WR34	WR33	WR32

* Modes: R - Read-Only, R(L) - Read-Only Latched Event Bit, R/W - Read or Write, R/WC - Read or Clear on Write cycle.
Note: "Reserved" bytes are not to be accessed. "Reserved" bits of R/W bytes are "Don't Care" but should be written to 0.

CHANNEL 1, 2, 3 MEMORY MAP

Address (Hex)	Mode*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
130-15F	Channel 1, See Channel 0 Register Map (add 030H to all addresses)								
160-18F	Channel 2, See Channel 0 Register Map (add 060H to all addresses)								
190-1BF	Channel 3, See Channel 0 Register Map (add 090H to all addresses)								

Note: Register locations with no entries are not implemented. The structure of the memory map is the same for each channel, except that Channel 0 uses the additional addresses 126H - 12FH for read and write pointers registers for all four channels and the corresponding registers for the other channels are Reserved. There is an address offset of 030H (48 decimal) bytes between adjacent per-channel register banks. Bit symbols contain the channel number digit (n=1, 2 or 3) instead of 0 as the first digit after the alphabetic characters.

MEMORY MAP DESCRIPTIONS

COMMON MEMORY MAP

Device Identification and Reset

Address*	Bit	Symbol	Description
000	7-0	MID7-MID0	**Manufacturer Identity:** Read-only register containing the least significant two nibbles (6B Hex) of the device manufacturer's identity. TranSwitch has been assigned the identity code 06B Hex or 107 Dec.
001	7-4	PN3-PN0	**Part Number:** Read-only register containing the least significant nibble (3 Hex) of the device part number 05427 (1533 Hex).
	3-0	MID11-MID8	**Manufacturer Identity:** Read-only register containing the most significant (third) nibble of the device manufacturer's identity (0 Hex).
002	7-0	PN11-PN4	**Part Number:** Read-only register containing the third and second nibbles of the device part number (53 Hex).
003	7-4	V3-V0	**Version:** Read-only register containing the device version number (1 Hex).
	3-0	PN15-PN12	**Part Number:** Read-only register containing the most significant (fourth) nibble of the device part number (1 Hex).
004	7-4	ML3-ML0	**Mask Level:** Read-only register containing the device mask level (0 Hex).
	3-0	G3-G0	**Growth:** Read-only register containing the device growth field (0 Hex).
007	7-0	Reset	**Software Reset:** Writing 91 Hex into this location will generate a software reset to the device. Writing other than 91 Hex to this location will remove COBRA from the reset state. Reading this location will return 00 Hex if COBRA is not in reset and 01 Hex if COBRA is in reset.

Status and Interrupt Control Bits

Address	Bit	Symbol	Description
008	7-5	Reserved	**Reserved:** Values read out are to be disregarded.
	4-1	CMS3-CMS0	**Change in State of Per Channel Latched Event Bits:** This bit (one per channel) is 1 when any of the corresponding per channel latched event bits (at addresses 191H, 161H, 131H and 101H, respectively) is 1.
	0	GCMS	**Change in State of Global Event Bits:** This bit is 1 when any of the three latched event bits common to all channels is 1. These global event bits are LCTOVF, LPNLOL and LHECERR in register 009H.

* Note: All Addresses are shown in hexadecimal notation

Address	Bit	Symbol	Description
009	7-3	Reserved	**Reserved:** Values read out are to be disregarded.
	2	LCTOVF	**Cell Transmit Overflow:** This latched bit is set to 1 when there is an INTPOS/INTNEG-enabled transition of the FIFO overflow indication for any of the channels on the transmit side. To return the device to correct operation, all channels must be reset by means of control bits RLENn. This bit is cleared on read.
	1	LPNLOL	**Pseudo Number Loss of Lock Error:** This latched bit is set to 1 when there is an INTPOS/INTNEG-enabled transition of the out of lock indication of the pseudo-random number analyzer. This bit is cleared on read.
	0	LHECERR	**HEC Error:** This latched bit is set to 1, if HEC checking is activated by control bit HECENA, when there is an INTPOS/INTNEG enabled transition of the HEC error indication. This bit is cleared on read.
00A	7-3	Reserved	**Reserved:** Set to 0.
	2	MCTOVF	**Cell Transmit Overflow Interrupt Mask:** When set to 1, the cell transmit overflow interrupt to the microprocessor is masked (i.e., no hardware interrupt is generated when the corresponding latched event bit is 1 in register 009H).
	1	MPNLOL	**Loss of Lock Interrupt Mask:** When set to 1, the pseudo-random number analyzer out of lock interrupt to the microprocessor is masked (i.e., no hardware interrupt is generated when the corresponding latched event bit is 1 in register 009H).
	0	MHECERR	**HEC Error Interrupt Mask:** When set to 1, the interrupt to the microprocessor due to HEC error is masked (i.e., no hardware interrupt is generated when the corresponding latched event bit is 1 in register 009H).
00B	7-2	Reserved	**Reserved:** Set to 0.
	1	INTPOS	**Interrupt on Start of Event:** If this bit is set to 1, it will cause the latched event bit to be set to 1, and a hardware interrupt to be generated if it is not masked, at the start of each event (i.e., at the positive, 0 to 1, transition of the current event indication). See Note 1.
	0	INTNEG	**Interrupt on End of Event:** If this bit is set to 1, it will cause the latched event bit to be set to 1, and a hardware interrupt to be generated if it is not masked, at the end of each event (i.e., at the negative, 1 to 0, transition of the current event indication). See Note 1.

Note 1: Latched event bits are not set, and interrupts are not generated, if INTPOS and INTNEG are both set to 0.

Device Configuration Register 1

<table>
<tr><th>Address</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td rowspan="5">00C</td><td>7-5</td><td>MSEL2-
MSEL0</td><td>Pseudo-Random Number Sequence Receiver Connection Select: These bits select the channel to connect to the pseudo-random number (PRN) sequence receiver. The coding is as follows:
<table>
<tr><th>MSEL2</th><th>MSEL1</th><th>MSEL0</th><th>PRN Sequence Receiver Connection</th></tr>
<tr><td>0</td><td>X</td><td>X</td><td>PRN sequence receiver unused</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Line received signal, channel 0</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Line received signal, channel 1</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Line received signal, channel 2</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Line received signal, channel 3</td></tr>
</table>
TLCn and RLCn bits must be set to appropriate values to use the PRN receiver when MSEL2 bit is set to 1. If the PRN receiver is activated, the line coding violation counter counts the received PRN sequence bit errors.</td></tr>
<tr><td>4</td><td>TAGMODE</td><td>TAG Mode: If this bit is set to 0 the routing tag bytes are prefixed to the 53 byte ATM cell. If it is set to 1, the routing tag bytes are appended to the 53 byte ATM cell.</td></tr>
<tr><td>3</td><td>NNIMODE</td><td>NNI Mode: If this bit is set to 0, UNI mode is selected. Only 8 bits of VPI are used. If this bit is set to 1, the GFC field is interpreted as VPI and 12 bits of VPI are used. This bit only affects the received ATM cell VPI/VCI channel matching. In the transmit direction, the 32-bit cell header stored in the control memory map is always used.</td></tr>
<tr><td>2</td><td>PADBIS1</td><td>Pad Bit is One: When PFILLn = 1, i.e., partial-fill mode is enabled for channel n, and this bit is set to 1, the padding bytes in a partially filled cell are set to all ones. If this bit is equal to 0, the padding bytes in a partially filled cell are set to all zeros.</td></tr>
<tr><td>1-0</td><td>PRNS1-
PRNS0</td><td>PRN Sequence Pattern Select: These bits select the pseudo-random number bit pattern. The coding is as follows:
<table>
<tr><th>PRNS1</th><th>PRNS0</th><th>Pattern</th></tr>
<tr><td>0</td><td>0</td><td>QRSS - (2^{20} - 1) with zero suppression</td></tr>
<tr><td>0</td><td>1</td><td>Reserved. Do not use.</td></tr>
<tr><td>1</td><td>0</td><td>2^{20} - 1</td></tr>
<tr><td>1</td><td>1</td><td>2^{15} - 1</td></tr>
</table></td></tr>
</table>

Device Configuration Register 2

Address	Bit	Symbol	Description
00D	7-5	TCAVTH2-TCAVTH0	**Transmit Cell Available Threshold:** These three bits define when the cell available signal is deasserted during the current cell period if a next cell is not available for transmit. TCAVTH0 is the LSB. The value of these bits must be 0 for UTOPIA compliance. For example, if TCAVTH is set to 100, the COCLAV/$\overline{\text{COFE}}$ pin is deasserted four clock cycles prior to the last byte of the cell.
	4-2	NRT2-NRT0	**Number of Routing Tag Bytes:** These three bits select the number of routing tag bytes to be prefixed or appended to a cell (as determined by TAGMODE). NRT0 is the LSB. A value of 0 indicates no routing tag (a 53 byte cell). Valid values are 0 through 7.
	1	UTOPIA	**UTOPIA Mode Select:** If this bit is set to 1, the cell interface is compliant with the ATM Forum UTOPIA Level 1 cell level flow control definition. If this bit is set to 0, the interface signals are similar to the signals for a synchronous FIFO.
	0	HECENA	**HEC Enable:** When set to 1, this bit enables checking of the ATM cell header HEC field on all four channels. When HECENA = 1, the cell is discarded on receiving a HEC error. If MHECERR is set to 0, an interrupt will be generated when LHECERR is 1.

Serial Port Control Registers

Address	Bit	Symbol	Description
010	7	LRW	**Line Control Read/Write:** Writing a 0 to this bit results in a read operation on the serial line control interface. Writing a 1 to this bit results in a write operation on the serial line control interface. The serial line control pins are activated whenever LRW is written to.
	6-2	Reserved	**Reserved:** Set to 0.
	1-0	LN1-LN0	**Line Number:** These bits select the line/channel interface number to which the read/write operations are to occur. LN0 is the LSB.
011	7-0	LRA7-LRA0	**Line Register Address:** These bits provide the register address in the line interface device selected by LN1-LN0. LRA0 is the LSB.
012	7-0	LS7-LS0	**Line Scan:** After a read operation from the line interface device, these bits provide the data read from the serial line interface device selected by LN1-LN0. LS0 is the LSB.
013	7-0	LD7-LD0	**Line Data:** These bits provide the data that will be written to the line interface device selected by LN1-LN0. LD0 is the LSB.

PER CHANNEL REGISTERS

The following entries show the per channel memory map registers. Entry addresses and symbols are shown for channel number n=0. The corresponding registers for channels n = 1, 2 and 3 start at addresses 1X0, where X = 3n, as described above for the memory map.

Address	Bit	Symbol	Description
Interrupt Current Status Register			
100	7	CSTRVA0	**Starvation Alarm:** This bit is set to 1 if a starvation condition exists in the receive side payload FIFO. Starvation condition is defined as no cell received for 2040 line clock cycles (255 bytes) after the payload FIFO becomes empty. An interrupt generated due to this alarm must be cleared by resetting that channel using the TLENn control bit.
	6	CFUF0	**FIFO Underflow:** This bit is set to 1 if the receive side payload FIFO becomes empty. This bit resets to 0 when the FIFO underflow condition is exited due to the arrival of cells.
	5	CCSCT0	**Sequence Check Change of State:** This bit is set to 1 if the sequence check mechanism enters the detection state from correction state. This bit resets to 0 when the sequence check mechanism enters the correction state.
	4	CTLLOA0	**Transmit Line Loss of Activity:** This bit is set to 1 if a high is detected on the TAM0 input pin. This bit resets to 0 when a low is detected on pin TAM0.
	3	CRLLOS0	**Receive Line Loss of Signal:** In the Unstructured service mode, if a loss of signal is detected, this bit is set to 1. This bit resets to 0 when loss of signal condition is exited.
	2	CLOSP0	**Loss of Structure Pointer:** If loss of synchronization of received cell structure pointer is detected by the structure pointer tracking state machine, this bit is set to 1. This bit resets to 0 when pointer synchronization is restored.
	1	CLOCS0	**Loss of Cell Sequence:** If SCCHK0 = 0 (low latency mode), and if 3 out of 8 consecutive cells arrive out of order, Loss-of-Cell sequence state is entered and this bit is set to 1. To exit the Loss-of-Cell sequence state and reset this bit to 0, 8 consecutive cells must be received in correct sequence. If SCCHK0 = 1 (ETSI mode), this bit is set to 1 when Loss-of-Cell sequence state is entered as defined in the ETSI standards. To exit the Loss-of-Cell sequence state and reset this bit to 0, 2 consecutive cells must be received in the correct sequence.
	0	CFOVF0	**FIFO Overflow:** This bit is set to 1 when an overflow condition is detected by the receive side payload FIFO. To resume normal operation the channel must be reset when a FIFO overflow condition is detected.

Address	Bit	Symbol	Description
Interrupt Latched Event Register			
101	7	LSTRVA0	Latched Value of CSTRVA0. This bit is cleared on read. See Note 1.
	6	LFUF0	Latched Value of CFUF0. This bit is cleared on read. See Note 1.
	5	LCSCT0	Latched Value of CCSCT0. This bit is cleared on read. See Note 1.
	4	LTLLOA0	Latched Value of CTLLOA0. This bit is cleared on read. See Note 1.
	3	LRLLOS0	Latched Value of CRLLOS0. This bit is cleared on read. See Note 1.
	2	LLOSP0	Latched Value of CLOSP0. This bit is cleared on read. See Note 1.
	1	LLOCS0	Latched Value of CLOCS0. This bit is cleared on read. See Note 1.
	0	LFOVF0	Latched Value of CFOVF0. This bit is cleared on read. See Note 1.

Note 1: Latching to 1 occurs on the positive and/or negative transition of the corresponding current status indication in register 100H, as selected by control bits INTPOS and INTNEG.

Address	Bit	Symbol	Description
Interrupt Mask Register			
102	7	MSTRVA0	**Starvation Alarm Interrupt Mask:** When this bit is set to 1, the alarm is masked and there is no interrupt when LSTRVA0 occurs.
	6	MFUF0	**FIFO Underflow Interrupt Mask:** When this bit is set to 1, the alarm is masked and there is no interrupt when LFUF0 occurs.
	5	MCSCT0	**Sequence Check Change of State Interrupt Mask:** When this bit is set to 1, the alarm is masked and there is no interrupt when LCSCT0 occurs.
	4	MTLLOA0	**Transmit Line Loss of Activity Interrupt Mask:** When this bit is set to 1, the alarm is masked and there is no interrupt when LTLLOA0 occurs.
	3	MRLLOS0	**Receive Line Loss of Signal Interrupt Mask:** When this bit is set to 1, the alarm is masked and there is no interrupt when LRLLOS0 occurs.
	2	MLOSP0	**Loss of Structure Pointer Interrupt Mask:** When this bit is set to 1, the alarm is masked and there is no interrupt when LLOSP0 occurs.
	1	MLOCS0	**Loss of Cell Sequence Interrupt Mask:** When this bit is set to 1, the alarm is masked and there is no interrupt when LLOCS0 occurs.
	0	MFOVF0	**FIFO Overflow Interrupt Mask:** When this bit is set to 1, the alarm is masked and there is no interrupt when LLFOVF0 occurs.

<table>
<tr><th>Address</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td colspan="4">Configuration Registers</td></tr>
<tr><td rowspan="8">103</td><td>7</td><td>SLOPE0</td><td>Slope of SRTS Values Positive: The setting options for this control bit will be inserted after clock recovery tests have been completed. Default setting of this bit must be 0.</td></tr>
<tr><td>6</td><td>TLEN0</td><td>Line Transmit Enable: This bit must be set to 1 to enable data transmission to the line and processing of cells received for this channel. If 0 is written to this control bit, AAL1 reassembly state machines are reset and cells received on this channel are discarded. To enable AAL1 reassembly operation, 1 must be written to this control bit.</td></tr>
<tr><td>5</td><td>RLEN0</td><td>Line Receive Enable: This bit must be set to 1 to enable processing of the line input data. If 0 is written to this control bit, the AAL1 segmentation state machines are reset and cells are not segmented for this channel. To enable AAL1 segmentation operation, 1 must be written to this control bit.</td></tr>
<tr><td>4</td><td>Reserved</td><td>Reserved: Set to 0.</td></tr>
<tr><td>3</td><td>TLCINV0</td><td>Invert Transmit Line Clock: When set to 1, the rising edge of the line transmit clock TCK0 is the active edge. When set to 0, the falling edge of the clock is the active edge. Serial line data is shifted out of the line output block on the active edge of the clock.</td></tr>
<tr><td>2</td><td>RLCINV0</td><td>Invert Receive Line Clock: When set to 1, the rising edge of the line receive clock RCK0 is the active edge. When set to 0, the falling edge of the clock is the active edge. Serial line input data is sampled on the active edge of the clock.</td></tr>
<tr><td>1-0</td><td>LC01-LC00</td><td>Line Coding: These bits define the line coding in the Unstructured service mode (STRU0 = 0). If STRU0 = 1, NRZ mode is used and the coding of these bits is ignored. If STRU0 = 0, the following line coding is used.
<table>
<tr><th>LC01</th><th>LC00</th><th>Line Coding</th></tr>
<tr><td>0</td><td>0</td><td>NRZ; line coder/decoder bypass</td></tr>
<tr><td>0</td><td>1</td><td>HDB3 (E1 operation)</td></tr>
<tr><td>1</td><td>0</td><td>AMI (T1 operation)</td></tr>
<tr><td>1</td><td>1</td><td>B8ZS (T1 operation)</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Address</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td rowspan="5">104</td><td>7</td><td>RLPBK0</td><td>Received Cell Loopback: If this bit is set to 1, cells received for this channel from the cell input interface are looped back to the cell output interface. The AAL1 reassembly process is not performed. Only one channel can be configured to be in cell receive loopback mode at any given time.</td></tr>
<tr><td>6</td><td>TLPBK0</td><td>Transmit Cell Loopback: If this bit is set to 1, cells generated by COBRA for this channel are looped back from the cell output block to the cell input block. Only one channel can be configured to be in transmit cell loopback mode at any given time.</td></tr>
<tr><td>5</td><td>Reserved</td><td>Reserved: Set to 0.</td></tr>
<tr><td>4</td><td>EXTSIG0</td><td>External Signal: When set to 1, XTC0/XRC0 and XTD0/XRD0 are selected for line interface transmit/receive clock and data respectively. AAL1 processing is not performed.</td></tr>
<tr><td>3-2</td><td>TLC01-
TLC00</td><td>Line Transmit Signal: These two bits select the signal to be sent as output from the Line Output block.
<table>
<tr><th>TLC01</th><th>TLC00</th><th>Signal Select</th></tr>
<tr><td>0</td><td>0</td><td>Clock recovery loop output (normal operation).</td></tr>
<tr><td>0</td><td>1</td><td>Test signal defined by pseudo-random number generator control bits PRNS1 and PRNS0.</td></tr>
<tr><td>1</td><td>0</td><td>All ones AIS signal.</td></tr>
<tr><td>1</td><td>1</td><td>Loopback received line signal
(line receive to line transmit loopback).</td></tr>
</table></td></tr>
<tr><td>1-0</td><td>RLC01-
RLC00</td><td>Line Receive Signal: These two bits select the signal from the Line Input block to be used for segmentation (cell assembly).
<table>
<tr><th>RLC01</th><th>RLC00</th><th>Signal Select</th></tr>
<tr><td>0</td><td>0</td><td>Received line signal (normal operation).</td></tr>
<tr><td>0</td><td>1</td><td>Reserved. Do not use.</td></tr>
<tr><td>1</td><td>0</td><td>All ones AIS signal.</td></tr>
<tr><td>1</td><td>1</td><td>Loopback transmitted line signal
(line transmit to line receive loopback)</td></tr>
</table></td></tr>
</table>

Address	Bit	Symbol	Description
105	7	DIVRAT0	**Divide Ratio:** When set to 0, XCKn must be 31.5 times the nominal frequency of the line clock to be recovered. For T1/E1 line rate, this bit should be set to 0. When set to 1, XCKn must be 9.5 times the nominal frequency of the line clock to be recovered. This is used for higher line rates.
	6	PFILL0	**Partial Fill:** This bit must be set to 1 for partially-filled cells. In this case, NFILLD05-NFILLD00 defines the number of user bytes in a cell. The rest are filled with dummy (padded) bytes.
	5-0	NFILLD05-NFILLD00	**Partial Fill Size:** These six bits define the number of user bytes in a partially-filled cell. NFILLD00 is the LSB. For example, a NFILLD0 value of 01H (1 decimal) means 2 user bytes per cell and a value of 2EH (46 decimal) means 47 user bytes per cell. For Unstructured service (STRU0=0), values of 09H through 2EH (9 through 46 decimal) are valid. For Structured service (STRU0=1), values of 09H through 2DH (9 through 45 decimal) are valid. All other values are invalid.
106	7-2	Reserved	**Reserved:** Set to 0.
	1-0	NN09-NN08	**Structure Size:** These are the two most significant bits of the number NN0 (NN09-NN00) used to define the size of a structure in channel 0.
107	7-0	NN07-NN00	**Structure Size:** These bits are the eight least significant bits used to define the size of a structure. NN0 + 1 is the size of the structure. For example, if NN0 is set to 017H (23 decimal), the structure size is 24. The maximum value of this 10-bit field is 92 decimal, i.e., a structure size of 93 decimal.
108	7	SCCHK0	**Sequence Count Check Mode Select:** ETSI mode: If this bit is set to 1, the cell sequence number tracking state machine takes a decision based on the analysis of two consecutive cells. The ETSI mode conforms to the ETSI standards AAL1 requirements. Low latency mode: If this bit is set to 0, the cell sequence number tracking state machine decision is based on the currently received cell.
	6	SRTS0	**Enable SRTS:** When set to 1, the SRTS mechanism is enabled for line clock recovery. When control bits KS03-KS00 are set to 0, the SRTS mechanism is disabled.
	5	STRU0	**Structured Service:** When this bit is set to 1, Structured service mode is enabled and NN09-NN00 will define the size of structure used. When this bit is set to 1, line coding control bits (LC01-LC00) are ignored and NRZ mode is assumed. A start of structure pulse will be generated on line transmit pin TNL0. The line input start of structure indicator is provided on input pin RNL0. When this bit is set to 0, Unstructured service mode is enabled.
	4	CLK0	**Clock Mode:** If set to 1, line clock recovery is not used and TCK0 is an input. If set to 0, line clock is recovered using SRTS and/or Adaptive FIFO algorithm; TCK0 is an output in this mode. For Structured service, if CLK0 is set to 1, TNL0 is a frame input. When CLK0 is set to 0, TNL0 is a frame output.

Address	Bit	Symbol	Description
108	3-0	REFDIV03-REFDIV00	**Reference Clock Divide:** The SRTSCK frequency is divided by 2 to the power of the value contained in these four bits (REFDIV00 is the LSB) and the derived clock is used as the reference clock for the SRTS time stamp generation and the SRTS clock recovery algorithm. For example, if REFDIV03-00 is set at 3, the reference clock (network clock) frequency is SRTSCK divided by 8. Valid values for REFDIV03-00 are 0 to 8. For DS1/E1 operation, if SRTSCK is set at 2.43 MHz, REFDIV0 must be set to 0. In general, the setting of REFDIVn must satisfy the following equation: $f_{RCKn} < (f_{SRTSCK} / 2^{REFDIVn}) < (2 \times f_{RCKn})$
109	7	DELFR0	**Delete Frame:** This bit is used only in Structured service mode. When this bit is set from 0 to 1, one structure NN0 (one frame) worth of payload will be deleted from the receive side payload FIFO. When a structure is deleted, FRDONE0 is set to 1 by the COBRA. The application software must not initiate another structure deletion or insertion until FRDONE0 is set to 1. DELFR0 must be set to 0 to reset FRDONE0 to 0. After FRDONE0 is reset to 0, another structure deletion action can be initiated by setting the DELFR0 bit to 1.
	6	INSFR0	**Insert Frame:** This bit is used only in Structured service mode. When this bit is set from 0 to 1, one structure NN0 (one frame) worth of payload will be inserted into the receive side payload FIFO. The value of the payload inserted is random. When a structure is inserted, FRDONE0 is set to 1 by the COBRA. The application software must not initiate another structure insertion or deletion until FRDONE0 is set to 1. INSFR0 must be set to 0 to reset FRDONE0 to 0. After FRDONE0 is reset to 0, another structure insertion action can be initiated by setting the INSFR0 bit to 1.
	5-4	Reserved	**Reserved:** Set to 0.
	3-0	KS03-KS00	**SRTS Loop Gain Factor:** These bits define the gain constant for the SRTS clock recovery loop. In normal operation, these bits should be set to 1H to enable the SRTS clock recovery engine. KS00 is the LSB.
10A	7-0	FIFLEN07-FIFLEN00	**Half Length of FIFO:** These bits define *half* the length of the receive side payload FIFO in terms of cells used for clock recovery. These bits must be set based on maximum cell delay variation and delay tolerance. The total payload FIFO length per channel is 16 cells (i.e., 16 x 47 = 752 bytes). In non-partial fill mode, the max. value for FIFLEN0 is 8. FIFLEN00 is the LSB.
10C	7-0	LTOFF0F-LTOFF08	**Long Term Offset:** These 16 bits are used to adjust the long term variation in frequency due to cell delay variation and/or when the adaptive clock recovery mechanism is used. In normal operation, these bits should be set to 0000H (LTOFF00 is the LSB)**.** The value of LTOFF0F-LTOFF00 will be latched by the clock recovery loop when address 10C is written.
10D	7-0	LTOFF07-LTOFF00	
110-116	7-0	RT037-RT030 to RT007-RT000	**Routing Tag:** These seven bytes are the locations provided for routing tag bytes that are prefixed (TAGMODE = 0) or appended (TAGMODE = 1) to a transmitted ATM cell. The number of bytes to be prefixed or appended (0-7) is programmed via the common memory control bits NRT2-NRT0. If NRT2-NRT0 is set to 5, the five routing tag bytes are attached to the cell in the order of RT057-RT050, RT047-RT040, ... , RT017-RT010.

Address	Bit	Symbol	Description
117	7-4	GFC03-GFC00	**GFC or VPI:** These bits constitute the most significant nibble of the ATM cell header. When NNIMODE=0, these bits are treated as GFC bits. When NNMODE=1, these bits are used as the most significant bits of the VPI field.
	3-0	VPI07-VPI04	**VPI:** This byte provides the VPI field for the ATM cell header when NNI-MODE = 0. This byte provides the least significant eight bits of VPI when NNIMODE=1. VPI00 is the LSB.
118	7-4	VPI03-VPI00	
	3-0	VCI0F-VCI0C	**VCI:** These two bytes are the 16-bit VCI field for the ATM cell header. VCI00 is the LSB.
119	7-0	VCI0B-VCI04	
11A	7-4	VCI03-VCI00	
	3-1	PTI02-PTI00	**PTI**: These three bits define the transmitted PTI field for the ATM cell header.
	0	CLP0	**CLP**: This bit defines the transmitted CLP bit for the ATM cell header.
11B	7-0	DCCTR07-DCCTR00	**Discarded Cell Count:** This 8-bit non-saturating counter counts the number of cells discarded due to uncorrectable AAL1 header errors. The counter is cleared after a microprocessor write operation on this address. DCCTR00 is the LSB.
11C	7-0	ICCTR07-ICCTR00	**Inserted Dummy Cell Count:** This 8-bit non-saturating counter counts the number of dummy cells inserted due to cell loss. The counter is cleared after a microprocessor write operation on this address. ICCTR00 is the LSB.
11D	7-0	CV07-CV00	**Coding Violation Count:** This 16-bit non-saturating counter counts the number of coding violations detected at the line input. If the pseudo-random number analyzer is connected to the received line input (based on MSEL2-0), then this counter does not count the coding violations. The value of the counter is latched on reading address 11D (Hex). To prevent reading incorrect count, the read sequence should start from address 11D followed by 11E. The counter is cleared on a write operation to address 11D or 11E. CV00 is the LSB.
11E	7-0	CV0F-CV08	
11F	7-1	Reserved	**Reserved:** Values read out are to be disregarded.
	0	FRDONE0	**Frame Slip Done:** This bit is set to 1 by COBRA to indicate that a frame deletion or insertion, initiated via bits DELFR0 or INSFR0, has been completed. This bit will reset to 0 after DELFR0 or INSFR0 has been reset to 0 by the application software.
126	7-0	RD07-RD00	**Read Pointer for Channel 0, Bits 7-0:** Lower 8 bits of 10-bit read pointer for Channel 0.
127	7-2	WR05-WR00	**Write Pointer for Channel 0, Bits 5-0:** Lower 6 bits of 10-bit write pointer for Channel 0.
	1-0	RD09-RD08	**Read Pointer for Channel 0, Bits 9-8:** Upper 2 bits of 10-bit read pointer for Channel 0.
128	7-4	RD13-RD10	**Read Pointer for Channel 1, Bits 3-0:** Lower 4 bits of 10-bit read pointer for Channel 1.
	3-0	WR09-WR06	**Write Pointer for Channel 0, Bits 9-6:** Upper 4 bits of 10-bit write pointer for Channel 0.

Address	Bit	Symbol	Description
129	7-6	WR11-WR10	**Write Pointer for Channel 1, Bits 1-0:** Lower 2 bits of 10-bit write pointer for Channel 1.
	5-0	RD19-RD14	**Read Pointer for Channel 1, Bits 9-4:** Upper 6 bits of 10-bit read pointer for Channel 1.
12A	7-0	WR19-WR12	**Write Pointer for Channel 1, Bits 9-2:** Upper 8 bits of 10-bit write pointer for Channel 1.
12B	7-0	RD27-RD20	**Read Pointer for Channel 2, Bits 7-0:** Lower 8 bits of 10-bit read pointer for Channel 2.
12C	7-2	WR25-WR20	**Write Pointer for Channel 2, Bits 5-0:** Lower 6 bits of 10-bit write pointer for Channel 2.
	1-0	RD29-RD28	**Read Pointer for Channel 2, Bits 9-8:** Upper 2 bits of 10-bit read pointer for Channel 2.
12D	7-4	RD33-RD30	**Read Pointer for Channel 3, Bits 3-0:** Lower 4 bits of 10-bit read pointer for Channel 3.
	3-0	WR29-WR26	**Write Pointer for Channel 2, Bits 9-6:** Upper 4 bits of 10-bit write pointer for Channel 2.
12E	7-6	WR31-WR30	**Write Pointer for Channel 3, Bits 1-0:** Lower 2 bits of 10-bit write pointer for Channel 3.
	5-0	RD39-RD34	**Read Pointer for Channel 3, Bits 9-4:** Upper 6 bits of 10-bit read pointer for Channel 3.
12F	7-0	WR39-WR32	**Write Pointer for Channel 3, Bits 9-2:** Upper 8 bits of 10-bit write pointer for Channel 3.

PACKAGE INFORMATION

The COBRA device is packaged in a 160-pin plastic quad flat package suitable for socket or surface mounting, as shown in Figure 32.

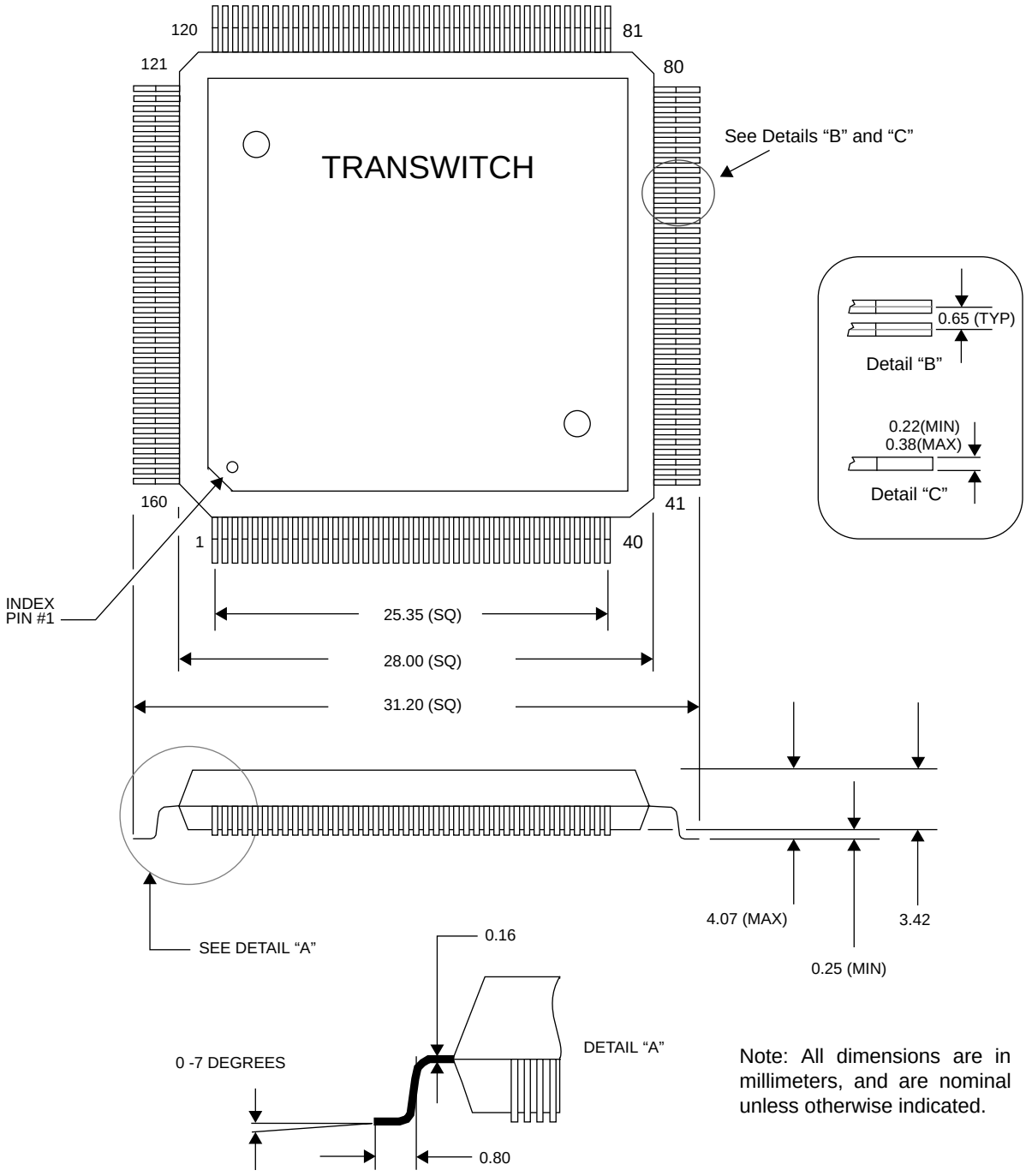


Figure 32. COBRA TXC-05427B 160-Pin Plastic Quad Flat Package

ORDERING INFORMATION

Part Number: TXC-05427-BIPQ 160-Pin Plastic Quad Flat Package

RELATED PRODUCTS

TXC-03102, QDS1F VLSI Device (Multichannel DS1 Framer). Provides D4SF, ESF (including FDL support) and transparent framing for four DS1 signals.

TXC-03104, QE1F VLSI Device (Multichannel E1 Framer). Provides standard and frame hold-off frame alignment, with optional CRC-4 multiframe check and selectable out of frame criteria, and transparent non-framing mode, for four E1 signals.

TXC-05501, SARA-S VLSI Device (ATM/SMDS Segmentation Controller). Simultaneously segments up to 8000 packets into ATM/SMDS cells using AAL3/4/5.

TXC-05601, SARA-R VLSI Device (ATM/SMDS Reassembly Controller). Simultaneously reassembles ATM/SMDS cells back into up to 8000 packets using AAL3/4/5.

TXC-05150, CDB VLSI Device (ATM Cell Delineation Block). Provides cell delineation and line rate adaptation for several line interfaces (1.544 Mbit/s to 155 Mbit/s).

TXC-05801, CUBIT VLSI Device. A *CellBus*-based ATM cell switching device.

TXC-06125, XBERT VLSI Device (Bit Error Rate Generator / Receiver). Programmable multi-rate test pattern generator and receiver in a single chip with serial, nibble, or byte interface capability.

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.):

American National Standards Institute (ANSI)
11 West 42nd Street
New York, New York 10036

Tel: 212-642-4900
Fax: 212-302-1286

The ATM Forum (U.S.A.):

ATM Forum World Headquarters
303 Vintage Park Drive
Foster City, CA 94404-1138

Tel: 415-578-6860
Fax: 415-525-0182

ATM Forum European Office
14 Place Marie - Jeanne Bassot
Levallois Perret Cedex
92593 Paris France

Tel: 33 1 46 39 56 26
Fax: 33 1 46 39 56 99

Bellcore (U.S.A.):

Bellcore
Attention - Customer Service
8 Corporate Place
Piscataway, NJ 08854

Tel: 800-521-CORE (In U.S.A.)
Tel: 908-699-5800
Fax: 908-336-2559

ETSI (Europe):

European Telecommunications Standards Institute
ETSI, 06921 Sophia - Antipolis
Cedex France

Tel: 33 92 94 42 00
Fax: 33 93 65 47 16

ITU-T (International):

Publication Services of International Telecommunication Union (ITU)
Telecommunication Standardization Sector (T)
Place des Nations
CH 1211
Geneve 20, Switzerland

Tel: 41-22-730-5285
Fax: 41-22-730-5991

TTC (Japan):

TTC Standard Publishing Group of the
Telecommunications Technology Committee
2nd Floor, Hamamatsucho - Suzuki Building,
1 2-11, Hamamatsu-cho, Minato-ku, Tokyo

Tel: 81-3-3432-1551
Fax: 81-3-3432-1553

LIST OF DATA SHEET CHANGES

This change list identifies those areas within this updated CUBIT Data Sheet that have technical differences relative to the previous and now superseded CUBIT Data Sheet:

Updated COBRA Data Sheet: Edition 2, August 1996

Superseded COBRA Data Sheet: Edition 1, April 1996

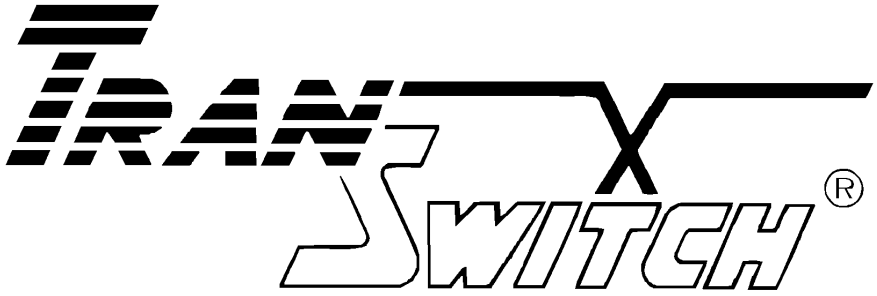
The page numbers indicated below of this updated data sheet include changes relative to the superseded data sheet.

Page Number of Updated Data Sheet	Summary of the Change
All	Changed edition number and date.
1	Added item 18 to Feature List.
2-3	Updated Table of Contents and List of Figures.
4	Made changes to the second paragraph.
6	Made changes to the second paragraph under Structured Service section.
10	Made changes to the first and second paragraphs.
14	Made changes to the paragraph under Cell Input Interface section.
19	Added description to Adaptive Clock Recovery section.
28	Made changes to the second paragraph and modified Figure 13.
33	Made changes to Name/Function column for CICLK and COCLK.
37	Made changes to Name/Function column for SYSCLK.
41	Deleted continuous power dissipation at 85 ^{o}C with 0 ft/min linear airflow row from the first table. Changed the row order of the last table.
44, 46	Changed Min column for Symbols $t_{H(1)}$, $t_{H(2)}$ and $t_{H(3)}$.
48-50	Changed Min column for Symbol t_{H}.
51	Modified Figure 24. Made changes to Parameter column for Symbol $t_{D(1)}$ and added last row to the table.
52-55	Made changes to waveform diagram and the corresponding table. Deleted the note.
60	Made changes to second row and added the third row to the first table.
61	Made changes to Addresses 10E, 10F, 11D and 11E.

Page Number of Updated Data Sheet	Summary of the Change
62	Made changes to Addresses 126 through 12F. Modified the note for the second table.
66, 67	Made changes to Description column for Bit 7 of Address 010 (LRW) and Bit 7 of Address 100 (CSTRVA0).
72	Made changes to Description column for Bits 7 and 6 of Address 109. Deleted Addresses 10B, 10E and 10F.
73	Made changes to Description column for Addresses 11D and 11E, Bit 0 of Address 11F.
73-74	Added Addresses 126 through 12F.
78-79	Updated List of Data Sheet Changes.

- NOTES -

- NOTES -



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