DATA SHEET

SAA6752HS
MPEG-2 video and MPEG-audio/AC-3 audio encoder with multiplexer

Product specification

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Philips Semiconductors

PHILIPS

CONTENTS

MPEG-2 video and MPEG-audio/AC-3 audio encoder with multiplexer

SAA6752HS

1 FEATURES

1.1 Video input and preprocessing

- Digital YUV input according to *"ITU-R BT.656"* (8 bits at 27 MHz) and *"ITU-R BT.601"*
- Support of enhanced *"ITU-R BT.656"* input format containing decoded VBI data readable via I^{2}C-bus; Closed Caption (CC), Wide Screen Signalling (WSS) and copyright information with Copy Generation Management System (CGMS)
- Processing of non-broadcast video signals from analog VCR according to IEC 756
- Two video clock input pins for switching two digital video sources
- *"ITU-R BT.601"* format conversion to 1/2D1, 2/3D1 and Standard Interchange Format (SIF)
- 4 : 2 : 2 to 4 : 2 : 0 colour format conversion
- Decimation filtering for all format conversions
- Adaptive median filter and motion compensated filter for input noise reduction.

1.2 Video compression

- Real-time MPEG-2 encoding compliant to Main Profile at Main Level (MP@ML) for 625 and 525 interlaced line systems
- Supported resolutions: D1, 2/3D1, 1/2D1 and SIF
- IPB frame, IP frame and I frame only encoding supported at all modes
- Supported bit rates: up to 25 Mbit/s I-only encoding; up to 15 Mbit/s IP-only or IBP encoding.
- Variable video bit rate mode for constant picture quality and constant bit rate mode to gain optimum picture quality from a fixed channel transfer rate
- Access to bit rate control parameters whilst encoding to support external real-time control algorithms (e.g. constrained variable bit rate control)
- Programmable Group Of Pictures (GOP) structure
- Innovative motion estimation with wide search range
- Adaptive quantization
- Motion compensated noise filter.

1.3 Audio input

- Audio inputs: I^{2}S format or EIAJ format (16, 18 or 20 bits), master or slave mode at 32, 44.1 and 48 kHz
- Two digital I^{2}S input ports for selection between two digital audio sources
- Audio clock generation: 256f_s or 384f_s (where f_s = 48 kHz) locked to video frame rate (if video is present)
- Sample rate conversion to 48 kHz (locked to video frame rate) for slave mode operation in all modes except Digital Versatile Disc (DVD) compliant bypass.

1.4 Audio compression

- Dolby®(1) Digital Consumer Encoding (DDCE) also known as AC-3(2) 2 channel audio encoding at 256 kbit/s or 384 kbit/s (SAA6752HS/101 only)
- MPEG-1 layer 2 audio encoding at 256 kbit/s or 384 kbit/s
- Input data bypass for Linear Pulse Code Modulation (LPCM) and compressed audio data [MPEG-1, MPEG-2, Dolby® Digital (DD) and Digital Theatre System (DTS)] according to IEC 61937
- Preamble Pc, Preamble Pd and bit stream information captured for identification of modes during bypass of compressed audio data for MPEG-1, MPEG-2, DD and DTS according to IEC 61937
- Audio mute via I^{2}C-bus control for all modes except DVD-compliant bypass.

1.5 Stream multiplexer

- Multiplexing of video and audio streams according to the MPEG-2 systems standard (*"ISO 13818-1"*)
- Generation and output of MPEG-2 Transport Streams (TS), MPEG-2 Program Streams (PS), Packetized Elementary Streams (PES) and Elementary Streams (ES) compliant to the DVD, D-VHS and DVB standards
- MPEG time stamp (PTS/DTS/SCR/PCR) generation and insertion (synchronization)
- Insertion of metadata
- Optional generation of empty time slots for subsequent insertion of application specific data packets
- Optional insertion of user data in the GOP header and in the picture header.

(1) Dolby is a registered trademark of Dolby Laboratories Licensing Corporation.

(2) AC-3 is a registered trademark of Dolby Laboratories Licensing Corporation.

1.6 Output interface

- Parallel interface 8-bit master/slave output
- 3-state output port
- Glueless interfacing with IEEE 1394 chip sets (for example, PDI 1394 L11)
- Data Expansion Bus Interface (DEBI) interface.

1.7 Control domain

- All control done via I^2C-bus
- I^2C-bus slave transceiver up to 400 kbit/s
- I^2C-bus slave address select pin
- Host interrupt flag pin.

1.8 Other features

- Single external clock or single crystal 27 MHz
- Separate 27 MHz system clock output
- Interface voltage 3.3 V
- TTL compatible digital outputs
- Power supply voltage 3.3 and 2.5 V
- Boundary Scan Test (BST) supported
- Power-down mode
- Single SDRAM system memory (16 Mbit@16 bit or 64 Mbit@16 bit).

2 GENERAL DESCRIPTION

2.1 General

Philips Semiconductors' second generation real time MPEG-2 encoder, the SAA6752HS, is a highly integrated single-chip audio and video encoding solution with flexible multiplexing functionality. With our expertise in two critical areas for consumer video encoding, noise filtering and motion estimation, we have pushed the boundaries for video quality even further, providing enhanced quality for low bit rates and enabling increased recording times for a given storage capacity. The SAA6752HS will also enable a key driver for new consumer digital recording applications and system cost reduction. By integrating all audio encoding and multiplexing functionality we will be moving from a three chip to a one chip system, with cost efficient design and process technology, thus providing a truly low cost, high quality encoding system.

The SAA6752HS/102 is intended for customers whose application does not require the DDCE function.

The SAA6752HS gives significant advantages to customers developing digital recording applications:

- **Fast time-to-market and low development resources.** By adding a simple external video input processor IC, an audio analog-to-digital converter, and an external SDRAM, analog video and audio sources are compressed into high quality MPEG-2 video and MPEG-1 layer 2 or AC-3 audio streams, multiplexed into a single program or transport stream for simple connection to various storage media or broadcast media. Hence, making design effort for our customers a minimum, as well as removing the need for in-depth experience in MPEG encoding.
- **Low system host resources.** All video and audio encoding algorithms and software are run on an internal MIPS®(1) processor. The SAA6752HS only requires a small amount of communication from the system host processor to set up and control required encoding parameters via the I^2C-bus.

2.2 Application fields

2.2.1 DVD BASED OPTICAL DISC RECORDERS (DVD+RW, DVD-RW, DVD-RAM)

Emerging optical disc based recording systems target to replace the existing consumer recording (VCR) and playback (DVD and VCD) products. The first generation recordable DVD based products will want to maximise recording times for the 4.7 Gbyte storage capacity. For these systems the SAA6752HS is critical, with its superior noise filtering and motion estimation, in enabling high quality at low bit rates.

Playback compatibility with existing DVD decoding solutions will also be important, which is why the SAA6752HS provides Dolby® digital consumer (AC-3) audio encoding to allow playback through existing players implementing DDCE (AC-3) decoding dominant in current DVD platforms.

The DVD stream is based on MPEG Program Stream (PS). The SAA6752HS directly outputs MPEG PS compliant to the DVD standard.

(1) MIPS is a registered trademark of MIPS Technologies.

2.2.2 HDD BASED TIME SHIFT RECORDING

Hard Disc Drive (HDD) based time-shift systems enable Personalized TV (PTV) functionality, providing consumers with new powers of control over what and when to watch broadcast content. With the audio and video content recorded digitally, identification, search and retrieval becomes a 'no brainer' task as compared to traditional VCR functionality. Combine this with electronic program guides and intelligent control, and the PTV can also analyse the viewers watching habits to search for programs likely to be of interest and automatically recorded in anticipation of the viewers preferences.

Since HDD recorders are closed systems, the recording format stream can be proprietary. The SAA6752HS flexible multiplexing formats support a number of recording stream formats for HDD including MPEG Transport Stream (TS) or MPEG Packetized Elementary Stream (PES).

2.2.3 DIGITAL VCR (DVHS) RECORDING

A DVHS player records streams based on MPEG Transport Streams (TS) packed in logical tape tracks. The SAA6752HS output streams are compliant with DVHS standard requirements.

2.2.4 VIDEO EDITING/TRANSMISSION/SURVEILLANCE/ CONFERENCING

The SAA6752HS can operate as a stand-alone device in all the above applications. The SAA6752HS full features and flexibility allows customers to tailor functionality and performance to specific application requirements. All required control settings such as GOP size and bit rate modes can be selected via the I^2C-bus.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDP}	digital supply voltage (pad cells)	3.0	3.3	3.6	V
V_{DDCO}	digital supply voltage (core)	2.3	2.5	2.7	V
V_{DDA}	analog supply voltage (oscillator and PLL)	2.3	2.5	2.7	V
$I_{DD(tot)}$	total analog plus digital supply current	407	453	525	mA
P_{tot}	total power dissipation	0.95	1.16	1.48	W
f_{DCXO}	quartz frequency (digital controlled tuning)	$27 \times [1 - (200 \times 10^{-6})]$	27	$27 \times [1 + (200 \times 10^{-6})]$	MHz
f_{SDRAM}	SDRAM clock frequency	–	108	–	MHz
f_{SCL}	I^2C-bus input clock frequency	100	–	400	kHz
B	output bit-rate	1.5	–	25	Mbit/s
V_{IH}	HIGH-level digital input voltage	1.7	–	3.6	V
V_{IL}	LOW-level digital input voltage	–0.5	–	+0.7	V
V_{OH}	HIGH-level digital output voltage	$V_{DDP} - 0.4$	–	V_{DDP}	V
V_{OL}	LOW-level digital output voltage	0	–	0.4	V
T_{amb}	ambient temperature	0	–	70	°C

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA6752HS/101[1]	SQFP208	plastic shrink quad flat package; 208 leads (lead length 1.3 mm); body $28 \times 28 \times 3.4$ mm; high stand-off height	SOT316-1
SAA6752HS/102[2]			

Notes

1. MPEG-2 video and MPEG-audio/AC-3 audio encoder with multiplexer.
2. MPEG-2 video and MPEG-audio encoder with multiplexer, but without AC-3 audio encoder.

5 BLOCK DIAGRAM

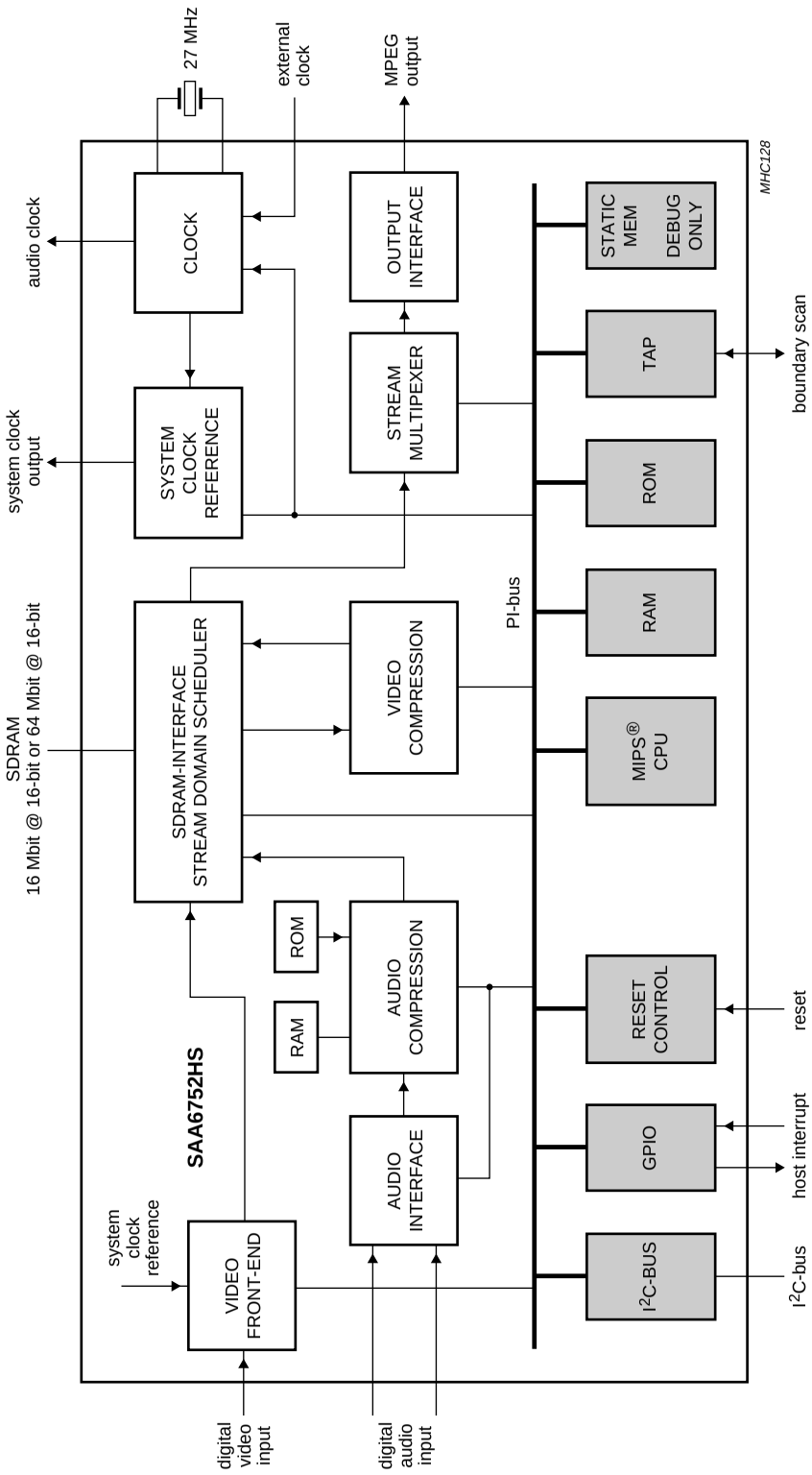


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	INPUT/OUTPUT[1]	I_{max} (mA)	DESCRIPTION
V_{SSP}	1	ground	–	pad ground
SDATA1	2	input	–	I^2S-bus serial data input port 1 with internal pull-down resistor
SCLK1	3	input/output	4	I^2S-bus serial clock port 1 with internal pull-down resistor
SWS1	4	input/output	4	I^2S-bus word select port 1 with internal pull-down resistor
V_{DDP}	5	supply	–	pad ring supply voltage (3.3 V)
SDATA2	6	input/output	4	I^2S-bus serial data port 2 with internal pull-down resistor
SCLK2	7	input/output	4	I^2S-bus serial clock port 2 with internal pull-down resistor
SWS2	8	input/output	4	I^2S-bus word select port 2 with internal pull-down resistor
ACLK	9	output	4	audio clock output ($256f_s$ or $384f_s$)
V_{SSP}	10	ground	–	pad ground
IDQ	11	input	–	reserved input with internal pull-down resistor; (recommended to connect to pin V_{SSP})
YUV0	12	input	–	video input signal bit 0 (LSB)
YUV1	13	input	–	video input signal bit 1
YUV2	14	input	–	video input signal bit 2
YUV3	15	input	–	video input signal bit 3
YUV4	16	input	–	video input signal bit 4
YUV5	17	input	–	video input signal bit 5
YUV6	18	input	–	video input signal bit 6
YUV7	19	input	–	video input signal bit 7 (MSB)
V_{SSP}	20	ground	–	pad ground
HSYNC	21	input	–	horizontal sync input (video) with internal pull-down resistor
VSYNC	22	input	–	vertical sync input (video) with internal pull-down resistor
FID	23	input	–	video field identification input (odd/even field) with internal pull-down resistor
VCLK1	24	input	–	video clock input 1 (27 MHz) with internal pull-down resistor
V_{SSCO}	25	ground	–	core ground
V_{SSCO}	26	ground	–	core ground
V_{DDCO}	27	supply	–	core supply voltage (2.5 V)
V_{DDCO}	28	supply	–	core supply voltage (2.5 V)
V_{DDP}	29	supply	–	pad ring supply voltage (3.3 V)
VCLK2	30	input	–	video clock input 2 (27 MHz) with internal pull-down resistor
PDOAV	31	3-state output	4	parallel stream data output for audio/video identifier
PDIDS	32	input	–	parallel stream data input for data strobe [request for packet in Data Expansion Bus Interface (DEBI) slave mode] with internal pull-up resistor
PDOSYNC	33	3-state output	4	parallel stream data output for packet sync
V_{SSP}	34	ground	–	pad ground
PDOVAL	35	3-state output	4	parallel stream data valid output with internal pull-up resistor
PDO0	36	3-state output	4	parallel stream data output bit 0 (LSB)

SYMBOL	PIN	INPUT/OUTPUT[1]	I_{max} (mA)	DESCRIPTION
PDO1	37	3-state output	4	parallel stream data output bit 1
PDO2	38	3-state output	4	parallel stream data output bit 2
V_{DDP}	39	supply	–	pad ring supply voltage (3.3 V)
PDO3	40	3-state output	4	parallel stream data output bit 3
PDO4	41	3-state output	4	parallel stream data output bit 4
PDO5	42	3-state output	4	parallel stream data output bit 5
PDO6	43	3-state output	4	parallel stream data output bit 6
V_{SSP}	44	ground	–	pad ground
PDO7	45	3-state output	4	parallel stream data output bit 7 (MSB)
PDIOCLK	46	input/output	4	parallel stream clock input/output
I2CADDRSEL	47	input	–	I^2C-bus address select input with internal pull-up resistor
SD_DQ15	48	input/output	8	SDRAM data input/output bit 15 (MSB)
V_{DDP}	49	supply	–	pad ring supply voltage (3.3 V)
SD_DQ0	50	input/output	8	SDRAM data input/output bit 0 (LSB)
SD_DQ14	51	input/output	8	SDRAM data input/output bit 14
SD_DQ1	52	input/output	8	SDRAM data input/output bit 1
V_{SSP}	53	ground	–	pad ground
SD_DQ13	54	input/output	8	SDRAM data input/output bit 13
SD_DQ2	55	input/output	8	SDRAM data input/output bit 2
SD_DQ12	56	input/output	8	SDRAM data input/output bit 12
V_{DDP}	57	supply	–	pad ring supply voltage (3.3 V)
SD_DQ3	58	input/output	8	SDRAM data input/output bit 3
SD_DQ11	59	input/output	8	SDRAM data input/output bit 11
SD_DQ4	60	input/output	8	SDRAM data input/output bit 4
SD_DQ10	61	input/output	8	SDRAM data input/output bit 10
V_{SSP}	62	ground	–	pad ground
SD_DQ5	63	input/output	8	SDRAM data input/output bit 5
SD_DQ9	64	input/output	8	SDRAM data input/output bit 9
SD_DQ6	65	input/output	8	SDRAM data input/output bit 6
SD_DQ8	66	input/output	8	SDRAM data input/output bit 8
V_{DDP}	67	supply	–	pad ring supply voltage (3.3 V)
SD_DQ7	68	input/output	8	SDRAM data input/output bit 7
SD_DQM1	69	output	8	SDRAM data mask enable output bit 1
SD_DQM0	70	output	8	SDRAM data mask enable output bit 0 (LSB)
$\overline{SD\_WE}$	71	output	8	SDRAM write enable output (active LOW)
V_{SSP}	72	ground	–	pad ground
$\overline{SD\_CAS}$	73	output	8	SDRAM column address strobe output (active LOW)
SD_CLK	74	output	8	SDRAM clock output
$\overline{SD\_RAS}$	75	output	8	SDRAM row address strobe output (active LOW)
SD_CKE	76	output	8	SDRAM clock enable output

SYMBOL	PIN	INPUT/OUTPUT[1]	I_{max} (mA)	DESCRIPTION
V_{SSCO}	77	ground	–	core ground
V_{SSCO}	78	ground	–	core and substrate ground
V_{DDCO}	79	supply	–	core supply voltage (2.5 V)
V_{DDCO}	80	supply	–	core supply voltage (2.5 V)
V_{DDP}	81	supply	–	pad ring supply voltage (3.3 V)
$\overline{SD\_CS}$	82	output	8	SDRAM chip select output (active LOW)
SD_A13	83	output	8	SDRAM address output bit 13 (bank selection for 64 Mbit)
SD_A9	84	output	8	SDRAM address output bit 9
SD_A8	85	output	8	SDRAM address output bit 8
V_{SSP}	86	ground	–	pad ground
SD_A11	87	output	8	SDRAM address output bit 11 (bank selection for 16 Mbit)
SD_A7	88	output	8	SDRAM address output bit 7
SD_A12	89	output	8	SDRAM address output bit 12 (bank selection for 64 Mbit)
SD_A6	90	output	8	SDRAM address output bit 6
V_{DDP}	91	supply	–	pad ring supply voltage (3.3 V)
SD_A10	92	output	8	SDRAM address output bit 10
SD_A5	93	output	8	SDRAM address output bit 5
SD_A0	94	output	8	SDRAM address output bit 0 (LSB)
SD_A4	95	output	8	SDRAM address output bit 4
V_{SSP}	96	ground	–	pad ground
SD_A1	97	output	8	SDRAM address output bit 1
SD_A3	98	output	8	SDRAM address output bit 3
SD_A2	99	output	8	SDRAM address output bit 2
SD_DQM3	100	output	8	reserved (do not connect)
V_{DDP}	101	supply	–	pad ring supply voltage (3.3 V)
SD_DQM2	102	output	8	reserved (do not connect)
SD_DQ31	103	input/output	8	reserved (do not connect)
SD_DQ16	104	input/output	8	reserved (do not connect)
V_{SSP}	105	ground	–	pad ground
SD_DQ30	106	input/output	8	reserved (do not connect)
SD_DQ17	107	input/output	8	reserved (do not connect)
SD_DQ29	108	input/output	8	reserved (do not connect)
V_{DDP}	109	supply	–	pad ring supply voltage (3.3 V)
SD_DQ18	110	input/output	8	reserved (do not connect)
SD_DQ28	111	input/output	8	reserved (do not connect)
SD_DQ19	112	input/output	8	reserved (do not connect)
SD_DQ27	113	input/output	8	reserved (do not connect)
V_{SSP}	114	ground	–	pad ground
SD_DQ20	115	input/output	8	reserved (do not connect)
SD_DQ26	116	input/output	8	reserved (do not connect)

SYMBOL	PIN	INPUT/OUTPUT(1)	I_{max} (mA)	DESCRIPTION
SD_DQ21	117	input/output	8	reserved (do not connect)
SD_DQ25	118	input/output	8	reserved (do not connect)
V_{DDP}	119	supply	–	pad ring supply voltage (3.3 V)
SD_DQ22	120	input/output	8	reserved (do not connect)
SD_DQ24	121	input/output	8	reserved (do not connect)
SD_DQ23	122	input/output	8	reserved (do not connect)
EXTCLK	123	input	–	27 MHz external clock input with internal pull-up resistor
V_{SSP}	124	ground	–	pad ground
V_{SSA}	125	ground	–	oscillator analog ground
XTALI	126	analog input	–	crystal oscillator input (27 MHz); note 2
XTALO	127	analog output	–	crystal oscillator output (27 MHz)
V_{DDA}	128	supply	–	oscillator analog supply voltage (2.5 V)
V_{SSCO}	129	ground	–	core ground
V_{SSCO}	130	ground	–	core ground
V_{DDCO}	131	supply	–	core supply voltage (2.5 V)
V_{DDCO}	132	supply	–	core supply voltage (2.5 V)
V_{DDP}	133	supply	–	pad ring supply voltage (3.3 V)
TDI	134	input	–	boundary scan test data input; pin must float or set to HIGH during normal operating; with internal pull-up resistor; note 3
TMS	135	input	–	boundary scan test mode select; pin must float or set to HIGH during normal operating; with internal pull-up resistor; note 3
TCK	136	input	–	boundary scan test clock; pin must be set to LOW during normal operating; with internal pull-up resistor; note 3
TDO	137	3-state output	4	boundary scan test data output; pin not active during normal operating; with 3-state output; note 3
V_{SSP}	138	ground	–	pad ground
$\overline{TRST}$	139	input	–	test reset input (active LOW), for boundary scan test (with internal pull-up resistor); notes 3 and 4
CLKOUT	140	output	4	27 MHz system clock output
TEST0	141	input/output	4	reserved (do not connect)
TEST1	142	input/output	4	reserved (do not connect)
V_{DDP}	143	supply	–	pad ring supply voltage (3.3 V)
TEST2	144	input/output	4	reserved (do not connect)
SDA	145	input/open-drain output	–	I^2C-bus serial data input/output
SCL	146	input/open-drain output	–	I^2C-bus serial clock input/output
$\overline{RESET}$	147	input	–	reset input (active LOW); with internal pull-up resistor
V_{SSP}	148	ground	–	pad ground
$\overline{RTS}$	149	output	4	reserved (do not connect); Universal Asynchronous Receiver/Transmitter (UART) request to send output (active LOW)

SYMBOL	PIN	INPUT/OUTPUT(1)	I_{max} (mA)	DESCRIPTION
$\overline{CTS}$	150	input	–	reserved (recommended connect to pin V_{DDP}); UART clear to send input; external static memory select input (active LOW); with internal pull-up resistor
RXD	151	input	–	reserved (recommended connect to pin V_{DDP}); UART receive data; internal boot select input; with internal pull-up resistor
TXD	152	output	4	reserved (do not connect); UART transmit data
V_{DDP}	153	supply	–	pad ring supply voltage (3.3 V)
$\overline{SM\_LB}$	154	input/output	4	reserved (do not connect)
$\overline{SM\_UB}$	155	input/output	4	reserved (do not connect)
H_IRF	156	3-state output	4	host interrupt flag output; with internal pull-up resistor
V_{SSP}	157	ground	–	pad ground
$\overline{SM\_OE}$	158	output	4	reserved (do not connect); static memory output enable output (active LOW)
SM_A9	159	output	4	reserved (do not connect); static memory address output bit 9
SM_A10	160	output	4	reserved (do not connect); static memory address output bit 10
V_{DDP}	161	supply	–	pad ring supply voltage (3.3 V)
SM_A8	162	output	4	reserved (do not connect); static memory address output bit 8
SM_A11	163	output	4	reserved (do not connect); static memory address output bit 11
SM_A7	164	output	4	reserved (do not connect); static memory address output bit 7
SM_A12	165	output	4	reserved (do not connect); static memory address output bit 12
V_{SSP}	166	ground	–	pad ground
SM_A6	167	output	4	reserved (do not connect); static memory address output bit 6
SM_A13	168	output	4	reserved (do not connect); static memory address output bit 13
SM_A5	169	output	4	reserved (do not connect); static memory address output bit 5
SM_A14	170	output	4	reserved (do not connect); static memory address output bit 14
V_{DDP}	171	supply	–	pad ring supply voltage (3.3 V)
$\overline{SM\_WE}$	172	output	4	reserved (do not connect); static memory write enable output (active LOW)
SM_D7	173	input/output	4	reserved (do not connect); static memory data input/output bit 7 with internal pull-down resistor
SM_D8	174	input/output	4	reserved (do not connect); static memory data input/output bit 8 with internal pull-down resistor
SM_D6	175	input/output	4	reserved (do not connect); static memory data input/output bit 6 with internal pull-down resistor
V_{SSP}	176	ground	–	pad ground
SM_D9	177	input/output	4	reserved (do not connect); static memory data input/output bit 9 with internal pull-down resistor
SM_D5	178	input/output	4	reserved (do not connect); static memory data input/output bit 5 with internal pull-down resistor
SM_D10	179	input/output	4	reserved (do not connect); static memory data input/output bit 10 with internal pull-down resistor

SYMBOL	PIN	INPUT/OUTPUT[1]	I_{max} (mA)	DESCRIPTION
SM_D4	180	input/output	4	reserved (do not connect); static memory data input/output bit 4 with internal pull-down resistor
V_{SSCO}	181	ground	–	internal pre-driver and substrate ground
V_{SSCO}	182	ground	–	core ground
V_{DDCO}	183	supply	–	core supply voltage (2.5 V)
V_{DDCO}	184	supply	–	internal pre-driver supply voltage (2.5 V)
V_{DDP}	185	supply	–	pad ring supply voltage (3.3 V)
SM_D11	186	input/output	4	reserved (do not connect); static memory data input/output bit 11 with internal pull-down resistor
SM_D3	187	input/output	4	reserved (do not connect); static memory data input/output bit 3 with internal pull-down resistor
SM_D12	188	input/output	4	reserved (do not connect); static memory data input/output bit 12 with internal pull-down resistor
SM_D2	189	input/output	4	reserved (do not connect); static memory data input/output bit 2 with internal pull-down resistor
V_{SSP}	190	ground	–	pad ground
SM_D13	191	input/output	4	reserved (do not connect); static memory data input/output bit 13 with internal pull-down resistor
SM_D1	192	input/output	4	reserved (do not connect); static memory data input/output bit 1 with internal pull-down resistor
SM_D14	193	input/output	4	reserved (do not connect); static memory data input/output bit 14 with internal pull-down resistor
SM_D0	194	input/output	4	reserved (do not connect); static memory data input/output bit 0 (LSB) with internal pull-down resistor
V_{DDP}	195	supply	–	pad ring supply voltage (3.3 V)
SM_D15	196	input/output	4	reserved (do not connect); static memory data input/output bit 15 (MSB) with internal pull-down resistor
$\overline{SM\_CS3}$	197	output	4	reserved (do not connect); static memory chip select output for external ROM or RAM (active LOW)
SM_A4	198	output	4	reserved (do not connect); static memory address output bit 4
SM_A3	199	output	4	reserved (do not connect); static memory address output bit 3
V_{SSP}	200	ground	–	pad ground
SM_A2	201	output	4	reserved (do not connect); static memory address output bit 2
SM_A15	202	output	4	reserved (do not connect); static memory address output bit 15
SM_A1	203	output	4	reserved (do not connect); static memory address output bit 1
SM_A16	204	output	4	reserved (do not connect); static memory address output bit 16
V_{DDP}	205	supply	–	pad ring supply voltage (3.3 V)
SM_A0	206	output	4	reserved (do not connect); static memory address output bit 0 (LSB)
SM_A17	207	output	4	reserved (do not connect); static memory address output bit 17 (MSB)
$\overline{SM\_CS0}$	208	output	4	reserved (do not connect)

Notes

1. All input pins, input/output pins (in input mode), output pins (in 3-state mode) and open-drain output pins are limited to 3.3 V.
2. If used with external clock source the input voltage has to be limited to 2.5 V.
3. In accordance with the *"IEEE 1149.1"* standard.
4. Special function of pin $\overline{\text{TRST}}$:
   a) For board designs without boundary scan implementation, pin $\overline{\text{TRST}}$ must be connected to ground.
   b) Pin $\overline{\text{TRST}}$ provides easy initialization of the internal BST circuit. By applying a LOW level it can be used to force the internal Test Access Port (TAP) controller to the Test-Logic-Reset state (normal operating) immediately.

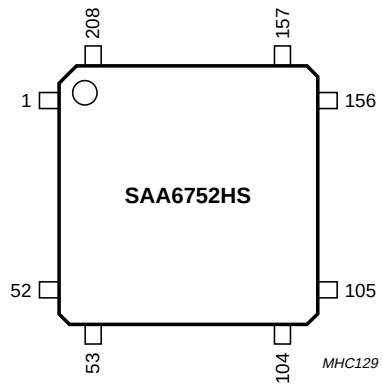


Fig.2 Pin configuration.

7 FUNCTIONAL DESCRIPTION

7.1 System operation

7.1.1 GENERAL

The SAA6752HS has a multi-processor architecture. The different processing and control modules are not locked to each other but run independently within the limits of the global scheduling. The data transfer between the processing units is carried out via FIFO memories or the external SDRAM. The device is configured and the operation modes are selected via the I^2C-bus.

7.1.2 OPERATING MODES

There are five operating modes:

1. **Idle.** This mode is set after applying a hard reset (i.e. on power-up). In this mode the SAA6752HS can be initialized by the host to the required configuration. Video and audio processing is disabled. A hard reset always resets the SAA6752HS configuration parameters back to the default states.
2. **Stop.** In Stop mode, the video and audio input processing is enabled but the multiplexer output remains disabled. It is possible to read status information on the input video and audio signals via the I^2C-bus. The SAA6752HS initialization settings cannot be modified, except to some specific dynamic encoding parameters (i.e. bit rate setting).
3. **Encode.** In this mode, the multiplexer output is enabled. Like Stop mode, only dynamic encoding parameters can be modified in this mode.
4. **Paused.** This mode allows the SAA6752HS to make seamless transitions. Restarting from Paused mode will generate a stream output with sequential time stamps and MPEG buffer model content.
5. **Power-down.** In this mode, the internal clock is disabled, sending the SAA6752HS into a (non-functional) power saving state. A hard reset will re-initialize the SAA6752HS.

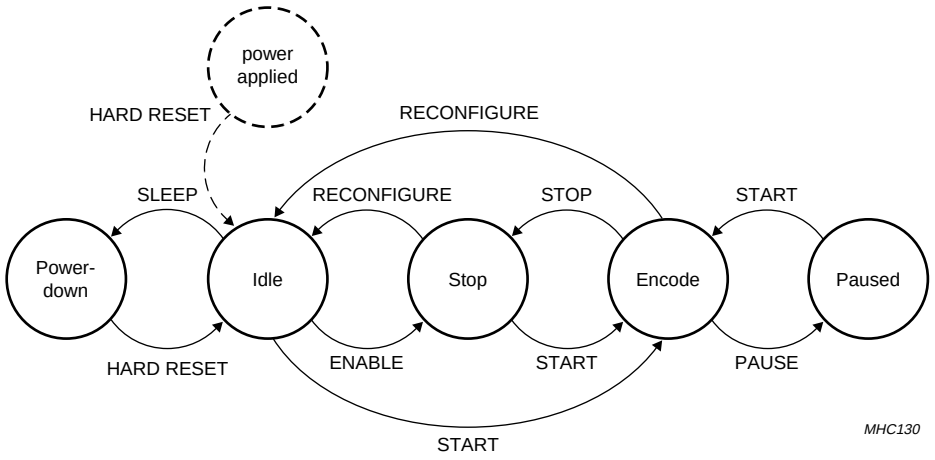


Fig.3 Mode transition diagram.

7.1.3 Mode transition commands

There are seven mode transition commands:

1. **SOFT RESET.** Like a hard reset, a soft reset can be applied in any mode, setting the SAA6752HS back to Idle mode and resetting all configuration parameters back to the default settings.
2. **RECONFIGURE.** This command sets the SAA6752HS back to Idle mode without resetting the configuration parameters back to the default settings.
3. **ENABLE.** This transition sets Stop mode, enabling the video and audio input processing.
4. **START.** This transition sets Encode mode, enabling the multiplexer stream output. Note that if the SAA6752HS is commanded to start from the Idle mode, then the internal transition is via the Stop mode.
5. **STOP.** This command will disable the multiplexer stream output, setting the SAA6752HS to Stop mode. The current GOP and/or audio frame is completed and an end of sequence bit appended to the stream.
6. **PAUSE.** A PAUSE transition will cause the multiplexer to complete the current GOP and/or audio frame but no end of sequence bit is appended. The current MPEG buffer model contents are saved to provide a seamless transition on START.
7. **SLEEP.** This mode disables the internal clock.
8. **FORCED RECONFIGURE.** A STOP command whilst in the Encode mode will not work in case the video or audio input signal is interrupted, because for stopping, the SAA6752HS tries to finish the current GOP. The forced reconfigure command allows a mode transition back to the Idle state, without losing the actual configuration settings.

The SAA6752HS is not able to process any other commands during mode transitions. In this event, a get running mode request will return a busy flag. The completion of a mode transition can also be flagged as an event using the host interrupt pin.

7.2 Digital video input

7.2.1 General

The video front-end processes an *"ITU-R BT.601/605"* compliant video stream for conversion to 4 : 2 : 0 format (MP@ML). It includes synchronization, digital video signal processing through several filters, subsampling, sliced/raw VBI data handling, and SDRAM address generation.

The video interface is designed for use with Philips SAA7114 digital multi-standard decoder or similar video decoders. The input interface accepts a digital video input stream according to *"ITU-R-BT.601"*. 625 lines standard at 50 Hz and 720 pixels by 576 lines as well as 525 lines at 60 Hz and 720 pixels by 480 lines are covered. The video synchronization may either follow *"ITU-R-BT.656"* recommendation or can also be supplied by external signals (HSYNC, VSYNC and FID). The formatter module performs a colour conversion from 4 : 2 : 2 to 4 : 2 : 0 format. Optionally, also SIF progressive down-scaling and 2/3D1, 1/2D1 down-scaling may be activated.

The SAA6752HS supports non-standard features of the SAA711x series of video input processors, such as hard-wired external synchronization signals (2 and 3-wire sync), special VCR playback signal streams (IEC 756 subset for VCR playback and still pictures), extraction of sliced data from the input video stream.

7.2.2 Video front-end configuration options

The following configuration options can be selected from the host:

- VIDEO INPUT PORT SELECTION. Two input clock pins are selectable.
- VIDEO INPUT FORMAT. 525 or 625-line formats can be selected.
- VIDEO SYNC FORMAT. Various combinations and polarities of HSYNC, VSYNC and Field Information (FID) can be selected as the source of sync signal processing.
- VIDEO FILTER SETTINGS. Noise pre-filter and horizontal filters can be enabled and, if the default coefficients are not suitable for an application, new coefficients can be set.
- VIDEO FORMAT CONVERSION. Selection of conversion from D1 to 1/2D1, 2/3D1 or SIF progressive down-scaling.
- VBI DATA EXTRACTION. VBI data extraction of WSS or CC data can be enabled.

7.2.3 Video encoder status information

The following configuration option can be selected from the host:

- VBI DATA: WSS and CC data can be read back via the I^2C-bus.

7.2.4 Data input format

7.2.4.1 Interface definition

The data input interface uses 13 pins, all of which are inputs (see Table 1). Pins YUV0 to YUV7 carry video and synchronization data and 3 pins are reserved for control purposes. Two separate clock inputs allow two different signal sources to be used. The input clock can be asynchronous to the SAA6752HS system clock.

Table 1 List of pins data input port

PIN	DESCRIPTION
YUV0 to YUV7	video input signal (synchronous to VCLK)
FID	odd/even field identification signal; note 1
HSYNC	horizontal synchronization signal; note 1
VSYNC	vertical synchronization signal; note 1
VCLK1 or VCLK2	video clock signal (from source 1 or 2)

Note

1. In ITU-T 656 mode sync signals are embedded in the video data input stream. The external sync signals are not used.

7.2.5 Video signal processing

7.2.5.1 Acquisition of video data

Data is latched with the incoming video clock to provide robust data capture. Video clock and data is unlocked to the internal system clock therefore a clock domain bridge is used. This is performed by oversampling of video clock and data with 108 MHz.

7.2.5.2 Sync decoding and filtering

To allow selection of the right portion of the video input stream, synchronization signals from the stream are recognized by a sync decoder. This checks the incoming field (FID), vertical sync and horizontal sync. It is possible to select either ‘internal synchronization’ (which means that SAV/EAV codes in the ITU 601/656 video streams are used) or externally applied hardware synchronization signals (which are given by the video input processor). In the latter case, 3 pin or 2 pin (V-sync and H-sync only) synchronization can be used.

Using 2 pin synchronization, the FID information is given by the timing of the transition of the V-sync. If a Vertical Blanking Interval (VBI) starts during H-sync, the next field will be the top field, otherwise it will be the bottom field.

A sync filter is used to inhibit sync signal triggering if an incorrect number of pixels or lines has been input. It also checks for the correct consecutive fields. The filter works on three different levels. An H-sync is only accepted after a predefined number of video cycles, a V-sync is only accepted after a programmed number of lines and a field is only accepted if top field follows bottom field or vice versa.

7.2.5.3 Horizontal and vertical shift

This function is intended for correction in synchronization of external sync signals if incorrectly timed. The amount of shift is programmable via the I^2C-bus.

7.2.5.4 SAV/EAV decoder

A SAV/EAV decoder extracts the F, V and H bits from the video timing reference code. The decoder evaluates the protection bits to be able to correct one bit errors within the code word. If multiple bit errors are detected, the protection bits are ignored and the field (F), vertical sync (V) and horizontal sync (H) bits are directly extracted from the code.

7.2.5.5 Video format conversion

The SAA6752HS converts the input video input signal to the formats defined in Table 2 controlled by the I^2C-bus command. A 4 : 2 : 2 to 4 : 2 : 0 colour conversion is performed as this is a pre-requisite of MPEG MP@ML encoding.

Table 2 Format conversion

MODE	PICTURE FORMAT (PIXEL/LINES)
D1	720
2/3D1	480
1/2D1	352; note 1
SIF	352; notes 1 and 2

Notes

1. The 8 pixels at the right edge of the scaled picture are not encoded.
2. Top field only.

7.2.6 VIDEO FILTERING

7.2.6.1 Adaptive mean filter

The SAA6752HS uses an adaptive mean filter. There are three different filter modes that can be selected: median, averaging or no filter.

The median algorithm provides better noise performance and is well suited to suppress single noise spikes without degrading the signal edges. The averaging algorithm is a standard low-pass filter so has greater impact on signal edges.

The default threshold and gain coefficients of this filter can be overwritten via the I^2C-bus to allow user optimization for different applications.

7.2.6.2 Horizontal pre-filter/decimation filter

There is a horizontal filter for Y and C and this can operate as a pre-filter or decimation filter. It is a symmetrical FIR filter with up to 8 coefficients programmable via the I^2C-bus.

7.2.6.3 Vertical chrominance filtering

For 4 : 2 : 2 to 4 : 2 : 0 conversion, vertical filtering and subsampling of the chrominance is performed. The sequence of coefficients is mirrored in top and bottom field. This generates the right phases of the chrominance samples between the luminance samples (a non co-sited sampling scheme).

7.2.7 VBI DATA EXTRACTION

The SAA6752HS supports the extraction of WSS and CC data using two independent VBI data extractor modules. The data is available via the I^2C-bus.

The following VBI data formats are supported: Closed Caption (CC525 and CC625) and Wide Screen Signalling (WSS525 and WSS625). For CC525, CC625 and WSS625 the sliced data from a video input processor (e.g. SAA7114) are extracted from the digital video input signal and can be read via the I^2C-bus. For WSS525 an internal data slicer is available which slices the oversampled raw data, which are delivered by the video input processor. The extracted WSS525 signal can be read via the I^2C-bus.

7.3 Video compression

7.3.1 GENERAL

Compression of video data is performed by the video compressor block; see Fig.4. The input to this block is the uncompressed video information pre-processed by the video front-end and stored in external SDRAM memory. The output is a compressed video stream, compliant to MPEG-2 Video Elementary Stream (VES) up to slice level. Controlling information (for example, quantizer step size) as well as the bit stream for higher layers of the VES is generated by the embedded MIPS® processor of the SAA6752HS.

The video compressor contains several subblocks. The MacroBlock Processor (MBP) performs generation of video ES on macroblock level. Controlling parameters for this task and MB headers as well as slice headers are generated by the core control subblock. Bitstream formatting and concatenation of MBP bitstream and header information is done by the subblocks pre-packer and packer.

7.3.2 Video encoder configuration options

The following configuration options can be selected from the host:

- VIDEO COMPRESSION SETTINGS. I, IP and IPB encoding with various GOP structures can be selected.
- ENCODER BIT RATE. The bit rate for variable bit rate or constant bit rate modes can be programmed using bit rate and quantization control parameters. These parameters can be adjusted whilst encoding, not just set at initialization.
- ENCODER PERFORMANCE TUNING. The ability for the user to tune encoding performance is provided by allowing control of adaptive quantization depth. Also the SAA6752HS allows download of new quantizer matrix contents.

7.3.3 Video encoder status information

The following status information is available to the host:

- CURRENT ENCODER BIT RATE. The actual encoded bit rate, as number of bytes per GOP, is available allowing the use of constrained variable bit rate algorithms to fine tune the encoding efficiency.

7.3.4 GOP structure

The programmable GOP structure features a reference frame distance (M) up to 3, and a GOP length (N) of up to 19. Supported structures are real closed GOP(M,N) and backward predicted closed GOP(M,N). For the use of B-frames in D1 and 2/3D1 mode a 64 Mbit SDRAM is needed.

In D1 mode, B-frames will be unidirectional. Backward predicted closed GOPs may have the first one (M = 2) or two (M = 3) B-frames referenced inside the GOP dependent on the I^{2}C-bus register settings. This is intended for editable applications as GOPs are independent of each other. Non-editable GOPs allow the first one (M = 1) or two (M = 2) B-frames to be referenced to the P-frame in the previous GOP. This is a non-editable format but has optimum encoding efficiency. This structure is sometimes called an open GOP. The first one (M = 1) or two (M = 2) B-frames in the first GOP of a sequence are always forced backwards predicted.

Table 3 GOP

GOP LENGTH (N)	REFERENCE FRAME DISTANCE (M)			
	0	1	2	3
1	I	(1)	(1)	(1)
2	(1)	IP	(1)	(1)
3	(1)	IPP	IBP(2)	(1)
4	(1)	IPPP	BIBP(3)	IBBP(2)
5	(1)	IPPPP	IBPBP(2)	(1)
6	(1)	IPP...PP	BIBPBP(3)	BBIBBP(3)
7	(1)	IPP...PP	IBP...BP(2)	IBBPBBP(2)
8	(1)	IPP...PP	BIBP...BP(3)	(1)
9	(1)	IPP...PP	IBP...BP(2)	BBI...BBP(3)
10	(1)	IPP...PP	BIBP...BP(3)	IBBP...BBP(2)
11	(1)	IPP...PP	IBP...BP(2)	(1)
12	(1)	IPP...PP	BIBP...BP(3)	BBI...BBP(3)
13	(1)	IPP...PP	IBP...BP(2)	IBBP...BBP(2)
14	(1)	IPP...PP	BIBP...BP(3)	(1)
15	(1)	IPP...PP	IBP...BP(2)	BBI...BBP(3)
16	(1)	IPP...PP	BIBP...BP(3)	IBBP...BBP(3)
17	(1)	IPP...PP	IBP...BP(2)	(1)
18	(1)	IPP...PP	BIBP...BP(3)	BBI...BBP(3)
19	(1)	IPP...PP	IBP...BP(2)	IBBP...BBP(2)

Notes

1. Undefined.
2. This GOP structure is defined as a Real Closed GOP (RCG).
3. This GOP structure is defined as a Backward Predicted Closed GOP (BPCG) or Non-Editable GOP (NEG), selectable via the I^{2}C-bus.

7.3.5 Bit rate control

The SAA6752HS supports two modes of video bit rate control: variable bit rate and constant bit rate.

The Variable Bit Rate (VBR) mode is intended for burst data transfer applications, where the bit rate is allowed to vary but the image quality should be constant. In this mode, a combination of three parameters can be set: Rvbr, Qmin_VBR and Qmax_VBR. While aiming at the target bit rate Rvbr, only quantizer scale values within the range between Qmin_VBR and Qmax_VBR are applied. Broadening this range leads to greater variations in picture quality but better adherence to Rmax. Constriction of this range forces a better constancy in picture quality at the expense of meeting the target bit rate. Note that optimal control results require reasonable combinations of Rmax, Qmin_VBR and Qmax_VBR. Furthermore, the maximum bit rate Rmax can be set. If Rmax is reached in VBR mode, the CBR algorithm takes over the control by increasing the quantizer scale values temporarily (over Qmax_VBR) to guarantee that Rmax is never exceeded. Hence, the closer Rmax and Rvbr are chosen, the more the control in VBR mode turns to CBR mode behaviour.

The Constant Bit Rate (CBR) mode is intended for applications, where a fixed channel rate is provided (e.g. transmission systems). A tight control of the quantizer scale is applied to make optimal use of the given bandwidth. The parameter Rmax specifies the required constant bit rate.

Independent of the bit rate mode (CBR or VBR), a B-frame weighting factor (the weighting factor is applied to the quantization scale) can be applied to further reduce the bit rate of B-frames. In IP-only GOP structures, every second P-frame is weighted by this factor generating ‘virtual B-frames’ to simulate a bit rate distribution similar to IPB sequences. This feature can further improve the perceptual rate-distortion ratio by taking advantage of the inertia of the human visual system.

7.3.6 Adaptive quantization

Adaptive quantization is an algorithm that uses internal generated statistics to fine tune the quantizer scale used for encoding a specific macroblock. For example, the controller adapts the quantization scale with respect to the local complexity distribution within a frame, resulting in a perceptually smoother picture quality. The amount of fine tuning can be adjusted by control of the adaptive quantization depth.

7.3.7 Quantizer matrix table download

The MPEG standard default quantizer matrices can be overwritten to allow picture encoding optimization.

7.3.8 User data insertion

User data insertion of up to 64 bytes is supported on GOP and picture level.

7.3.9 Motion adaptive noise reduction

The gain and adaptivity can be controlled to optimize encoding efficiency in case of noisy input sequences, i.e. off-air reception.

7.3.10 Compression block partitioning

The video compression block, shown in Fig.4, contains the following sub-modules:

- **MacroBlock Processor (MBP).** Reads uncompressed video data from SDRAM and generates the compressed bitstream on MB level (without MB headers). Addresses for frame buffer (previous frame) access are generated by the MBP.
- **Core control.** Performs MB and slice header generation, base address generation for the current MB (uncompressed), motion vector candidate generation, and computation of encoding statistics required by the CPU for bit rate controlling.
- **Pre-packer** (part of packing unit). Since the MBP output words are not necessarily fully used (i.e. some output words may contain unused bits) the pre-packer packs the output of the MBP in such a way that all words contain valid bits. This reduces the amount of memory required for storing the MB data.
- **Packer** (part of packing unit). Merges header and MB headers.

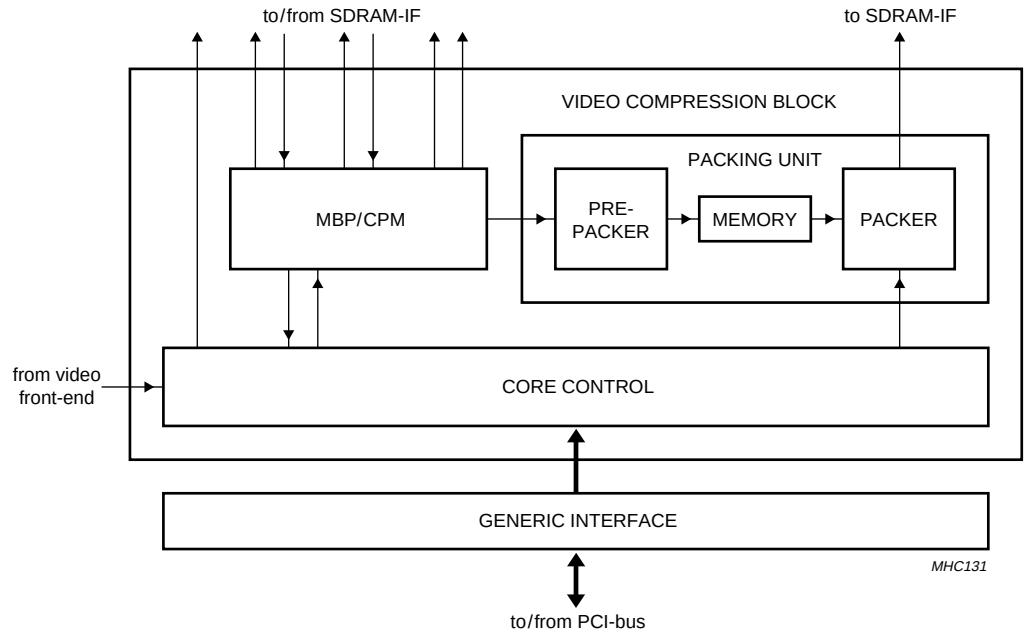


Fig.4 Video compressor block diagram.

7.4 Digital audio input

7.4.1 General

The audio input interface (I^2S) accepts serial digital audio data and supports master and slave mode. The interface is able to handle 16 to 20 bits audio data with left and right channel. Audio data with more than 20-bit word width is accepted as input, but the additional bits are ignored.

7.4.2 Audio port configuration options

The following configuration options can be selected from the host:

- AUDIO INPUT PORT SELECTION. Two digital audio input ports are selectable.
- AUDIO INPUT FORMAT. Various I^2S and EIAJ formats can be selected.
- AUDIO INPUT MODES. Master or slave mode can be selected.
- AUDIO CLOCK OUTPUT. An audio clock output (256×48 kHz or 384×48 kHz) can be used for external analog-to-digital converter clocking.
- AUDIO OUTPUT. The second audio interface port can be configured as output in special applications e.g. concurrent encoding of audio and video without internal multiplexing of the two streams.

7.4.3 Input formats

The digital audio input interface can select between two digital audio input ports via I^2C-bus control and is able to input the following audio formats:

- I^2S, see Fig.5
- EIAJ, see Fig.6
- EIAJ alternative format.

The alternative formats are defined as having the word select shifted by one clock cycle with respect to the data.

EIAJ and EIAJ alternative format are supported for 16, 18 and 20-bit resolution. I^2S and I^2S alternative format are supported for 16, 18, 20 and 24-bit resolution. Input data is truncated to 20 bits internally if 24-bit resolution is applied.

Each of the formats can be applied in master or slave mode.

When in master mode, the external audio analog-to-digital convertor must be clocked using the audio clock generated by the SAA6752HS. This can be set to 256×48 kHz or 384×48 kHz (locked to the video frame frequency).

In slave mode an internal sample rate converter converts the input sample frequency to a video frame locked 48 kHz sample frequency.

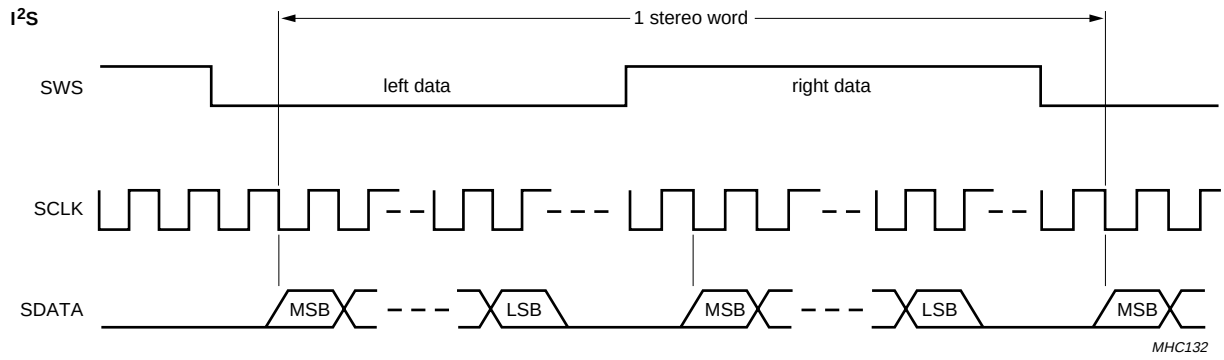


Fig.5 I^2S mode format protocol.

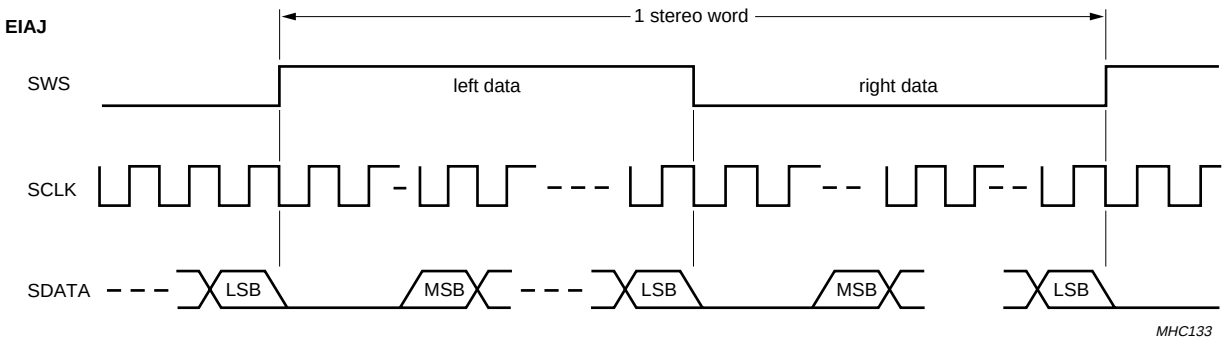


Fig.6 EIAJ mode format protocol.

7.4.4 AUDIO INPUT PROCESSING

In order to be able to cope with analog and digital sources, the I^2S input ports can be configured as master (analog) or slave (digital). For the slave mode however, a sample rate converter will be involved, except for DVD-compliant audio bypass. Table 4 reflects the different configuration possibilities.

Table 4 Audio input processing modes

PROCESSING MODE[1]	AUDIO CONTENT FORMAT	INPUT SAMPLE FREQUENCY (kHz)		NO. OF ENCODED BITS	ENCODED BIT RATE (kbits/s)
		MASTER[2]	SLAVE[3][4]		
MPEG-1 L2 encoding	LPCM at 16, 18, 20 or 24 bits[5][6]	48	32 kHz ±0.1% 44.1 kHz ±0.1% 48 kHz ±0.1%	20	256, 384
DDC encoding[7]	LPCM at 16, 18, 20 or 24 bits[5]	48	32 kHz ±0.1% 44.1 kHz ±0.1% 48 kHz ±0.1%	20	256, 384
LPCM bypass (uncompressed audio format)[8]	LPCM at 16, 18, 20 or 24 bits[5]	48	32 kHz ±0.1% 44.1 kHz ±0.1% 48 kHz ±0.1%	16	–
DVD-compliant audio bypass	16 bits[9]	–	48 kHz[10]	16	–

Notes

1. Processing modes can be changed when SAA6752HS is in Idle mode.
2. In master mode, the external audio source must use the SAA6752HS audio clock as a clock source.
3. A sample rate conversion process will convert incoming data to a nominal 48 kHz audio frequency that is locked to V-sync of the video input signal (if present). The sample rate converter is not enabled for DVD-compliant bypass mode.
4. The sample rate conversion input frequency range has been selected to be compatible with class 2 SPDIF receivers.
5. 24-bit input option only applies to I^2S input formats, in this event it will be truncated to 20 bits internally in the SAA6752HS before processing. EIAJ formats are limited to 20 bits maximum.
6. The MPEG encoder gain is set to −3 dB.
7. Only for SAA6752HS/101.
8. In systems that use 16 Mbit SDRAM due to system architecture constraints, LPCM bypass must be restricted to be used with I and IP video encoding only. There is no constraint if 64 Mbit SDRAM is used.
9. The IEC 60958 format defines 20 bits for an audio sample, plus 4 auxiliary bits, which can be used to extend the word length. IEC 61937 uses only 16 data bits of each IEC 60958 sub-frame. It depends on the settings of an external SPDIF to I^2S converter if 16, 18, 20 or 24 bits are transferred to the SAA6752HS.
10. For DVD-compliant bypass mode the audio clock must be locked to the video clock externally.

7.5 Audio compression

7.5.1 General

The digital audio signal from the I^2S input port is compressed according to MPEG-1 layer 2 and DDC (AC-3) encoding (SAA6752HS/101 only). The constant bit rate is programmable via the I^2C-bus.

An audio stream with 16 to 20 bits and a sampling frequency of 48 kHz can be processed. A higher accuracy of more than 20 bits is ignored. A bypass mode can be selected for LPCM for 16-bit data resolution and compressed audio signals (MPEG-1 layer 2, MPEG-2, DD and DTS) according to IEC 61397 or LPCM. The format of such compressed inputs is identified and made accessible via the I^2C-bus.

7.5.2 Audio encoder configuration options

The following configuration options can be selected from the host:

- AUDIO PROCESSING MODES. MPEG-1 L2 or DDC (AC-3) encoding (only in SAA6752HS/101) modes can be selected. Two bypass modes are also available: LPCM bypass and DVD-compliant bitstream bypass.
- AUDIO MUTE. It is possible to mute the audio data prior to encoding.

7.5.3 Audio encoder status information

The following configuration options can be selected from the host:

- DVD-BYPASS HEADER INFORMATION. Header information is available to allow the host to determine the content of the bypassed audio data stream. This includes information from the Preamble Pc, Preamble Pd and audio frame headers.

7.5.4 MPEG-1 layer 2 encoding

MPEG-1 layer 2 encoding can be selected. The available I^2C-bus settings are:

- No pre-emphasis (default setting)
- 50/15 μs (compliant to ISO 11172-3)
- CCITT J.17 (compliant to ISO 11172-3).

7.5.5 DDC encoding (only for SAA6752HS/101)

Dolby® Digital Consumer (DDC) encoding mode can be selected. The encoder performance is suitable for consumer electronic recordable DVD systems.

7.5.6 LPCM bypass

16-bit LPCM audio streams can be bypassed by the audio encoder module.

7.5.7 DVD-compliant audio bypass

DVD-compliant bypass and pause burst handling is selectable in accordance to IEC 61937. Preamble Pc, Preamble Pd and part of the elementary stream header are captured and made available via the I^2C-bus. If any non DVD-compliant formats are detected then these are flagged via host interrupt.

Table 5 DVD-compliant audio bypass

MODE	BIT RATE	SAMPLE FREQUENCY	CHANNEL CONFIGURATION
MPEG-1/2 layer 2 without extension	64 to 384 kbit/s	48 kHz only	mono, stereo or multi-channel up to 7.1
MPEG-2 layer 2 with extension	up to 912 kbit/s	48 kHz only	mono, stereo or multi-channel up to 7.1
Dolby® digital	64 to 448 kbit/s	48 kHz only	1/0, 2/0, 3/0, 2/1, 3/1, 2/2 and 3/2
DTS-1	192 to 1536 kbit/s	48 kHz only	stereo or multi-channel up to 5.1

7.6 SDRAM interface

7.6.1 General

The external SDRAM is used as memory for storing video and audio information during the compression process. It is also used as a buffer for the output stream. The interfacing to and from the functional blocks is done via a number of internal FIFO memories.

The SAA6752HS will support 16 Mbit@16 bit ($512k \times 16 \times 2$) and 64 Mbit@16 bit ($1024k \times 16 \times 4$) SDRAM devices. The minimum recommended speed of the SDRAM is 125 MHz. Recommended SDRAMs include the Samsung K4S641632D-TC/L80 and K4S161622D-TC/L80 devices.

7.7 Multiplexer

7.7.1 General

The system stream multiplexer combines compressed audio and video streams into a single MPEG system stream. Presentation data is synchronized by the use of time stamps as specified in the MPEG systems standards. The multiplexer ensures an MPEG-compliant multiplexing with respect to buffer maintenance, synchronization and data alignment. It takes care of the system specific requirements for D-VHS, DVD, DVB and ATSC.

7.7.2 Multiplexer configuration options

The following configuration options can be selected from the host:

- STREAM FORMAT. Selection of audio or video elementary stream, packetized elementary stream, program stream or transport stream options and general system parameters including maximum system bit rate, number of flushing bytes and PES header IDs.
- TRANSPORT STREAM SYSTEM MODES. In TS mode, it is possible to set packet IDs and download system information tables.

7.7.3 Multiplexer status information

The following status information can be selected from the host:

- METABYTES INFORMATION. If selected and in program stream or pack stream, it is possible to insert video and audio status information into the stream output as special metabyte data packets for later system processing.
- NUMBER OF BYTES PER GOP. It is possible to read the current system bit rate of the output stream.

7.7.4 Elementary stream output

Video and audio elementary stream outputs can be selected.

7.7.5 Packetized elementary stream output

Packetized Elementary Stream (PES) outputs can be selected. There are two options: PES (DVD) and PES (TS). Variable bit rate is only available in PES (DVD) mode and constant bit rate only available in PES (TS) mode.

The video and audio PES IDs can be programmed via the I^2C-bus. Original copy or copyright flags can also be set.

7.7.6 Program stream output

Program stream output, intended for storage recording applications, can be selected. Time slot reservation for navigation packets is available. Metabytes can be appended after each pack, see Section 7.7.9.

7.7.7 Pack stream output

A special mode called pack stream can be selected. This is a program stream but without the MPEG buffer model implemented. This minimizes the throughput time of video and audio data through the SAA6752HS and is intended for applications where low latency is important. In this mode no program stream header is inserted.

7.7.8 Transport stream output

Transport stream output can be selected. The video, audio and PCR (clock) Packet Identifiers (PIDs) can be programmed. System information tables can be transferred to the SAA6752HS via the I^2C-bus. If transport stream output is combined with DIO master mode as output mode then packets are sent in a controlled way, so that a set-top box can be connected.

7.7.9 Metabytes data

In program stream and pack stream modes, the SAA6752HS can append additional metabyte data packets to the stream, providing information on sector information for downstream application processing. The video and audio metabytes format is defined in Tables 6 and 7. The sector and metabytes form a block format, where each sector of 2048 bytes is followed by 16 metabytes containing data on the previous sector.

Table 6 Video metabytes data

BYTE (HEX)	NAME	LSB/ MSB	BIT	DESCRIPTION
00	identification		0 to 7	55H; video
01	flags		0	‘GOP start flag’; indicates that a GOP start code is present in the sector
			1	‘GOP start header’; indicates that a group of GOPs starts in the sector
			2	‘sequence end flag’; indicates that a sequence end code is present in the sector
			3 and 4	reserved
			5 to 7	undefined
02	data length	LSB	0 to 7	amount of non-stuffing bytes minus one
03		MSB	0 to 7	
04	time stamp	LSB	0 to 7	The value of the STC at the moment that the first byte of the first frame arrived at the input. Only 32 bits are used; note 1.
05			0 to 7	
06			0 to 7	
07		MSB	0 to 7	
08	picture start count		0 to 7	the amount of picture starts in the sector
09	picture types		0 and 1	1st picture type: 00: I picture 01: P picture 10: B picture 11: invalid type
			2	reserved
			4 and 5	2nd picture type: 00: I picture 01: P picture 10: B picture 11: invalid type
			6	reserved
0A	first picture position	LSB	0 to 7	position (in bytes) of the first picture (or GOP or sequence) start code in the sector
0B		MSB	0 to 7	
0C	second picture position	LSB	0 to 7	position (in bytes) of the first picture (or GOP or sequence) start code in the sector
0D		MSB	0 to 7	
0E	GOP header position	LSB	0 to 7	position (in bytes) of the GOP start code in the sector, if present, else 0000
0F		MSB	0 to 7	

Note

1. This is the same value as used to generate the PTS and DTS values.

Table 7 Audio metabytes data

BYTE (HEX)	NAME	LSB/ MSB	BIT	DESCRIPTION
00	identification		0 to 7	AAH; audio
01	flags		0	reserved
			1	‘terminated audio flag’; this flag is only set at the end of a recording session and indicates that this sector is not completely filled with audio data
			2	‘synchronization flag’; indicates that the audio data in the sector is related in time to the beginning of a Video Object Unit (VOBU)
			3	reserved
			4	reserved
			5 to 7	audio pack type: 000: MPEG-1 layer 2 or MPEG-2 without extension 010: MPEG-2 with extension 011: DDCE (only for SAA6752HS/101) 100: DTS-1 (512 samples/frame) 101: reserved 110: reserved 111: LPCM 16-bit stereo 48 kHz
02	data length	LSB	0 to 7	amount of non-stuffing bytes minus one
03		MSB	0 to 7	
04	time stamp	LSB	0 to 7	The value of the STC at the moment that the first byte of the first frame arrived at the input. Only 32 bits are used; note 1.
05			0 to 7	
06			0 to 7	
07		MSB	0 to 7	
08	reserved		0 to 7	00
09	frame start count		0 to 7	the amount of frame starts in the sector
0A	first frame position	LSB	0 to 7	position (in bytes) of the first frame in the sector
0B		MSB	0 to 7	
0C	last frame position	LSB	0 to 7	position (in bytes) of the last frame in the sector
0D		MSB	0 to 7	
0E	reserved		0 to 7	00
0F	reserved		0 to 7	00

Note

1. This is the same value as used to generate the PTS value.

7.8 MPEG stream output port

7.8.1 General

The MPEG stream output port connects the SAA6752HS multiplexer output to the outside world. The parallel interface performs a parallel output transition of audio and video data to an externally connected device and supports 3-bus protocol modes.

7.8.2 Output port configuration options

The following configuration options can be selected from the host:

- OUTPUT PROTOCOL. Three output protocols can be selected: DIO slave mode, DIO master mode and DEBI slave mode and associated signalling pin polarities.
- OUTPUT DISABLE. Output can be set to high-impedance if the SAA6752HS is not used in application.

7.8.3 Data output format

The data to be transmitted have a width of 8 bits in all modes. The data output port supports DIO and DEBI bus protocols. The bus protocol mode is set via an I^2C-bus controlled register. The DEBI protocol provides only a transmission of 8-bit data block transfer without address decoding.

7.8.4 Protocol description

Table 8 Output port definitions

PORT	I/O	DESCRIPTION
PDIDS	I	Request from external system if interface is in DEBI slave mode.
PDIOCLK	I/O	Output clock to the external system if interface is set to DIO master mode. Input clock to the SAA6752HS if interface is set to DIO slave mode.
PDO[7:0]	O	output data (8-bit parallel)
PDOSYNC	O	Indicates a first byte of a data packet (for transport streams in DIO mode).
PDOAV	O	Indicates when an audio packet is output (for transport stream).
PDOVAL	O	Indicates whether currently sent data is valid.

7.8.4.1 DIO master mode

The PDIOCLK clock for the DIO interface is derived from the system clock by a division of the 27 MHz clock by 3 or by 4, generating a data output clocked at 9 or 6.75 MHz. A PDOVAL signal indicates whether current data at the output is valid. If the output buffer is empty the PDOVAL signal will stay LOW. The number of valid pulses indicate the real number of data transmissions. The signal PDOSYNC in conjunction with PDOVAL indicates the first byte of a transport stream packet.

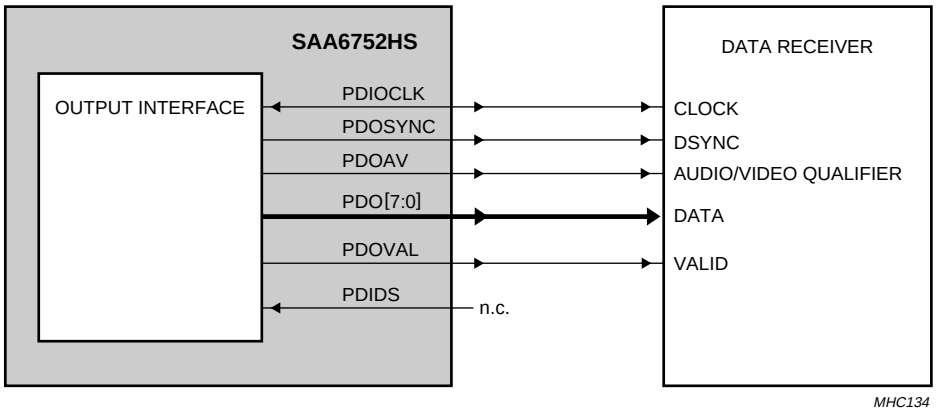


Fig.7 DIO master mode protocol.

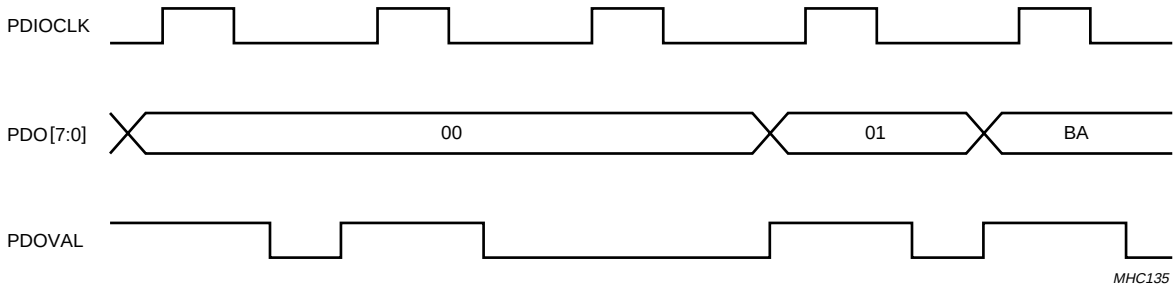


Fig.8 Data transfer in DIO master mode.

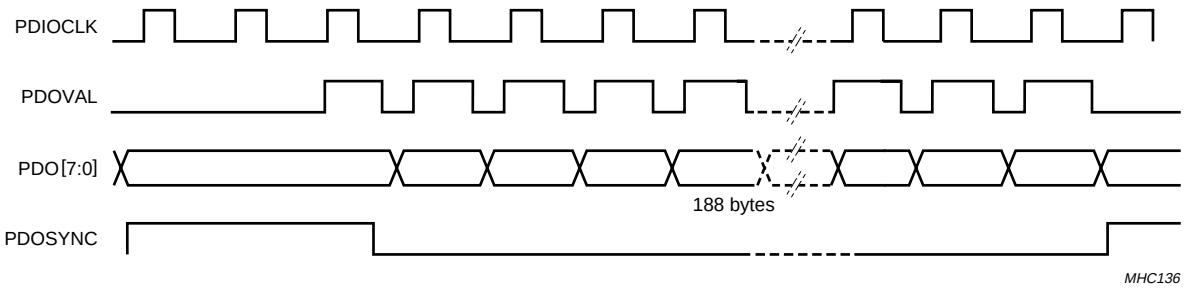


Fig.9 DIO master mode, transport stream packet.

7.8.4.2 DIO slave mode

The SAA6752HS can be enabled in a DIO slave mode where the data receiver acts as master. PDO, PDOSYNC and PDOAV are clocked out by the internal clock; earliest two internal clock cycles e.g. 36 to 58 ns after the falling edge of the external clock. The external clock PDIOCLK should not exceed a maximum of 9 MHz. The PDOVAL signal still indicates if data is available in the output buffer. To operate in this mode, the PDIDS request input must be set to logic 1.

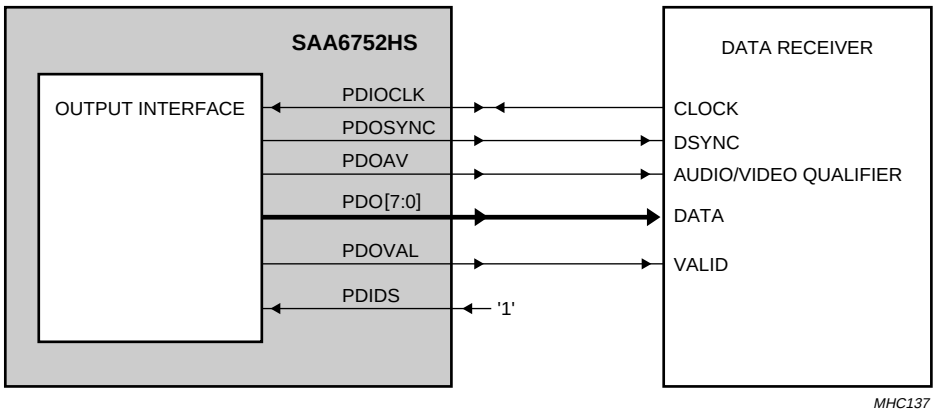


Fig.10 DIO slave mode protocol.

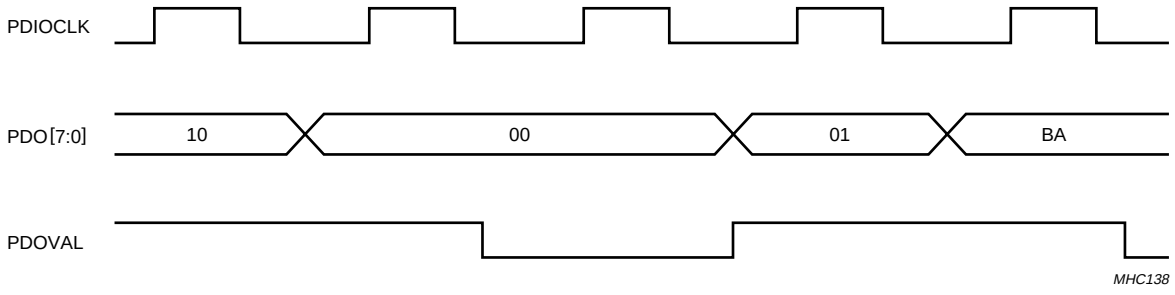


Fig.11 Data transfer in DIO slave mode.

7.8.4.3 DEBI slave mode

The SAA6752HS supports DEBI slave mode with a block transfer of 8-bit data. This can be used for interfacing with a PCI bridge (for example, an SAA7146A chip set). There is no addressing phase necessary. The transfer starts with recognition of a PDIDS pulse. The requested data, PDO[7:0], is transferred when the PDOVAL signal goes HIGH, indicating that data is available in the output buffer. In the event of interfacing to an SAA7146A chip set, the PDOVAL pin is connected to the $\overline{\text{DTACK\_RDY}}$ pin and serves as a handshake. The LDS_RDN and UDS_WRN signals should be used to generate the PDIDS signal.

Note that to operate correctly to the DEBI transfer protocol the VALID output signal should be inverted by the I^2C-bus command.

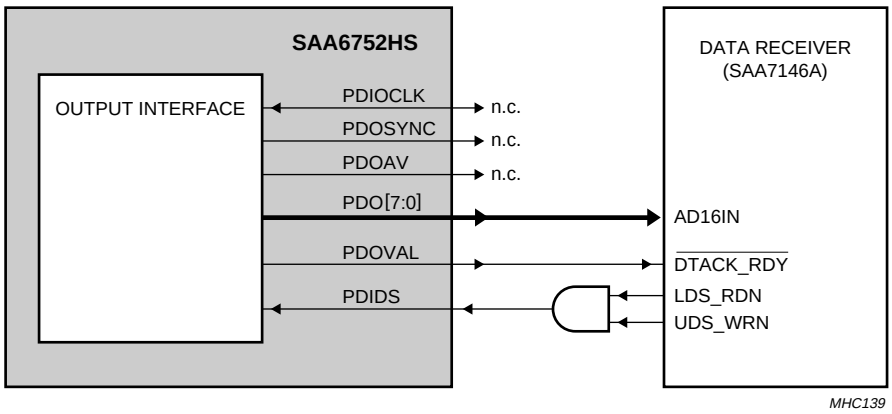


Fig.12 DEBI slave mode protocol.

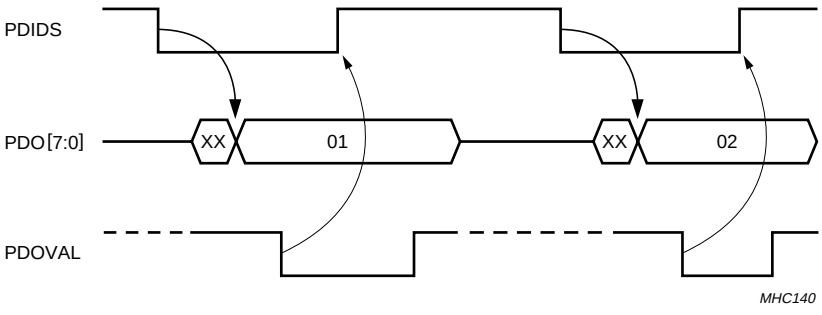


Fig.13 Data transfer in DEBI slave mode.

7.9 Clock generation

7.9.1 General

The SAA6752HS is designed to operate with a single fundamental 27 MHz crystal or an external 27 MHz clock. From these clock sources an internal PLL produces the 27 MHz, 54 MHz and 108 MHz frequencies needed for operation.

It is possible to use a third overtone crystal in combination with a 9 MHz external trap. In this event Clock mode 2 and tuning by the I^2C-bus commands are not usable.

7.9.2 Clock configuration options

The following configuration options can be selected from the host:

- CLOCK MODE. Dependent on the type of application (i.e. video frame locked, reference clock locked etc.), three different clock modes are available
- CLOCK SOURCE. The clock can be generated from an internal crystal controlled clock or an external source. If from a crystal then a fine tune adjustment is available
- CLOCK OUTPUT. It is possible to enable a system clock output so that the 27 MHz clock can be used elsewhere by the user.

7.9.3 Clock Modes

The SAA6752HS internal PLL can be configured in three different clock modes: Clock modes 1, 2 and 3. A definition of the clock modes is shown in Table 9. The clock modes are intended for different applications:

- Clock mode 1. System clock reference locked to input video frame frequency. Intended for applications where the output stream is recorded directly onto a medium (i.e. DVD video recorder).
- Clock mode 2. Crystal locked to input video frame frequency. Intended for applications that require both recording and direct playback. However it is limited by the required accuracy of the input video frame frequency
- Clock mode 3. Crystal free-running. Intended for applications where the output stream is played real time directly by a decoder.

To meet the requirements for each clock mode the conditions specified in Table 10 must be met.

Table 9 Clock modes

CLOCK MODE	OUTPUT STREAM TIME-STAMP COMPLIANCE	SYSTEM FREQUENCY	SYSTEM CLOCK REFERENCE FREQUENCY
1	DVD-compliant(1)	crystal frequency	27 MHz ± video frame frequency accuracy
2	DVD and MPEG-compliant	27 MHz ± video frame frequency accuracy	27 MHz ± video frame frequency accuracy
3	MPEG-compliant	crystal frequency	crystal frequency

Note

1. The stream contents are MPEG-compliant but the time stamps are not synchronized with real time (i.e. dependent on the accuracy of the video input frame frequency). Playback of such a stream is MPEG-compliant due to the re-generation of time synchronization.

Table 10 Clock modes requirements

CLOCK MODE	CRYSTAL FREQUENCY	EXTERNAL CLOCK FREQUENCY	INPUT VIDEO FRAME FREQUENCY(1)
1	27 MHz ±0.1%	27 MHz ±0.1%	nominal – 8% to nominal + 2%
2	$27 \times (1 \pm 200 \times 10^{-6})$ MHz (to allow fine tuning via PLL)	not applicable	nominal $\times (1 \pm 200 \times 10^{-6})$
3	$27 \times (1 \pm 30 \times 10^{-6})$ MHz	$27 \times (1 \pm 30 \times 10^{-6})$ MHz	not applicable

Note

1. The nominal video frame frequency is dependent on the video mode set: 525 or 625 lines.

7.9.4 Clock mode 2 auto-switch

An auto-switch mode is available if Clock mode 2 is selected. In this event the PLL will switch to Clock mode 1 or 3 if the conditions for Clock mode 2 are no longer met (i.e. video frame frequency outside the range $1 \pm 200 \times 10^{-6}$). The auto-switch preference is set by an I²C-bus command during the SAA6752HS initialization. If auto-switch occurs then a host interrupt can be flagged.

7.9.5 Crystal tuning

It is possible to tune the crystal frequency by up to $1 \pm 200 \times 10^{-6}$ via the I²C-bus. If necessary this can be used to achieve the MPEG-2 accuracy of $1 \pm 20 \times 10^{-6}$ with standard crystals.

7.9.6 External clock source

It is possible to use an external system clock. For start-up before switching to the external clock input a crystal has to be connected or the external frequency has to be applied to pin XTALI. The input voltage for this pin must be limited to 2.5 V. An external clock source cannot be used with Clock mode 2.

7.9.7 Audio clock

A switchable sampling frequency for an audio Analog-to-Digital Converter (ADC) is generated by the internal PLL. Two sampling frequencies are selectable: 256×48 kHz and 384×48 kHz. This clock output can be used as clock signal for an external audio ADC. The system clock reference frequency as described in Table 9, is used as reference for the internal PLL generating the audio clock.

7.10 Power control and reset

7.10.1 General

An external reset pulse at power-up is needed to start-up the SAA6752HS. This will start the oscillator and initialize hardware and firmware. The SAA6752HS can be set to a power saving sleep mode where all internal clocks are switched off. In this mode restarting can only be done by a hard reset pulse.

7.11 I²C-bus interface

7.11.1 General

The I²C-bus interface within the SAA6752HS is a slave transceiver. It is used for all control settings. The read mode may be used to read back error or status codes.

The I²C-bus interface is compliant to the I²C-bus standard at 100 kHz and 400 kHz clock frequency and suitable for bus line voltage levels of 3.3 V. If an I²C-bus with higher voltage is used by an application, it is possible to add a small interface between 3.3 V and a higher voltage level. Only two MOSFET transistors (e.g. BSN10, BSN20 or BSS83) are needed. A description of this circuit is available at http://www.semiconductors.philips.com/i2c/facts/

Information about the I²C-bus can be found in the brochure *"The I²C-bus and how to use it"* (order number 9398 393 40011).

7.11.2 Slave Addresses

Two write I²C-bus slave addresses (SAD) are available, 40H and 42H (8-bit), dependent on the state of address select pin I2CADDRSEL. This avoids possible address conflict of addresses with other devices. A HIGH-level at the address selection pin will set the device write address to 42H.

Similarly for read operations there are two slave addresses: 41H and 43H. A HIGH-level at the address selection pin will set the device read address to 43H.

7.12 Exception handling

7.12.1 General

The SAA6752HS is capable of flagging certain events to a host via a host interrupt flag pin H_IRF. The host is able to read back a 16-bit status word via the I²C-bus to identify the specific event and take action accordingly. Detectable events include copyright violations, loss of input synchronization, DVD compliance errors etc.

7.12.2 Exception conditions

A list of the SAA6752HS exception conditions, as indicated by the status word, is defined in Table 11. The I²C-bus subaddress is 12H (see Table 14).

Table 11 Interrupt status definition

STATUS WORD BIT	EXCEPTION CONDITION	RESPONSE IF EXCEPTION IS DETECTED
0	video copyright violation	SAA6752HS continues encoding; see note 1.
1	input video signal not detected or lost	SAA6752HS continues encoding but outputs audio ES packets only; SAA6752HS will resynchronize if video input is recommenced; notes 2 and 3.
2	when a difference between the V-sync period in I^2C-bus settings and in the video input signal is detected	SAA6752HS continues but frames may be lost during the event.
3	Clock mode 2 out of range	If enabled, the SAA6752HS PLL will auto-switch to Clock mode 1 or 3 as programmed.
4	output buffer overflow (due to loss of data read command)	Stream output stops or corrupted data will be delivered; reset needed to recover.
5	video and audio time stamps out of alignment	Video and audio in output stream lose synchronization.
6	input audio not DVD-compliant (to IEC 61937) incorrect Preamble Pc sampling frequency out of range bit rate out of range SAA6752HS/102: switching to DDCE	SAA6752HS continues encoding but will not include audio packets.
7	audio format change detected in DVD bypass mode	SAA6752HS continues encoding but will not include audio packets.
8	audio pause burst detected	SAA6752HS continues operation.
9	SAA6752HS mode transition complete	SAA6752HS continues operation.
10	illegal I^2C-bus command I^2C-bus command not recognized command in invalid mode command parameter error	SAA6752HS ignores the I^2C-bus command.
11	general error	SAA6752HS will go to Idle mode if time-out is enabled or stop operating if time-out is disabled; in case of the later a forced reconfigure is recommended.
12	input audio word select signal not detected or audio stream stopped after exception status bit 4, 6, 7 or 8	SAA6752HS continues encoding but outputs video ES packets only; transition to STOP needed to recover.
13	VBI WSS data has been captured	SAA6752HS continues operation.
14	VBI CC data has been captured	SAA6752HS continues operation.
15	video frame drop	SAA6752HS continues operation, video and audio output restart resynchronized.

Notes

1. ‘No copy’ flag is only detected if the correct WSS or CC VBI mode is enabled.
2. This error flag detects mismatches between the input video format (525 or 625) and SAA6752HS video setting (525 or 625). Video syncs out of range are also detected.
3. A loss of video sync is flagged if 10 consecutive syncs are not detected.

7.12.3 HOST INTERRUPT OPERATION

A HIGH level as signalled by the host interface pin indicates that an exception condition has been detected. The host interrupt flag pin H_IRF is reset to LOW by reading the interrupt status word via the I^2C-bus.

7.12.4 INTERRUPT MASKING

It is possible to mask any combination of exception conditions by setting a 16-bit interrupt mask via the I^2C-bus.

8 BOUNDARY SCAN TEST

8.1 General

The SAA6752HS has built-in logic and 5 dedicated pins to support boundary scan testing, which allows board testing without special hardware (nails). The SAA6752HS follows the *"IEEE Std. 1149.1 - Standard Test Access Port and Boundary Scan Architecture"* set by the Joint Test Action Group (JTAG) chaired by Philips.

The 5 special pins are: Test Mode Select (TMS), Test Clock (TCK), Test Reset ($\overline{TRST}$), Test Data Input (TDI) and Test Data Output (TDO).

The Boundary Scan Test (BST) functions BYPASS, EXTEST, SAMPLE, CLAMP and IDCODE are all supported (see Table 12). Details on the JTAG BST-TEST can be found in the specification "*IEEE Std. 1149.1"*. A file containing the detailed Boundary Scan Description Language (BSDL) description of the SAA6752HS is available on request.

Table 12 Boundary Scan Test (BST) instructions

INST	DESCRIPTION
BYPASS	This mandatory instruction provides a minimum length serial path (1-bit) between TDI and TDO, when no test operation of the component is required.
EXTEST	This mandatory instruction allows testing of off-chip circuitry and board level interconnections.
SAMPLE	This mandatory instruction can be used to take a sample of the inputs during normal operation of the component. It can also be used to preload data values into the latched outputs of the boundary scan register.
CLAMP	This optional instruction is useful for testing, when not all ICs have BST. It addresses the bypass register, while the boundary scan register is in external test mode.
IDCODE	This optional instruction will provide information on the components manufacturer, part number and version number.

8.2 Initialization of boundary scan circuit

The Test Access Port (TAP) controller of an IC should be in the reset state (TEST_LOGIC_RESET), when the IC is in functional mode. This reset state also forces the instruction register into a functional instruction such as IDCODE or BYPASS.

To solve the power-up reset, the standard specifies that the TAP controller will be forced asynchronously to the TEST_LOGIC_RESET state by setting pin $\overline{TRST}$ to LOW.

8.3 Device identification codes

A device identification register is specified in *"IEEE Std. 1149.1-1990 - IEEE Standard Test Access Port and Boundary Scan Architecture*". It is a 32-bit register which contains fields for the specification of the IC manufacturer, the IC part number and the IC version number.

Its biggest advantage is the possibility to check for the correct ICs mounted after production and determination of the version number of ICs during field service.

When the IDCODE instruction is loaded into the BST instruction register, the identification register will be connected between TDI and TDO of the IC.

The identification register will load a component specific code during the CAPTURE_DATA_REGISTER state of the TAP controller and this code can subsequently be shifted out. At board level this code can be used to verify component manufacturer, type and version number. The device identification register contains 32 bits, numbered 31 to 0, where bit 31 is the most significant bit (nearest to TDI) and bit 0 is the least significant bit (nearest to TDO); see Fig.14.

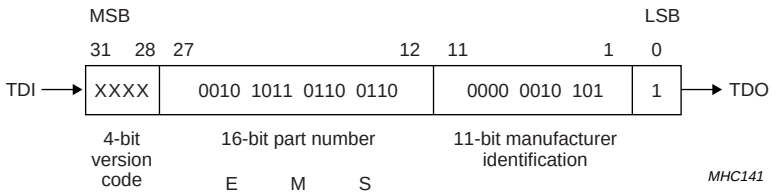


Fig.14 32 bits of identification code.

9 I²C-BUS CONTROL AND STATUS REGISTERS

Tables 13 to 26 list the I²C-bus instructions intended for functional control and status.

Column M identifies the SAA6752HS modes that are valid for each I²C-bus instruction. The key is:

I - write and/or read valid in Idle mode

P- write and/or read valid in Paused mode

S - write and/or read valid in Stop mode

E - write and/or read valid in Encode mode

All - write and/or read valid in Idle, Encode, Paused and Stop mode.

Table 13 I²C-bus control

ADR HEX	M	COMMAND NAME	R/W	SIZE/POSITION	PARAMETER/RANGE	DEFAULT	DESCRIPTION
00	all	soft reset	W	none	none	–	This command resets the SAA6752HS to its default settings.
01	I	enable	W	none	none	–	go to Stop mode from Idle mode
02	I, P, S	start	W	none	none	–	go to Encode mode
03	E	stop	W	none	none	–	go to Stop mode from encode mode
04	E	pause(1)	W	none	none	–	go to Paused mode from encode mode
05	E, P, S	reconfigure	W	none	none	–	go to Idle mode
06	I	sleep	W	none	none	–	go to Power-down mode
07	E, P, S	forced reconfigure	W	none	none	–	Go to Idle mode without completing the current GOP/audio frame. This is intended for use in cases similar to no video/audio input present.
08	I	enable system time-out	R/W	1 byte		disabled	Enables SAA6752HS to time-out to Idle mode if STOP to IDLE transition cannot be completed (i.e. due to no video signal being present). If a general error event is detected, the SAA6752HS will automatically switch to Idle mode via forced reconfigure.
				bit 0 = 1	enabled		
				bit 0 = 0	disabled		

Note

1. Paused mode transitions are not applicable to transport stream and DIO output mode combination, only transport stream and DEBI output mode combination.

Table 14 I²C-bus status

ADR HEX	M	COMMAND NAME	R/W	SIZE/POSITION	PARAMETER/RANGE	DEFAULT	DESCRIPTION
10	all	get running mode	R	1 byte		–	This command gets the actual running mode from the SAA6752HS and is read-only. The busy flag indicates that the SAA6752HS is working at a control command. If the busy flag is set, the SAA6752HS skips all received I²C-bus commands.
				bit 0 = 1	idle		
				bit 1 = 1	encoding		
				bit 2 = 1	stopped		
				bit 3 = 1	paused		
				bit 4 = 1	reserved		
				bit 5 = 1	busy flag		
11	all	status mask	W	2 bytes (16 bits)		all 0's	masking of events; see Table 11
				bit = 0	event disabled		
				bit = 1	event enabled		
12	all	interrupt status	R	2 bytes (16 bits)		–	This command allows reading a status register. Reading the status will clear the status and reset the interrupt assertion pin.
				bit = 0	no event detected		
				bit = 1	event detected		
13	all	get version number	R	12 bytes	–	–	This command allows reading of the current MIPS® firmware version number, hardware number and the audio DSP firmware number. Each number contains 4 bytes.

Table 15 I²C-bus SDRAM size

ADR HEX	M	COMMAND NAME	R/W	SIZE/POSITION	PARAMETER/RANGE	DEFAULT	DESCRIPTION
20	I	bus width and memory size	R/W	1 byte		16 bit 64 Mbit	bus width of the SDRAM interface and size of connected SDRAM
				bit[1:0] = 00	16 Mbit 16-bit wide		
				bit[1:0] = 10	64 Mbit 16-bit wide		
				bit[1:0] = 11	reserved		

Table 16 I²C-bus clock static/dynamic settings

ADR HEX	M	COMMAND NAME	R/W	SIZE/POSITION	PARAMETER/RANGE	DEFAULT	DESCRIPTION
30	I	clock mode	R/W	1 byte		mode 1	
				bit[1:0] = 01	mode 1		mode 1: crystal frequency fixed; SCR frequency frame locked to V-sync
				bit[1:0] = 10	mode 2		mode 2: crystal frequency frame locked to V-sync
				bit[1:0] = 11	mode 3		mode 3: crystal frequency fixed
31	I	clock source	R/W	1 byte		crystal clock	This command is used to switch from an internal crystal controlled clock source to an external clock source and vice versa.
				bit 0 = 0	crystal clock		
				bit 1 = 1	external clock		
32	I	clock auto mode	R/W	1 byte		mode fixed	This command sets the behaviour of the SAA6752HS in Clock mode 2 if video sync cannot be achieved. Either mode 2 is continued or the SAA6752HS will automatically switch to mode 1 or mode 3, as selected.
				bit[1:0] = 00	mode fixed		
				bit[1:0] = 01	enable mode 2 and 1 auto-switch		
				bit[1:0] = 10	enable mode 2 and 3 auto-switch		
33	I	enable system clock output	R/W	1 byte		disable	This command outputs the internal crystal generated clock (27 MHz) to an output pin CLKOUT for use in other parts of an application.
				bit 0 = 0	disabled		
				bit 0 = 1	enabled		
34	all	adjust crystal oscillator	R/W	1 byte	–128 to +127	0	adjust the frequency of the oscillator

Table 17 I²C-bus video front-end input interface static settings

ADR HEX	M	COMMAND NAME	R/W	SIZE/POSITION	PARAMETER/RANGE	DEFAULT	DESCRIPTION
40	I	625/525	R/W	1 byte		625	defines the input signal either as 625 lines or 525 lines
				bit[1:0] = 00	625		
				bit[1:0] = 01	525		
41	I	subsampling type	R/W	1 byte		D1	specifies the subsampling type
				bit[1:0] = 00	D1		
				bit[1:0] = 01	2/3D1		
				bit[1:0] = 10	1/2D1		
				bit[1:0] = 11	SIF		
42	I	video sync format	R/W	1 byte		0	defines the incoming video sync sources
				bit[1:0] = 00	H-sync, V-sync and Field Identification (FID) information coded in the EAV/SAV bytes complying to ITU-R BT.656		
				bit[1:0] = 01	separate H-sync, V-sync and FID signals input to from external source(s)		
				bit[1:0] = 10	separate H-sync and V-sync signals input to from external source(s)		
43	I	video clock select	R/W	1 byte		video clock 1	defines which external video input clock is used
				bit 0 = 0	video clock 1		
				bit 0 = 1	video clock 2		
44	I	vertical sync timing adjustment	R/W	2 bytes		0, 0	
				byte 0	0 to 225		defines the number of shifted lines in the top field
				byte 1	0 to 225		defines the number of shifted lines in the bottom field
45	I	horizontal shift	R/W	2 bytes	0 to 511 (bits 0 to 8)	0	defines the number of shifted cycles for every field

ADR HEX	M	COMMAND NAME	R/W	SIZE/POSITION	PARAMETER/RANGE	DEFAULT	DESCRIPTION
46	I	sync polarity	R/W	byte		000	defines the polarity of the sync signals
				bit 0 = 0	H-sync signal HIGH for horizontal blanking		
				bit 0 = 1	H-sync signal LOW for horizontal blanking		
				bit 1 = 0	V-sync signal HIGH for vertical sync		
				bit 1 = 1	V-sync signal LOW for vertical sync		
				bit 2 = 0	FID signal LOW for first field		
				bit 2 = 1	FID signal HIGH for first field		
47	–	reserved	–	–	–	–	–

Table 18 I²C-bus video front-end filters static/dynamic settings

ADR HEX	M	COMMAND NAME	R/W	SIZE/POSITION	PARAMETER/RANGE	DEFAULT	DESCRIPTION
50	I, E, P, S	noise pre-filter off/on	R/W	1 byte		off	enables or disables noise pre-filter and selects the mode for this filter
				bit[1:0] = 00	off		
				bit[1:0] = 01	median filter		
				bit[1:0] = 10	average filter		
51	I, E, P, S	noise pre-filter coefficients	R/W	4 bytes	4 × 6 bits; bits 0 to 5 valid	33H, 20H, 16H, 0DH	defines the filter coefficients for the noise pre-filter
52	I, E, P, S	noise pre-filter thresholds	R/W	3 bytes	3 × 6 bits; bits 0 to 5 valid	10, 15, 20	defines the threshold coefficients for the median filter
53	I, E, P, S	horizontal filter off/on	R/W	1 byte		off	enables or disables the horizontal filter by bypassing
				bit 0 = 0	off		
				bit 0 = 1	on		
54	I, E, P, S	horizontal filter coefficients	R/W	16 bytes	array of word (8 × 10 bits)	first word = 256, the others = 0	Defines the coefficients for the horizontal filter; the default applies to D1 mode only. When other subsampling modes are selected the SAA6752HS automatically overwrites the horizontal filter coefficients with the appropriate parameters.
55	I, E, P, S	horizontal filter scaling factor	R/W	1 byte (4 bits)	0 to 15	8	Defines the scaling factor for the horizontal filter; the default applies to D1 mode only. When other subsampling modes are selected the SAA6752HS automatically overwrites the horizontal filter scaling parameter with the appropriate parameter.

Table 19 I²C-bus video front-end VBI data extraction

ADR HEX	M	COMMAND NAME	R/W	SIZE/POSITION	PARAMETER/RANGE	DEFAULT	DESCRIPTION
60	I	VBI mode select	W	5 bytes		–	
				bit 0 = 0	WSS mode		selects between WSS and CC modes
				bit 0 = 1	CC mode		
				bit 8 = 0	data input sliced		Selects if the input data is sliced by the video input processor (sliced) or by the SAA6752HS (unsliced).
				bit 8 = 1	data input unsliced		
					sliced data		sent in case of sliced input data
				bit[17:16]	data type[3:2]		The data type compared with the data type field in the VBI data header for extraction decision; bits 3 and 2.
				bit[23:18]	SDID, 0 to 63		The SDID compared with the SDID field in the VBI data header for extraction decision.
				bit[28:24]	line number, 0 to 31		line number of data as set by the video input processor
				bit 29 = 0	top field		field dependent on video input processor setting
				bit 29 = 1	bottom field		
				bit[31:30]	data type[1:0]		The data type compared with the data type field in the VBI data header for extraction decision; bits 1 and 0.
				bit 32 = 1	field qualifier mask SDID		match the SDID
				bit 33 = 1	field qualifier mask data type		match data type
				bit 34 = 1	field qualifier mask field		match field
				bit 35 = 1	field qualifier mask line number		match line number
				bit[39:36]	reserved		must be set to zero

ADR HEX	M	COMMAND NAME	R/W	SIZE/POSITION	PARAMETER/RANGE	DEFAULT	DESCRIPTION
60	I	VBI mode select (continued)	W	continued	**unsliced data**	–	sent in case of unsliced input data
				bit[20:16]	line number for bottom, 0 to 31		line number for bottom field as set by the video input
				bit[28:24]	line number for top, 0 to 31		line number for top field as set by the video input
				bit[37:32]	reserved		must be set to zero
				bit 38 = 1	field qualifier mask line field 1		match if field = ‘top’ and line = ‘line number’
				bit 39 = 1	field qualifier mask line field 2		match if field = ‘bottom’ and line = ‘line number’
61	I	WSS data enable	R/W	1 byte		disabled	enables or disables WSS data extraction
				bit[1:0] = 00	disabled		
				bit[1:0] = 01	enabled		
				bit[1:0] = 10	enabled without checksum		
62	all	WSS read data	R/W	2 bytes	–	–	WSS data and flag indicating valid data
				bit[13:0]	WSS data		
				bit 14 = 0	valid data		
				bit 14 = 1	invalid or previous data		
63	I	CC data enable	R/W	1 byte		disabled	enables the closed caption data extraction
				bit 0 = 0	disabled		
				bit 0 = 1	enabled		
64	all	CC read data	R	3 bytes		–	CC data and flags indicating valid data and current field
				bit[15:0]	CC data		
				bit 16 = 0	top field		
				bit 16 = 1	bottom field		
				bit 23 = 0	valid data		
				bit 23 = 1	invalid data		

Table 20 I²C-bus video encoder: general

ADR HEX	M	COMMAND NAME	R/W	SIZE/POSITION	PARAMETER/RANGE	DEFAULT	DESCRIPTION
70	I	disable video encoder	R/W	1 byte		enabled	Specifies if the video encoder is enabled. If the video encoder is disabled, no video data will be inserted in the output stream.
				bit 0 = 0	enabled		
				bit 0 = 1	disabled		
71	I	bit rate mode	R/W	1 byte		VBR	defines the encoding bit rate
				bit 0 = 0	VBR		
				bit 0 = 1	CBR		
72	I	GOP definition	R/W	2 bytes		0001H: M = 0; N = 1	Defines the used GOP structure as (N.M), where 'N' is the number of frames per GOP and 'M' is the distance of 2 sequential I- or P-frames (reference frame distance); distance = 0 is I-frame coding; see Table 3 for meaningful combinations.
				byte 0	distance (M) (0 to 3)		
				byte 1	length (N) (0 to 19)		
73	I	user data GOP header	R/W	64 bytes		all 0	Specifies the data to be inserted into the GOP header.
74	I	number of user data GOP	R/W	1 byte		0	Specifies the amount of user data to be inserted into the GOP header.
75	I	number of user data picture header	R/W	1 byte		0	Specifies the amount of user data to be inserted into the picture header.
76	I	user data picture header	R/W	array of bytes [64]		all 0	Specifies the data to be inserted into the picture header.
77	I	noise filter coefficients	R/W	2 bytes	array of coefficients	off	Defines the noise filter coefficients gain and criterion scale.
78	I	adaptive quantization depth	R/W	1 byte	0 to 128	32	Selects the depth of quantization adaptation; 0 for no adaptation, 128 for maximum adaptation.
79	I	quantizer matrix	R/W	2 × 64 bytes	array of integers (8 × 8 bytes)	–	Specifies the quantizer matrix as 2 tables, each an 8 × 8 array. Data must be transferred column by column, not row by row. The inter Q matrix must be downloaded first, the intra Q matrix downloaded second; see note 1.
7A	I	reserved	–	–	–	–	–

ADR HEX	M	COMMAND NAME	R/W	SIZE/POSITION	PARAMETER/RANGE	DEFAULT	DESCRIPTION
7B	I	disable forced backward prediction	R/W	1 byte		0	Applies only for GOP structures starting with a B-frame: disabled forced backward prediction results in non-editable (open) GOPs with prediction from a former GOP. Enabled forced backward prediction results in backward predicted closed GOPs without prediction from a former GOP. In all cases the leading B-frames of the very first GOP structure after start of encoding are forced to backward prediction.
				bit 0 = 0	enabled		
				bit 0 = 1	disabled		
7C	I	scan select	R/W	1 byte		0	
				bit 0 = 0	alternate scan		
				bit 0 = 1	zigzag scan		
7D	I	quantizer scale table	R/W	1 byte		0	
				bit 0 = 0	logarithmic		
				bit 0 = 1	linear		

Note

1. If no Q matrix is downloaded then the default is the MPEG standard and no Q matrix is inserted into the stream.

Table 21 I²C-bus video encoder: bit rate control (dynamic settings)

ADR HEX	M	COMMAND NAME	R/W	SIZE/POSITION	PARAMETER/RANGE	DEFAULT	DESCRIPTION
80	I, E, P, S	Rvbr	R/W	2 bytes	–	6000	VBR target bit rate (kbit/s); this applies to VBR mode only; Rvbr must be set to less than Rmax.
81	I, E, P, S	Rmax	R/W	2 bytes	–	9800	CBR mode: target bit rate (kbit/s); VBR mode: maximum bit rate (kbit/s); Rmax should only be set in 1 kbit/s increments; note 1.
82	I, E, P, S	Qmin_VBR	R/W	1 byte	1 to 112	4	Minimum Q-scale for external constraints of VBR
83	I, E, P, S	Qmax_VBR	R/W	1 byte	1 to 112	12	Maximum Q-scale for external constraints of VBR.
84	I, E, P, S	B-frame weighting	R/W	1 byte	32 to 128	128, no weighting	B-frame weighting factor (internally divided by 128; i.e. 128 = no effect)
85	I, E, P, S	read bytes per GOP	R	4 bytes	–	–	This command reads the number of bytes per GOP.

Note

1. If the video bit rate Rmax is intended to be changed during the encoding state, the maximum applied value for Rmax has to be set before start of encoding. I.e. the Rmax value that was valid at start of encoding (coming from stop) is the maximum allowed value for this encoding process.

Table 22 I²C-bus audio encoder: bit rate control (static settings)

ADR HEX	M	COMMAND NAME	R/W	SIZE/POSITION	PARAMETER/RANGE	DEFAULT	DESCRIPTION
90	I	disable audio encoder	R/W	1 byte		0	Specifies if the audio encoder is enabled. If the audio encoder is disabled, no audio data will be inserted in the output stream.
				bit 0 = 0	enabled		
				bit 0 = 1	disabled		
91	I	audio input format	R/W	1 byte		I²S	defines the audio input format
				bit[2:0] = 000	I²S		
				bit[2:0] = 001	reserved		
				bit[2:0] = 010	EIAJ 16 bits		
				bit[2:0] = 011	EIAJ 18 bits		
				bit[2:0] = 100	EIAJ 20 bits		
				bit[2:0] = 101	EIAJ alternative format 16 bits		
				bit[2:0] = 110	EIAJ alternative format 18 bits		
				bit[2:0] = 111	EIAJ alternative format 20 bits		
92	I	audio input mode and port select	R/W	1 byte		slave, port 1	In master mode, SAA6752HS delivers the bit clock and word select signal. In slave mode, SAA6752HS receives the bit clock and word select signal. Note that, if I²S port 2 is switched to output mode (VES + AES output stream mode) then SAA6752HS is fixed to master mode.
				bit 0 = 0	master mode		
				bit 0 = 1	slave mode		
				bit 1 = 0	port 1		
				bit 1 = 1	port 2		
93	I	audio processing mode	R/W	1 byte		MPEG-1 L2	defines the audio processing mode (see Section 7.5); note 1
				bit[1:0] = 00	MPEG-1 L2 encode		
				bit[1:0] = 01	DDC encode (only for SAA6752HS/101)		
				bit[1:0] = 10	LPCM bypass		
				bit[1:0] = 11	DVD bypass		

ADR HEX	M	COMMAND NAME	R/W	SIZE/POSITION	PARAMETER/RANGE	DEFAULT	DESCRIPTION
94	I	audio encoding bit rate and output resolution	R/W	1 byte		256 kbit/s 16-bit	defines the audio encoding bit rate (see Section 7.5); note 2
				bit 0 = 0	256 kbit/s		
				bit 0 = 1	384 kbit/s		
				bit 1 = 0	16-bit		
				bit 1 = 1	reserved		
95	I	audio clock output frequency	R/W	1 byte		256 × 48 kHz	selects the output frequency at the audio clock mode
				bit 0 = 0	256 × 48 kHz		
				bit 0 = 1	384 × 48 kHz		
96	I	audio pre-emphasis mode	R/W	1 byte		off	selects audio pre-emphasis mode of input signal (valid for MPEG encoding only)
				bit[1:0] = 00	off		
				bit[1:0] = 01	50/15 ms		
				bit[1:0] = 10	CCITT J17		

Notes

1. In systems that use 16 Mbit SDRAM, due to system architecture constraints, LPCM bypass must be restricted to be used with I and IP video encoding only. There is no constraint if 64 Mbit SDRAM is used.
2. All compressed audio data is 16-bit. In the event of LPCM bypass 20-bit data can be truncated to 16 bits. 16-bit output LPCM bypass mode is DVD-compliant.

Table 23 I^2C-bus audio encoder: bit rate control (dynamic settings)

ADR HEX	M	COMMAND NAME	R/W	SIZE/POSITION	PARAMETER/RANGE	DEFAULT	DESCRIPTION
A0	E, P, S	Preamble Pc	R	1 byte		I^2S	Preamble Pc in case of IEC 61937 input (data type), applies to DVD bypass mode only
				bit[4:0]	data type		
				bit[6:5]	reserved		
				bit 7	error flag indicating validity of burst load		
A1	E, P, S	Preamble Pd	R	2 bytes	Preamble Pd (16 bits)	–	Preamble Pd in case of IEC 61937 input (payload length); this applies to DVD bypass mode only
A2	E, P, S	audio bit stream information	R	8 bytes	bit stream information (4×16 bits)	–	Part of audio frame header in case of IEC 61937 input; this applies to DVD bypass mode only.
A3	–	reserved	–	–	–	–	–
A4	all	audio mute on/off	R/W	1 byte		0	
				bit 0 = 0	off		
				bit 0 = 1	on		

Table 24 I²C-bus multiplexer: general (static settings)

ADR HEX	M	COMMAND NAME	R/W	SIZE/POSITION	PARAMETER/RANGE	DEFAULT	DESCRIPTION
B0	I	output stream format	R/W	1 byte		PS (DVD)	Selects the MPEG-2 output format (see SAA6752HS output stream formats for details):
				bit[2:0] = 000	ES video (VES)		Elementary Stream (ES): Elementary stream output is possible for audio or video only encoding.
				bit[2:0] = 001	ES audio (AES)		
				bit[2:0] = 010	PES (DVD)		Packetized Elementary Stream (PES): DVD-compliant: PES packets have a limited size and can be easily multiplexed into a DVD program stream. TS-compliant: PES packets have an unlimited size and can be easily multiplexed into a transport stream. PES packets containing audio and video information are flagged with an audio/video signal pin. The audio/video polarity of the signal pin is programmable.
				bit[2:0] = 011	PES (TS)		
				bit[2:0] = 100	PS (DVD)		Program Stream (PS): A DVD-compliant program stream is generated, but no navigation packs are inserted.
				bit[2:0] = 101	TS		Transport Stream (TS): A transport stream is generated.
				bit[2:0] = 110	pack stream		Pack stream is a special not MPEG-compliant mode. The MPEG buffer model is not used.
				bit[2:0] = 111	VES + AES		VES + AES mode allows VES output from the output port at the same time as an SPDIF formatted AES is output from the 2nd I²S audio port.
B1	I	maximum system bit rate	R/W	2 bytes	<27000; note 1	10800	Maximum target bit rate of the system stream in kbit/s (= 1000 bit/s) and must be set if TS or PS or pack stream modes are selected. It is ignored if ES or PES streams are selected.
B2	I	number of flushing bytes	R/W	2 bytes	–	0	Number of flushing bytes appended to the stream after a stop.
B3	I	video PES ID	R/W	8 bits	E0H to EFH	E0H	Stream ID for video PES header; must be set for TS, PS and PES output.

ADR HEX	M	COMMAND NAME	R/W	SIZE/POSITION	PARAMETER/RANGE	DEFAULT	DESCRIPTION
B4	I	audio PES ID	R/W	8 bits	C0H to DFH	C0H	Stream ID for audio PES header; must be set for TS, PS and PES output.
B5	I	PES original copy and copyright	R/W	1 byte		copy, no copyright	Copy and copyright setting in audio and video PES header.
				bit 0 = 0	original		
				bit 0 = 1	copy		
				bit 1 = 0	copyright		
				bit 1 = 1	no copyright		
B6	I	multiplexer special DVD PS settings	R/W	1 byte		2 GOPs, off, metabyte, 0 (NAV packet), inserted (PES header)	
				bit[3:0]	1 to 15, number of GOP/VOBU		The number of GOPs per VOBU for PS output.
				bit 4 = 0	metabyte output off		Enables/disables the output of metabytes for PS (DVD) and pack stream modes.
				bit 4 = 1	metabyte output on		
				bit[6:5]	0 to 3, time slot reservation for NAV packets		Specifies the number of reserved time slots for navigation packets and DVD recorder data.
				bit 7 = 0	inserted		Determines if the PES header extension is inserted into the stream; this applies to program stream and pack stream modes; note: for DVD-compliance, the PES header extension must be inserted
				bit 7 = 1	not inserted		
B7	I	audio substream ID	R/W	1 byte	–	00	audio substream ID; for PS (DVD) or PES (DVD) only
B8	E	current system bit rate	R	2 bytes	–	–	Current system bit rate of the system stream in kbit/s (= 1000 bit/s); applies for PS and TS modes. The parameter includes the number of stuffing bytes. During pause mode, this address will read back the value of the last GOP before the pause command.
B9	I	enable MPEG end code	R/W	1 byte		disable	Enables the MPEG end code (for program stream only).
				bit 0 = 1	enable		
				bit 0 = 0	disable		

Note

1. The limit for I-frame only is 27 Mbit/s. For IP or IPB formats the limit is 16 Mbit/s.

Table 25 I²C-bus multiplexer: transport stream (static settings)

ADR HEX	M	COMMAND NAME	R/W	SIZE/POSITION	PARAMETER/RANGE	DEFAULT	DESCRIPTION
C0	I	video TS packet ID	R/W	2 bytes	0020H to 1FFEH	0100H	Packet ID for transport stream packets containing video data; for TS only.
C1	I	audio TS packet ID	R/W	2 bytes	0020H to 1FFEH	0102H	Packet ID for transport stream packets containing audio data; for TS only.
C2	I	system information tables	W	189 bytes (maximum value)	first byte is byte table number range (0 to 4) + array of maximum 188 bytes values	–	There are 5 different tables followed by an array of up to 188 bytes.The tables must be sent one by one; the size of the tables is not defined but limited to 188 bytes. Table 0: Program Association Table (PAT) Table 1: Program Map Table (PMT) Table 2: free programmable [e.g. Conditional Access Table (CAT)] Table 3: free programmable [e.g. Network Information Table (NIT)] Table 4: free programmable [e.g. Selection Information Table (SIT)]
C3	I	insert DIT	R/W	1 byte		disabled	A discontinuity information table is inserted at the beginning of the stream (stop recording).
				bit 0 = 1	enabled		
				bit 0 = 0	disabled		
C4	I	clock TS packet ID	R/W	2 bytes	0020H to 1FFEH	0104H	Packet ID for transport stream packets containing PCR values; for TS only.

Table 26 I²C-bus output interface

ADR HEX	M	COMMAND NAME	R/W	SIZE/POSITION	PARAMETER/RANGE	DEFAULT	DESCRIPTION
D0	I		R/W	1 byte			Defines the output interface in one byte (collects all sub parameter bits in one byte). All states defined are the active states
		output protocol		bit[1:0] = 00	DIO slave mode	DIO slave mode	DIO master mode: SAA6752HS delivers the clock signal. DIO slave mode: SAA6752HS receives the clock signal.
				bit[1:0] = 01	DIO master mode		
				bit[1:0] = 10	not applicable		
				bit[1:0] = 11	DEBI slave mode		
		data valid pin polarity		bit 2 = 0	positive	positive	must be negative if DEBI mode is selected
				bit 2 = 1	negative		
		high impedance on/off		bit 3 = 0	off	on	Selection of high-impedance for output pin.
				bit 3 = 1	on		
		audio/video pin polarity		bit 4 = 0	audio HIGH, video LOW	audio HIGH, video LOW	
				bit 4 = 1	audio LOW, video HIGH		
		sync pin polarity		bit 5 = 0	positive	positive	
				bit 5 = 1	negative		
		data request pin polarity		bit 6 = 0	negative	negative	
				bit 6 = 1	positive		
		PDO clock frequency		bit 7 = 0	9 MHz	9 MHz	
				bit 7 = 1	6.75 MHz		

10 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDP}	digital supply voltage for pads		–0.5	+4.0	V
V_{DDCO}	digital supply voltage for core		–0.5	+2.8	V
V_{DDA}	analog supply voltage		–0.5	+2.8	V
V_I	digital input voltage	note 1	–0.5	+4.0	V
V_i	analog input voltage	note 2	–0.5	+2.8	V
V_O	digital output voltage	note 3	–0.5	V_{DDP} + 0.5	V
I_{sc}	short-circuit current of output pads	note 4	–	125	mA
$I_{lu(prot)}$	latch-up protection current		–	100	mA
P_{tot}	total power dissipation		–	2	W
T_{stg}	storage temperature		–25	+125	°C
T_{amb}	ambient temperature		0	70	°C
V_{es}	electrostatic handling voltage	note 5	–2000	+2000	V
		note 6	–150	+150	V

Notes

1. All pads are not 5 V tolerant.
2. Pins XTALI and XTALO.
3. At V_{DDP} > 3.7 V only maximum 4.2 V at digital outputs is allowed.
4. Short-circuit current is only allowed for a short time (<1 s).
5. Human body model: C = 100 pF; R = 1.5 kΩ.
6. Machine model: C = 200 pF; L = 0.75 μH; R = 0 Ω.

11 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; soldered to a PCB with supply and ground plane	28	K/W

12 CHARACTERISTICS

V_{DDCO} = 2.5 V, V_{DDA} = 2.5 V and V_{DDP} = 3.3 V for the I/O pads; supply voltages V_{DDCO} and V_{DDA} are connected externally together; grounds V_{SSCO}, V_{SSA} and V_{SSP} are connected externally together; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies: pins V_{DDP}, V_{DDCO} and V_{DDA}						
V_{DDP}	digital supply voltage (pad cells)		3.0	3.3	3.6	V
V_{DDCO}	digital supply voltage (core)		2.3	2.5	2.7	V
V_{DDA}	analog supply voltage (oscillator and PLL)		2.3	2.5	2.7	V
I_{DDP}	digital supply current (pad cells)		17	25	37	mA
I_{DDCO}	digital supply current (core)		390	430	500	mA
I_{DDA}	analog supply current		–	3	–	mA
P_{tot}	total power dissipation		0.95	1.16	1.48	W
Input: pins YUV0 to YUV7						
V_{IL}	LOW-level input voltage		–0.5	–	+0.7	V
V_{IH}	HIGH-level input voltage		1.7	–	V_{DDP}	V
V_{hys}	hysteresis voltage		0.4	–	–	V
I_{IL}	LOW-level input current	$V_{IL} = V_{SSP}$	–5	–	–	µA
I_{IH}	HIGH-level input current	$V_{IH} = V_{DDP}$	–	–	5	µA
C_I	input capacitance		–	–	10	pF
Input with pull-up resistor: pins $\overline{\text{CTS}}$, EXTCLK, I2CADDRSEL, PDIDS, $\overline{\text{RESET}}$, RXD, TCK, TDI, TMS and $\overline{\text{TRST}}$						
V_{IL}	LOW-level input voltage		–0.5	–	+0.7	V
V_{IH}	HIGH-level input voltage		1.7	–	V_{DDP}	V
V_{hys}	hysteresis voltage		0.4	–	–	V
$I_{pu(L)}$	LOW-level pull-up input current	$V_{IL} = V_{SSP}$	–20	–50	–70	µA
$I_{pu(H)}$	HIGH-level pull-up input current	$V_{DDCO} < V_{IH} < V_{DDP}$	–	0	10	µA
C_I	input capacitance		–	–	10	pF
Input with pull-down resistor: pins FID, IDQ, HSYNC, SDATA1, VCLK1, VCLK2 and VSYNC						
V_{IL}	LOW-level input voltage		–0.5	–	+0.7	V
V_{IH}	HIGH-level input voltage		1.7	–	V_{DDP}	V
V_{hys}	hysteresis voltage		0.4	–	–	V
I_{pd}	pull-down input current	$V_{DDCO} < V_{IL} < V_{DDP}$	–20	–50	–70	µA
C_I	input capacitance		–	–	10	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs/outputs with I_{max} = 4 mA: pins PDIOCLK, $\overline{SM\_CS0}$, $\overline{SM\_LB}$, $\overline{SM\_UB}$, TEST0, TEST1 and TEST2						
V_{IL}	LOW-level input voltage		–0.5	–	+0.7	V
V_{IH}	HIGH-level input voltage		1.7	–	V_{DDP}	V
V_{hys}	hysteresis voltage		0.4	–	–	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	–	–	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = –4 mA	V_{DDP} – 0.4	–	V_{DDP}	V
I_{sc}	short-circuit current	note 1	–55	–	+55	mA
I_{TL}	3-state leakage current	$V_{IH} = V_{DDP}$; $V_{IL} = V_{SSP}$	–5	–	+5	µA
C_I	input capacitance		–	–	10	pF
C_L	load capacitance		–	–	30	pF
Inputs/outputs with I_{max} = 4 mA and pull-down resistor: pins SCLK1, SCLK2, SDATA2, SM_D0 to SM_D15, SWS1 and SWS2; note 2						
V_{IL}	LOW-level input voltage		–0.5	–	+0.7	V
V_{IH}	HIGH-level input voltage		1.7	–	V_{DDP}	V
V_{hys}	hysteresis voltage		0.4	–	–	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	–	–	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = –4 mA	V_{DDP} – 0.4	–	V_{DDP}	V
I_{sc}	short-circuit current	note 1	–55	–	+55	mA
I_{pd}	pull-down input current	$V_{DDCO} < V_{IL} < V_{DDP}$	–20	–50	–70	µA
C_I	input capacitance		–	–	10	pF
C_L	load capacitance		–	–	30	pF
Inputs/outputs with I_{max} = 8 mA: pins SD_DQ0 to SD_DQ31; note 2						
V_{IL}	LOW-level input voltage		–0.5	–	+0.7	V
V_{IH}	HIGH-level input voltage		1.7	–	V_{DDP}	V
V_{hys}	hysteresis voltage		0.4	–	–	V
V_{OL}	LOW-level output voltage	I_{OL} = 8 mA	–	–	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = –8 mA	V_{DDP} – 0.4	–	V_{DDP}	V
I_{sc}	short-circuit current	note 1	–55	–	+55	mA
I_{TL}	3-state leakage current	$V_{IH} = V_{DDP}$; $V_{IL} = V_{SSP}$	–5	–	+5	µA
C_I	input capacitance		–	–	10	pF
C_L	load capacitance		–	–	30	pF
3-state output with I_{max} = 4 mA: pins PDO0 to PDO7, PDOAV and PDOSYNC; note 2						
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	–	–	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = –4 mA	V_{DDP} – 0.4	–	V_{DDP}	V
I_{sc}	short-circuit current	note 1	–55	–	+55	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{TL}	3-state leakage current	$V_{IH} = V_{DDP}$; $V_{IL} = V_{SSP}$	–1	–	+1	µA
C_L	load capacitance		–	–	30	pF
3-state output with I_{max} = 4 mA and pull-up resistor: pin PDOVAL; note 2						
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	–	–	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = –4 mA	V_{DDP} – 0.4	–	V_{DDP}	V
I_{sc}	short-circuit current	note 1	–55	–	+55	V
$I_{pu(L)}$	LOW-level pull-up input current	$V_{IL} = V_{SSP}$	–20	–50	–70	µA
$I_{pu(H)}$	HIGH-level pull-up input current	$V_{DDCO} < V_{IH} < V_{DDP}$	–	0	10	µA
C_L	load capacitance		–	–	30	pF
Output with I_{max} = 4 mA: pins ACLK, CLKOUT, $\overline{\text{RTS}}$, SM_A0 to SM_A17, $\overline{\text{SM\_CS3}}$, $\overline{\text{SM\_OE}}$, $\overline{\text{SM\_WE}}$, TDO and TXD						
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	–	–	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = –4 mA	V_{DDP} – 0.4	–	V_{DDP}	V
I_{sc}	short-circuit current	note 1	–55	–	+55	mA
I_{TL}	3-state leakage current	$V_{IH} = V_{DDP}$; $V_{IL} = V_{SSP}$	–1	–	+1	µA
C_L	load capacitance		–	–	30	pF
Output with I_{max} = 8 mA: pins SD_A0 to SD_A13, $\overline{\text{SD\_CAS}}$, SD_CKE, SD_CLK, $\overline{\text{SD\_CS}}$, SD_DQM0 to SD_DQM3, $\overline{\text{SD\_RAS}}$ and $\overline{\text{SD\_WE}}$						
V_{OL}	LOW-level output voltage	I_{OL} = 8 mA	–	–	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = –8 mA	V_{DDP} – 0.4	–	V_{DDP}	V
I_{sc}	short-circuit current	note 1	–125	–	+125	mA
C_L	load capacitance		–	–	30	pF
I^2C-bus interface: pins SCL and SDA; notes 3 and 4						
f_{SCL}	SCL clock frequency		100	–	400	kHz
V_{IL}	LOW-level input voltage		–	–	$0.3V_{DDP}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDP}$	–	3.6	V
V_{hys}	hysteresis voltage		–	$0.05V_{DDP}$	–	V
I_I	input current		–10	–	+10	µA
V_{OL}	LOW-level output voltage; open-drain	3 mA sink current	0	–	0.4	V
t_{LOW}	SCL LOW time		1.3	–	–	µs
t_{HIGH}	SCL HIGH time		0.6	–	–	µs
$t_{r(I2C)}$	rise time of both SDA and SCL		–	–	0.3	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{f(I2C)}$	fall time of both SDA and SCL		–	–	0.3	µs
$t_{SU;DAT}$	data set-up time		100	–	–	ns
$t_{HD;STA}$	hold time START condition		0.6	–	–	µs
$t_{SU;STO}$	set-up time STOP condition		0.6	–	–	µs
Video clock input timing: pins VCLK1 and VCLK2; see Fig.15						
T_{cy}	cycle time		35	37	39	ns
δ	duty factor	t_{HIGH}/T_{cy}	40	50	60	%
$t_{r(VCLK)}$	rise time	V_I = 0.8 to 2 V	–	–	5	ns
$t_{f(VCLK)}$	fall time	V_I = 2 to 0.8 V	–	–	6	ns
Video input data and control timing: pins YUV7 to YUV0, FID, HSYNC and VSYNC; see Fig.15						
$t_{SU;DAT}$	data set-up time		6	–	–	ns
$t_{HD;DAT}$	data hold time		3	–	–	ns
Video input parameter range						
$f_{i(D)}$	data input frequency rate	frame-locked; notes 5 and 6	25.46	27	28.54	MHz
f_H	line frequency	625 lines; note 6	14734	15625	16515	kHz
		525 lines; note 6	14837	15734	16631	kHz
f_V	field frequency	625 lines; notes 7 and 8	46	50	50.75	kHz
		525 lines; notes 7 and 8	55	60	60.9	kHz
$N_{al/f}$	active lines/field	625 lines; notes 7 and 9	265	288	311	
		525 lines; notes 7 and 9	221	240	259	
Crystal oscillator: pins XTALI and XTALO; note 10						
f_{XTAL}	fundamental frequency	note 11	$27 \times (1 - 80 \times 10^{-6})$	27	$27 \times (1 + 80 \times 10^{-6})$	MHz
f_{stab}	MPEG2 frequency stability	note 11	$27 \times (1 - 30 \times 10^{-6})$	–	$27 \times (1 + 30 \times 10^{-6})$	MHz
C_L	load capacitance		8	10	12	pF
V_{IL}	LOW-level input voltage	if used with external clock	–0.5	–	+0.7	V
V_{IH}	HIGH-level input voltage	if used with external clock	1.7	–	V_{DDA}	V
C_{shunt}	shunt capacitance		–	–	7	pF
R_S	serial resistance		–	–	25	Ω

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Crystal oscillator tuning: pins XTALI and XTALO; note 10						
N_{tune}	tuning steps		–127	–	+128	
$C_{tune(min)}$	minimum internal tuning capacitance to V_{SSA}	N_{tune} = 128	–	8	–	pF
$C_{tune(max)}$	maximum internal tuning capacitance	N_{tune} = –127	–	72	–	pF
f_{step}	crystal frequency offset per tuning step		14	42	70	Hz
External clock input: pin EXTCLK						
f_{EXTCLK}	external frequency	square wave; note 11	25.7	27.0	28.3	MHz
δ	duty factor	t_{HIGH}/T_{cy}	40	50	60	%
$t_{r(EXTCLK)}$	rise time	V_I = 0.7 to 1.7 V	–	–	5	ns
$t_{f(EXTCLK)}$	fall time	V_I = 1.7 to 0.7 V	–	–	6	ns
I²C-bus address select input: pin I2CADDRSEL						
V_{IL}	LOW-level input voltage for I²C-bus addresses 40H and 41H		–0.5	–	+0.7	V
V_{IH}	HIGH-level input voltage for I²C-bus addresses 42H and 43H		1.7	–	V_{DDP}	V
Reset input: pin $\overline{\text{RESET}}$						
V_{IL}	LOW-level input voltage for active reset		–0.5	–	+0.7	V
t_{start}	start time of first reset pulse after power-on		–	0	10	µs
t_{length}	length of reset pulse after power-on and after sleep		10	–	–	ms
t_{init}	initialization phase after reset pulse until I²C-bus commands are accepted		–	–	1	s
SDRAM interface data, address and control timing: pins SD_DQ31 to SD_DQ0, SD_A13 to SD_A0, $\overline{\text{SD\_CAS}}$, $\overline{\text{SD\_RAS}}$, $\overline{\text{SD\_WE}}$ and $\overline{\text{SD\_OE}}$						
T_{cy}	cycle time	f_{sys} = 27 MHz	–	9.26	–	ns
t_{CAS}	CAS latency time		–	3	–	clock cycles
t_{RCD}	row to column delay time		–	$3T_{cy}$	–	ns
t_{RRD}	activate to activate delay time		–	$2T_{cy}$	–	ns
t_{RP}	row precharge time		–	$3T_{cy}$	–	ns
t_{WR}	write recovery time		–	$2T_{cy}$	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{RSC}	mode register set cycle time		–	$2T_{cy}$	–	ns
t_{RAS}	row activate time		–	$6T_{cy}$	–	ns
t_{RC}	row cycle time		–	$8T_{cy}$	–	ns
$t_{power-up}$	wait time after power-on		500	515	–	µs
Data output interface timing: pins PDO7 to PDO0, PDIDS, PDOSYNC, PDOAV and PDIOCLK						
$t_{l-o(PDIDS-PDOVAL)}$	PDIDS to PDOVAL low-ohmic time	DEBI slave mode	0	–	20	ns
$t_{l-o(PDIDS-PDO)}$	PDIDS to PDO[7:0] low-ohmic time	DEBI slave mode	0	–	20	ns
$t_{stab(PDO-PDOVAL)}$	PDO[7:0] data stable to falling PDOVAL time	DEBI slave mode	10	–	–	ns
$t_{r(PDOVAL-PDO)}$	rising PDOVAL to PDO[7:0] high-impedance time	DEBI slave mode	10	–	–	ns
$t_{h(PDO-PDIOCLK)}$	PDO[7:0] data to PDIOCLK hold time	DIO master mode; PDOVAL = 1	10	–	–	ns
$t_{su(PDO-PDIOCLK)}$	PDO[7:0] data to PDIOCLK set-up time	DIO master mode; PDOVAL = 1	10	–	–	ns
$t_{i(PDIOCLK)H}$	input PDIOCLK HIGH time	DIO slave mode	55	–	–	ns
$t_{i(PDIOCLK)L}$	input PDIOCLK LOW time	DIO slave mode	55	–	–	ns
$t_{stab(PDIOCLK-PDO)}$	falling input PDIOCLK to PDO[7:0] data stable time	DIO slave mode; PDOVAL = 1	36	–	58	ns

Notes

1. Short-circuit current is only allowed for a short time (<1 s).
2. The output pins are 3.3 V tolerant when in 3-state mode.
3. Pins SCL and SDA of the I^2C-bus interface do not obstruct the SDA and SCL lines if the supply voltage V_{DDP} is switched off.
4. The open-drain outputs are 3.3 V tolerant.
5. Frame-locked input data rate deviation from SAA6752HS crystal clock.
6. Supporting output range of the Philips SAA7114 video input processor.
7. Applies for line frequencies ±2% from nominal.
8. Minimum limit according to IEC 60756; maximum limit because the SAA6752HS may drop frames for V-sync frequencies greater than 1.5% above nominal.
9. Deviation according to IEC 60756.7. The SAA6752HS will only encode 240 lines (when in 525-line mode) and 288 lines (when in 625-line mode). Therefore any additional lines in a field above these values will not be encoded.
10. Pin XTALO has to be used for connection with a crystal only. Do not use for other purposes.
11. The required stability of the crystal frequency or external system clock is dependent upon the clock mode used in the application.

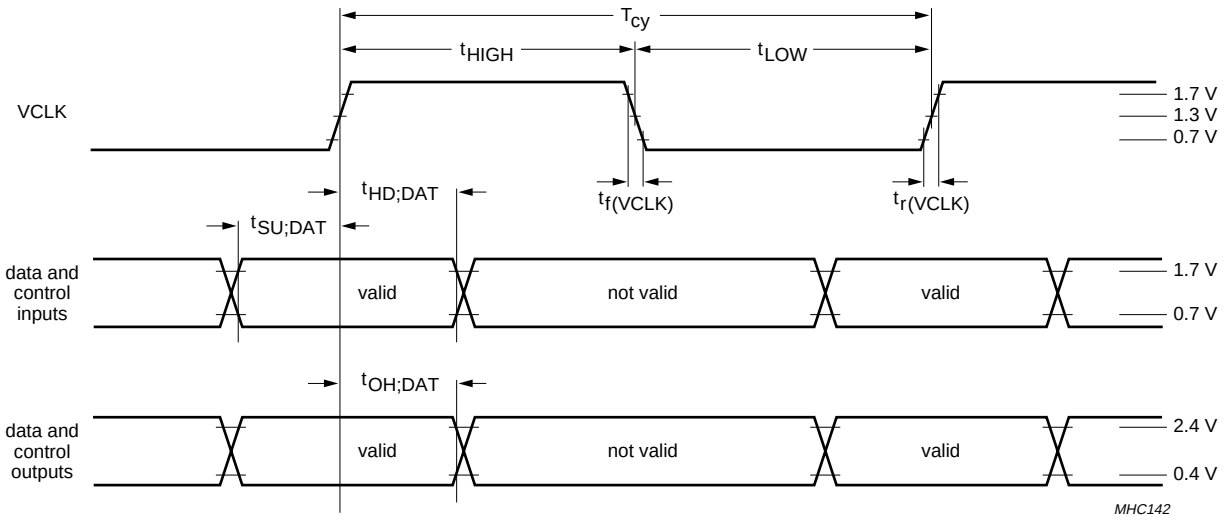
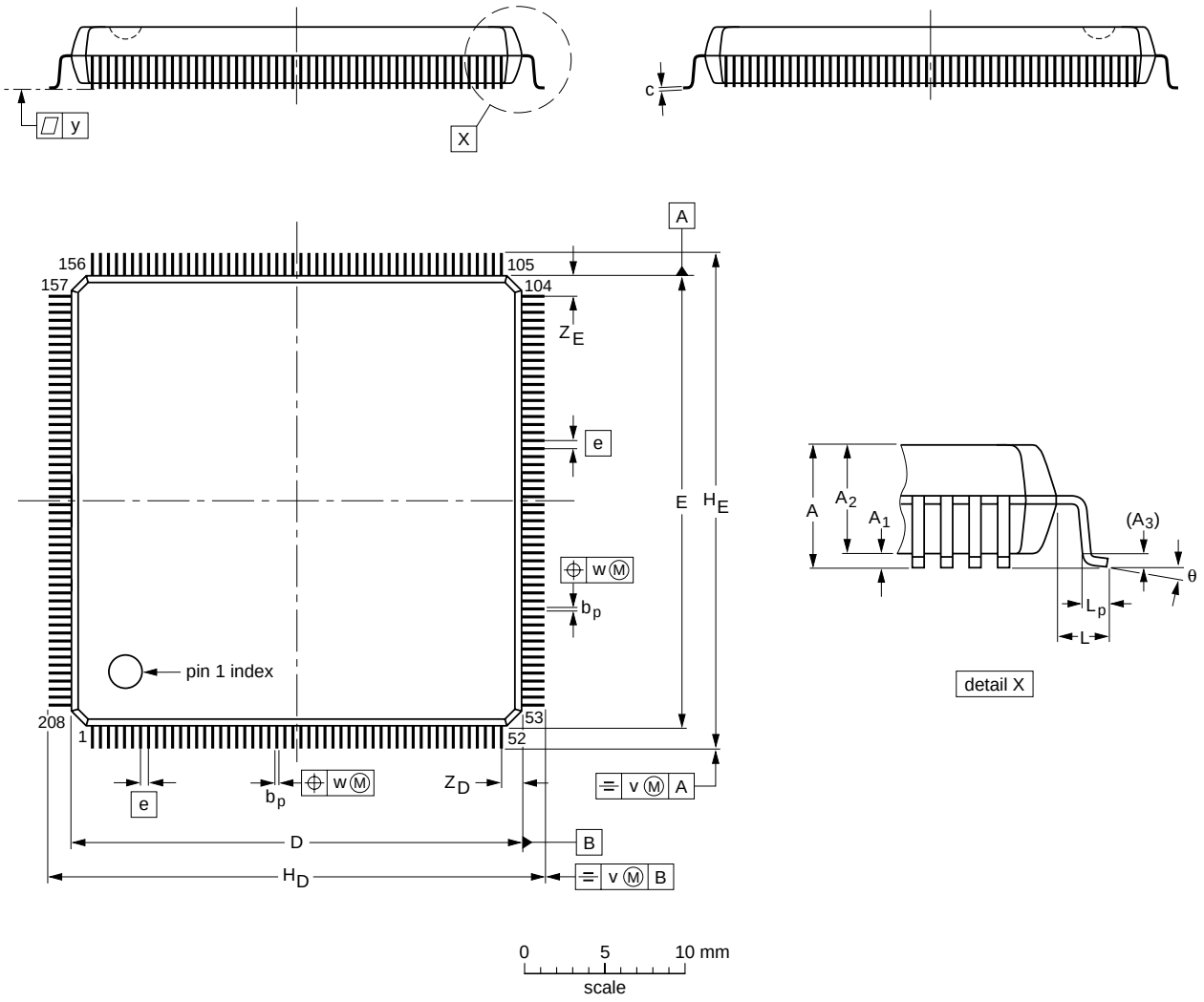


Fig.15 Clock data timing.

13 PACKAGE OUTLINE

SQFP208: plastic shrink quad flat package;
208 leads (lead length 1.3 mm); body 28 x 28 x 3.4 mm; high stand-off height **SOT316-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	4.10	0.50 0.25	3.6 3.2	0.25	0.27 0.17	0.20 0.09	28.1 27.9	28.1 27.9	0.5	30.9 30.3	30.9 30.3	1.3	0.75 0.45	0.2	0.08	0.08	1.39 1.11	1.39 1.11	8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT316-1		MS-029				~~99-12-27~~ 00-01-25

14 SOLDERING

14.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

14.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

14.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

14.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW[1]
BGA, HBGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	not suitable[2]	suitable
PLCC[3], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[3][4]	suitable
SSOP, TSSOP, VSO	not recommended[5]	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

15 DATA SHEET STATUS

DATA SHEET STATUS[1]	PRODUCT STATUS[2]	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

NOTES

NOTES

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