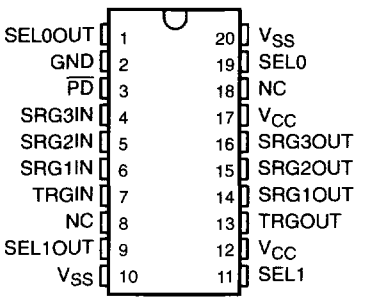
SOCS024B – FEBRUARY 1991

- **TTL-Compatible Inputs**
- **CCD-Compatible Outputs**
- **Full-Frame Operation**
- **Frame-Transfer Operation**
- **Solid-State Reliability**
- **Adjustable Clock Levels**

DW PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN28846 serial driver is a monolithic CMOS integrated circuit designed to drive the serial register gate (SRGn) and transfer gate (TRG) inputs of the Texas Instruments virtual-phase CCD image sensors. The SN28846 interfaces a user-defined timing generator to the CCD image sensor; it receives TTL signals from the timing generator and outputs level-shifted signals to the image sensor. The SN28846 contains three noninverting serial-gate drivers and one noninverting transfer-gate driver.

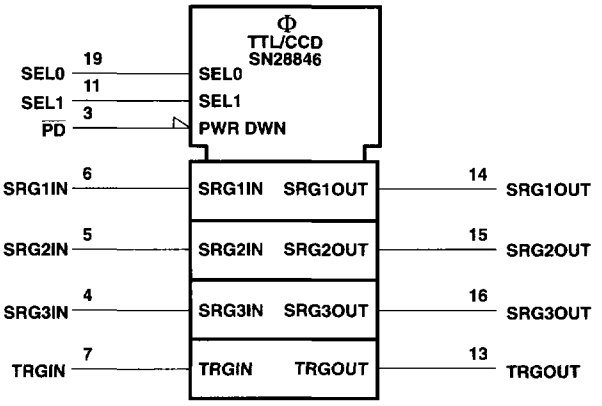
The voltage levels on outputs SRG1OUT, SRG2OUT, SRG3OUT, and TRGOUT are controlled by the levels on the two dc supply inputs V_{SS} and V_{CC}. The propagation delays for these outputs are controlled by the SEL0 and SEL1 inputs. The inputs $\overline{PD}$, SRG1IN, SRG2IN, SRG3IN, and TRGIN are TTL compatible.

A high level on the $\overline{PD}$ input allows the SN28846 to operate normally with the level-shifted outputs following the inputs. When $\overline{PD}$ is low, the device is in a low-power-consumption mode and all outputs are at V_{CC}.

The SN28846 is available in the DW surface-mount package and is characterized for operation from –20°C to 45°C.

This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, precautions should be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriated logic voltage level, preferably either V_{CC} or ground. Specific guidelines for handling devices of this type are contained in the publication *Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies* available from Texas Instruments.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
GND	2		Ground
NC‡	8		No connect
NC‡	18		No connect
$\overline{PD}$	3	I	Power down
SEL0	19	I	Propagation delay mode select
SEL1	11	I	Propagation delay mode select
SEL0OUT	1	O	Test pin (factory use only)
SEL1OUT	9	O	Test pin (factory use only)
SRG1IN	6	I	Serial-register gate 1 in
SRG2IN	5	I	Serial-register gate 2 in
SRG3IN	4	I	Serial-register gate 3 in
SRG1OUT	14	O	Serial-register gate 1 out
SRG2OUT	15	O	Serial-register gate 2 out
SRG3OUT	16	O	Serial-register gate 3 out
TRGIN	7	I	Transfer gate in
TRGOUT	13	O	Transfer gate out
V_{CC}‡	12	I	Positive supply voltage
V_{CC}‡	17	I	Positive supply voltage
V_{SS}‡	10	I	Negative supply voltage
V_{SS}‡	20	I	Negative supply voltage

‡ All pins of the same name should be connected together externally.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Positive supply voltage, V_{CC} (see Note 1) ..... 4 V
Negative supply voltage, V_{SS} (see Note 2) ..... –11.1 V
Input voltage range: SEL0 and SEL1 ..... V_{SS} to V_{CC}
Other inputs ..... 0 to 5.5 V
Operating free-air temperature range, T_A ..... –30°C to 75°C
Storage temperature range ..... –55°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C
Continuous total power dissipation, $T_A \leq 25°C$: Without heat sink (see Figure 1) DW package ... 825 mW
With heat sink (see Figure 1) DW package ..... 1150 mW

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the GND terminal.
2. The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for voltage levels only.

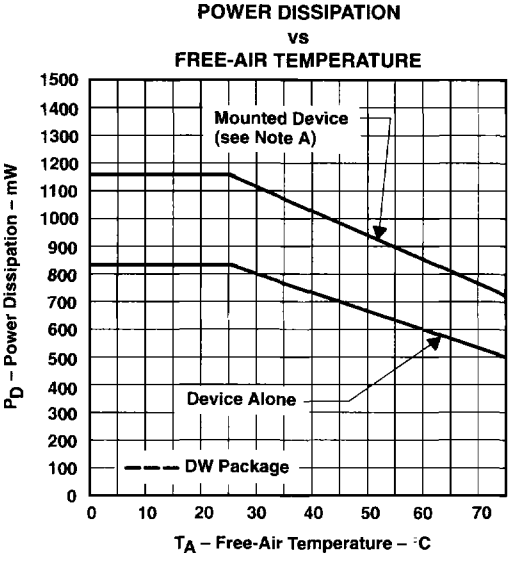


Figure 1

NOTE A: The mounted-device derating curve of Figure 1 was obtained under the following conditions:
The board was 50 mm by 50 mm by 1.6 mm thick.
The board material was glass epoxy.
The copper thickness of all the etch runs was 35 microns.
Etch run dimensions – DW package – All 20 etch runs were 0.4 mm by 22 mm.
Each chip was soldered to the board.
An aluminum cooling fin 10 mm by 10 mm by 1 mm thick was coupled to the chip with thermal paste.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Positive supply voltage, V_{CC}		0	1.5	3	V
Negative supply voltage, V_{SS} (see Note 2)		–11.1	–10.4	–9.7	V
High-level input voltage, V_{IH}	SRG1IN, SRG2IN, SRG3IN, TRGIN	2	5		V
	SEL0, SEL1		V_{CC}		
	$\overline{PD}$	4	5		
Low-level input voltage, V_{IL}	SRG1IN, SRG2IN, SRG3IN, TRGIN		0	0.8	V
	SEL0, SEL1		V_{SS}		
	$\overline{PD}$		0	0.4	
Output load	SRG1OUT, SRG2OUT, SRG3OUT			200	pF
	TRGOUT			350	
Operating free-air temperature, T_A		–20		45	°C

NOTE 2: The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	SRG1OUT, SRG2OUT, SRG3OUT	f = 4.8 MHz, Input t_w = 70 ns, See Figure 1	V_{CC} – 0.5	V_{CC}+0.5	V
		TRGOUT	f = 3.6 MHz, Input t_w = 140 ns, See Figure 1			
V_{OL}	Low-level output voltage	SRG1OUT, SRG2OUT, SRG3OUT	f = 4.8 MHz, Input t_w = 70 ns, See Figure 1	V_{SS}–0.8	V_{SS}+0.8	V
		TRGOUT	f = 3.6 MHz, Input t_w = 140 ns, See Figure 1			
V_n	Peak-to-peak output noise voltage	SRG1OUT, SRG2OUT, SRG3OUT	See Figure 1		300	mV
I_{IH}	High-level input current	SRG1IN, SRG2IN, SRG3IN, TRGIN, SEL0, SEL1	V_I = 5.5 V		50	µA
I_{IL}	Low-level input current		V_I = 0		± 10	µA
I_{SS}	Supply current		No load, $\overline{PD}$ at 0 V, T_A = 25°C		–0.5	mA
			See Note 3		–25	
f_{max}	Maximum frequency of operation	SRG1OUT, SRG2OUT, SRG3OUT	C_L = 200 pF	10		MHz
		TRGOUT	C_L = 350 pF	1		

NOTE 3: SRG1OUT, SRG2OUT, and SRG3OUT are loaded with 80-pF capacitive loads; TRGOUT is loaded with a 180-pF load. The SN28846 driver is clocked by the SN28835 timer. SEL0 and SEL1 are both held at –11.1 V.

switching characteristics for SRG1OUT, SRG2OUT, and SRG3OUT, V_{CC} = 2.3 V, V_{SS} = −10.3 V, T_A = 25°C (unless otherwise noted) (see Figure 1)†

PARAMETER		SELECT MODE‡	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	0	Input t_w = 70 ns, f = 4.8 MHz		28		ns
		1			36		
		2			42		
		3			48		
t_{PHL}	Propagation delay time, high-to-low-level output	0	Input t_w = 70 ns, f = 4.8 MHz		25		ns
		1			24		
		2			23		
		3			23		
Δt_{PLH}	(see Note 4)	Any	T_A = −20°C to 55°C			±5	ns
Δt_{PHL}	(see Note 4)					±5	
$t_{sk(o)}$	Skew time (see Note 5)					5	
						5	
t_w	Pulse duration	0	Input t_w = 70 ns, f = 4.8 MHz	63	68	73	ns
		1		54	59	64	
		2		47	52	57	
		3		40	45	50	
$\lvert t_{w(n)} - t_{w(m)} \rvert$	Pulse duration differential (see Note 6)	Any	Input t_w = 70 ns, f = 4.8 MHz			5	ns
t_r	Rise time	Any	Input t_w = 70 ns, f = 4.8 MHz	10	14	18	ns
t_f	Fall time			6	10	13	

† The load is a Texas Instruments CCD image sensor.

‡ The select mode is determined by the voltage levels applied to the SEL1 and SEL0 inputs as follows:

SELECT MODE	SEL1	SEL0
0	V_{SS}	V_{SS}
1	V_{SS}	V_{CC}
2	V_{CC}	V_{SS}
3	V_{CC}	V_{CC}

NOTES: 4. For a given channel, Δt_{PLH} and Δt_{PHL} are the changes in t_{PLH} and t_{PHL}, respectively, when the device is operated over the temperature range −20°C to 55°C rather than at 25°C.

5. This is the maximum absolute difference in propagation delay time, either t_{PLH} or t_{PHL}, through the three channels at any given temperature within the specified range.

6. This is the maximum difference in the pulse duration through the three channels.

switching characteristics for TRGOUT, V_{CC} = 2.3 V, V_{SS} = −10.3 V, T_A = 25°C (unless otherwise noted) (see Figure 1)†

PARAMETER		SELECT MODE‡	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	0	t_w = 140 ns, f = 3.6 MHz		24		ns
		1			33		
		2			39		
		3			47		
t_{PHL}	Propagation delay time, high-to-low-level output	0	t_w = 140 ns, f = 3.6 MHz		24		ns
		1			23		
		2			22		
		3			22		
Δt_{PLH}	(see Note 7)	Any	T_A = −20°C to 55°C			20	ns
Δt_{PHL}	(see Note 7)					20	
t_w	Pulse duration	Any	t_w = 140 ns, f = 3.6 MHz	100	140	180	ns
t_r	Rise time				17		
t_f	Fall time				10		

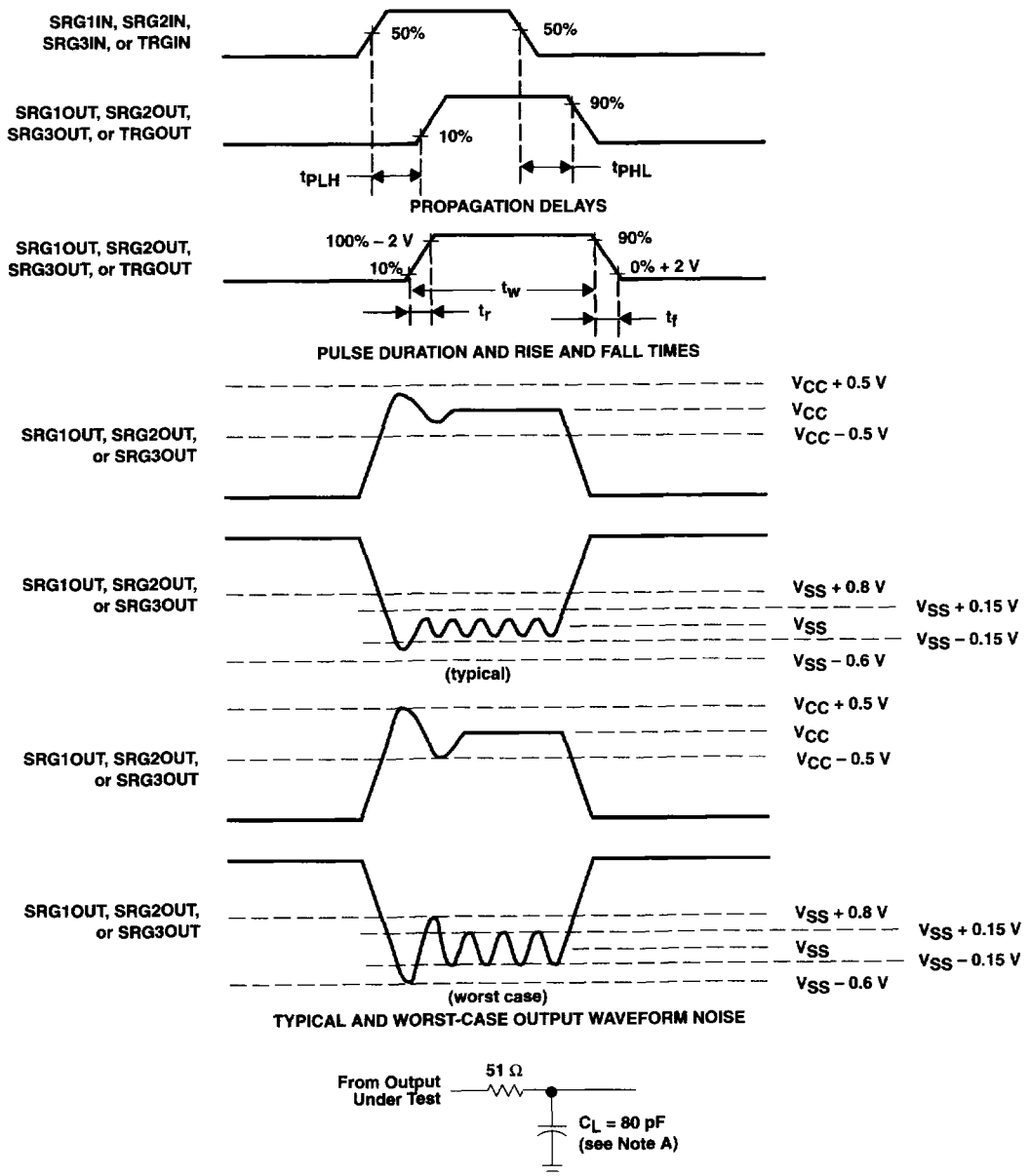
† The load is a Texas Instruments CCD image sensor.

‡ The select mode is determined by the voltage levels applied to SEL1 and SEL0 as follows:

SELECT MODE	SEL1	SEL0
0	V_{SS}	V_{SS}
1	V_{SS}	V_{CC}
2	V_{CC}	V_{SS}
3	V_{CC}	V_{CC}

NOTE 7: Δt_{PLH} and Δt_{PHL} are the changes in t_{PLH} and t_{PHL}, respectively, when the device is operated over the temperature range −20°C to 55°C rather than at 25°C.

PARAMETER MEASUREMENT INFORMATION



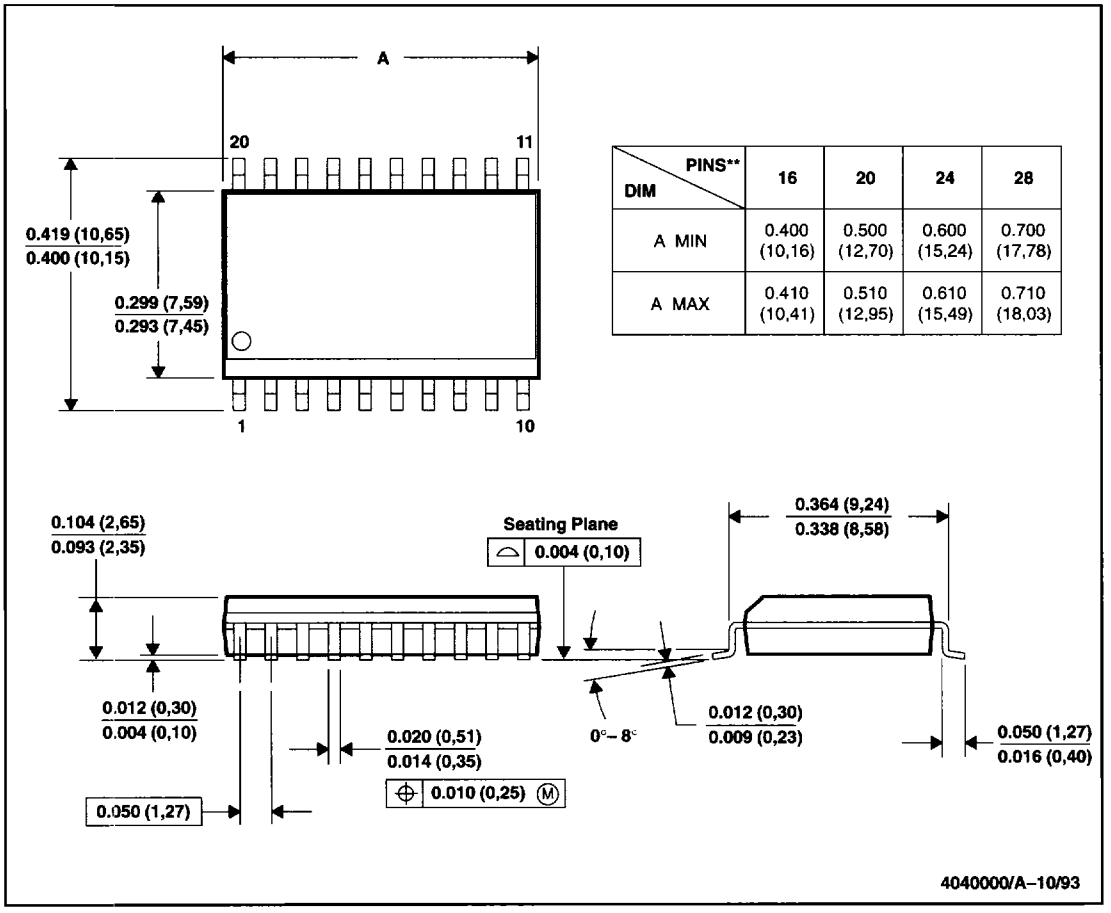
NOTE A: C_L Includes probe and jig capacitance.

Figure 2. Voltage Waveforms

MECHANICAL DATA

DW/R-PDSO-G** **PLASTIC WIDE-BODY SMALL-OUTLINE PACKAGE**

20 PIN SHOWN



DIM \ PINS**	16	20	24	28
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).