

TENTATIVE TOSHIBA HYBRID DIGITAL INTEGRATED CIRCUIT
134,217,728-WORD BY 18-BIT (256M Bytes) Direct Rambus DRAM MODULE

DESCRIPTION

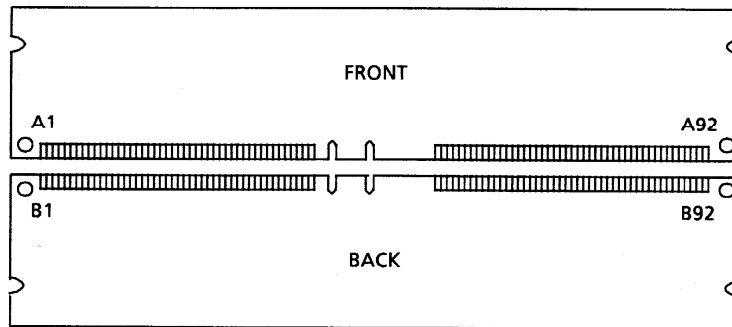
The THMR2E8Z is a 134,217,728-word by 18-bit direct rambus dynamic RAM module consisting of 8 TC59RM818MB Direct Rambus DRAMs on a printed circuit board.

FEATURES

	-6	-7	-8
Organization	128M word×18 bit	128M-word×18 bit	128M-word×18 bit
I/O Frequency	600MHz	711MHz	800MHz
t _{RAC} (Row Access time)	53ns	45ns	45ns
Part Designator	288M (×18) -8CSP	288M (×18) -8CSP	288M (×18) -8CSP

- Power supply of 2.5V (±5%)
- 256MB Direct RDRAM storage
- Each RDRAM has 32 banks for 256 banks total on module
- Separate Row and Column buses for higher efficiency
- Package: 184pin D1MM
- Gold contacts
- Serial Presence Detect suport
- 6 layer PCB

PIN ASSIGNMENT (TOP VIEW)



A1 Gnd	B1 Gnd	A24 LCOL0	B24 LDOB0	A47 NC	B47 NC	A70 Gnd	B70 Gnd
A2 LDOA8	B2 LDOA7	A25 Gnd	B25 Gnd	A48 NC	B48 NC	A71 RCOL2	B71 RCOL1
A3 Gnd	B3 Gnd	A26 LDOB1	B26 LDOB2	A49 NC	B49 NC	A72 Gnd	B72 Gnd
A4 LDOA6	B4 LDOA5	A27 Gnd	B27 Gnd	A50 NC	B50 NC	A73 RCOL4	B73 RCOL3
A5 Gnd	B5 Gnd	A28 LDOB3	B28 LDOB4	A51 Vref	B51 Vref	A74 Gnd	B74 Gnd
A6 LDOA4	B6 LDOA3	A29 Gnd	B29 Gnd	A52 Gnd	B52 Gnd	A75 RROW1	B75 RROW0
A7 Gnd	B7 Gnd	A30 LDOB5	B30 LDOB6	A53 SCL	B53 SA0	A76 Gnd	B76 Gnd
A8 LDOA2	B8 LDOA1	A31 Gnd	B31 Gnd	A54 Vdd	B54 Vdd	A77 NC	B77 RROW2
A9 Gnd	B9 Gnd	A32 LDOB7	B32 LDOB8	A55 SDA	B55 SA1	A78 Gnd	B78 Gnd
A10 LDOA0	B10 LCFM	A33 Gnd	B33 Gnd	A56 SVdd	B56 SVdd	A79 RCTM	B79 NC
A11 Gnd	B11 Gnd	A34 LSCK	B34 LCMD	A57 SWP	B57 SA2	A80 Gnd	B80 Gnd
A12 LCTMN	B12 LCFMN	A35 Vcmos	B35 Vcmos	A58 Vdd	B58 Vdd	A81 RCTMN	B81 RCFMN
A13 Gnd	B13 Gnd	A36 SOUT	B36 SIN	A59 RSCK	B59 RCMD	A82 Gnd	B82 Gnd
A14 LCTM	B14 NC	A37 Vcmos	B37 Vcmos	A60 Gnd	B60 Gnd	A83 RDOA0	B83 RCFM
A15 Gnd	B15 Gnd	A38 NC	B38 NC	A61 RDQB7	B61 RDQB8	A84 Gnd	B84 Gnd
A16 NC	B16 LROW2	A39 Gnd	B39 Gnd	A62 Gnd	B62 Gnd	A85 RDOA2	B85 RDOA1
A17 Gnd	B17 Gnd	A40 NC	B40 NC	A63 RDQB5	B63 RDQB6	A86 Gnd	B86 Gnd
A18 LROW1	B18 LROW0	A41 Vdd	B41 Vdd	A64 Gnd	B64 Gnd	A87 RDOA4	B87 RDOA3
A19 Gnd	B19 Gnd	A42 Vdd	B42 Vdd	A65 RDQB3	B65 RDQB4	A88 Gnd	B88 Gnd
A20 LCOL4	B20 LCOL3	A43 NC	B43 NC	A66 Gnd	B66 Gnd	A89 RDOA6	B89 RDOA5
A21 Gnd	B21 Gnd	A44 NC	B44 NC	A67 RDQB1	B67 RDQB2	A90 Gnd	B90 Gnd
A22 LCOL2	B22 LCOL1	A45 NC	B45 NC	A68 Gnd	B68 Gnd	A91 RDOA8	B91 RDOA7
A23 Gnd	B23 Gnd	A46 NC	B46 NC	A69 RCOL0	B69 RDQB0	A92 Gnd	B92 Gnd

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PIN NAMES

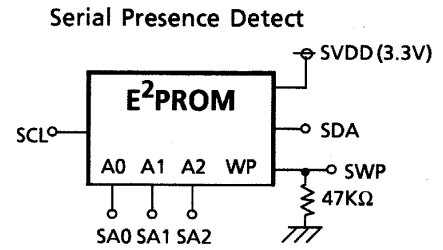
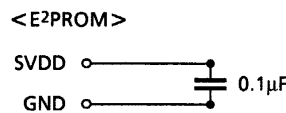
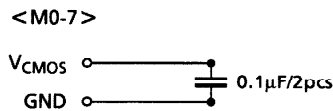
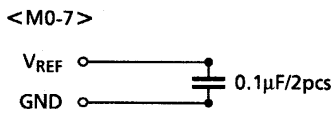
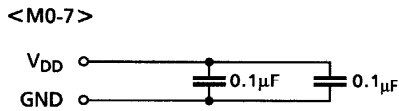
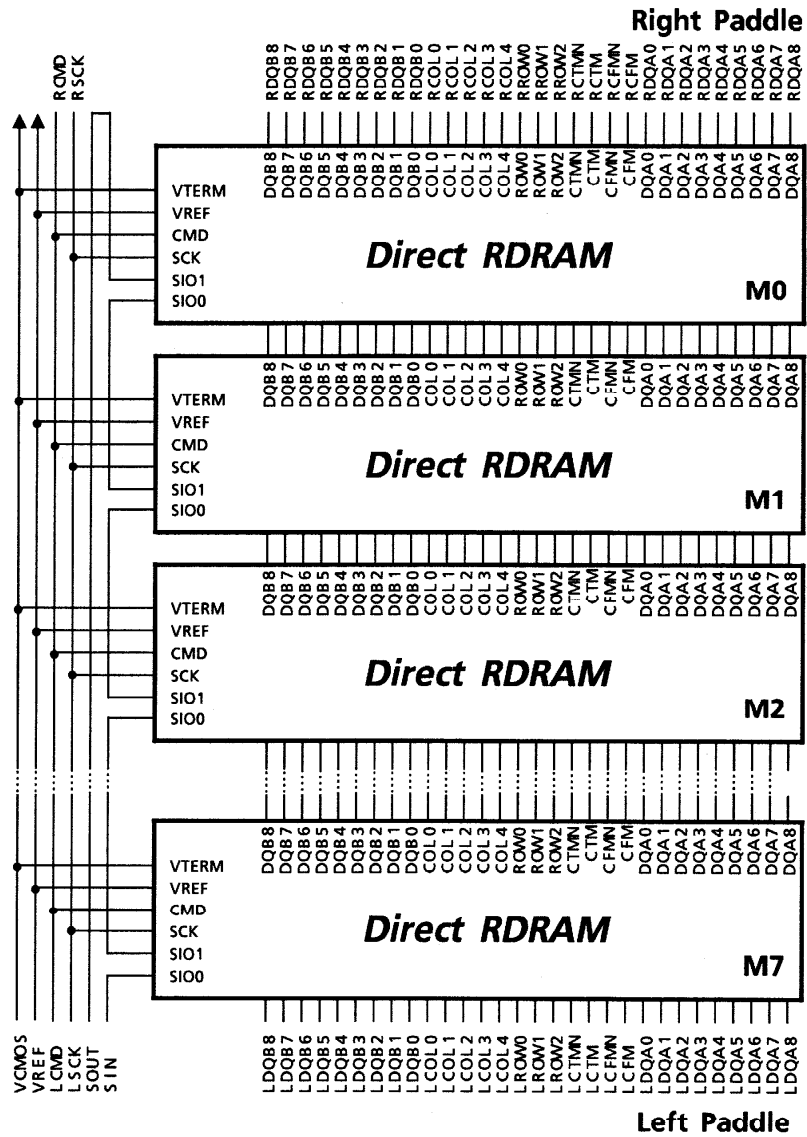
Signal	I/O	Type	Description	Pins
SIN	I/O	CMOS	Serial I/O. Pin for reading from and writing to the control registers.	B36
SOUT	I/O	CMOS	Serial I/O. Pin for reading from and writing to the control registers.	A36
VDD			Supply voltage for the RDRAM core and interface logic.	A41, B41, A42, B42, A54, B54, A58, B58
GND			Ground reference for RDRAM core and interface.	A1, B1, A3, B3, A5, B5, A7, B7, A9, B9, A11, B11, A13, B13, A15, B15, A17, B17, A19, B19, A21, B21, A23, B23, A25, B25, A27, B27, A29, B29, A31, B31, A33, B33, A39, B39, A52, B52, A60, B60, A62, B62, A64, B64, A66, B66, A68, B68, A70, B70, A72, B72, A74, B74, A76, B76, A77, A78, B78, A80, B80, A82, B82, A84, B84, A86, B86, A88, B88, A90, B90, A92, B92
LDQA8 to 0	I/O	RSL	Data bus A. A 9-pin bus carrying a byte of read or write data between the Channel and the RDRAM.	A2, B2, A4, B4, A6, B6, A8, B8, A10
LCFM	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Positive polarity.	B10
LCFMN	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Negative polarity.	B12
	VREF		Logic threshold reference voltage for RSL signals.	A51, B51
LCTMN	I	RSL	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Negative polarity.	A12
LCTM	I	RSL	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Positive polarity.	A14
LROW2 to 0	I	RSL	Row bus. 3-pin bus containing control and address information for row accesses.	B16, A18, B18
LCOL4 to 0	I	RSL	Column bus. 5-pin bus containing control and address information for column accesses.	A20, B20, A22, B22, A24
LDQB8 to 0	I/O	RSL	Data bus B. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM.	B32, A32, B30, A30, B28, A28, B26, A26, B24
LCMD	I	CMOS	Serial Command Pin. Pin used to read from and write to the control registers. Also used for power management.	B34
LSCK	I	CMOS	Clock input. Pin used to read from and write to the control registers.	A34
RDQA8 to 0	I/O	RSL	Data bus A. A 9-pin bus carrying a byte of read or write data between the Channel and the RDRAM.	A91, B91, A89, B89, A87, B87, A85, B85, A83
RCFM	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Positive polarity.	B83
RCFMN	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Negative polarity.	B81
RCTM	I	RSL	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Positive polarity.	A79
RROW2 to 0	I	RSL	Row bus. 3-pin bus containing control and address information for row accesses.	B77, A75, B75
RCOL4 to 0	I	RSL	Column bus. 5-pin bus containing control and address information for column accesses.	A73, B73, A71, B71, A69
RDQB8 to 0	I/O	RSL	Data bus B. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM.	B61, A61, B63, A63, B65, A65, B67, A67, B69
RCMD	I	CMOS	Serial Command Input. Pin used to read from and write to the control registers. Also used for power management.	B59
RSCK	I	CMOS	Clock input. Pin used to read from and write to the control registers.	A59
SCL	I	CMOS	Serial Presence Detect Clock.	A53
SDA	I/O	CMOS	Serial Presence Detect Data (Open Collector I/O).	A55
SA0	I	CMOS	Serial Presence Detect Address 0.	B53
SA1	I	CMOS	Serial Presence Detect Address 1.	B55
SA2	I	CMOS	Serial Presence Detect Address 2.	B57
SWP	I	CMOS		A57
VCMOS			Termination Voltage.	A37, B37, A35, B35
SVDD			Supply voltage for the E ² PROM (SPD).	A56, B56
N.C.				B14, A16, A38, B38, A40, B40, A43, B43, A44, B44, A45, B45, A46, B46, A47, B47, A48, B48, A49, B49, A50, B50, B79,

SERIAL PRESENCE DETECT

Byte Number	Function	THMR2E8Z-6		THMR2E8Z-7		THMR2E8Z-8	
		128Mx18 (256MB + ECC), 600MHz-53ns		128Mx18 (256MB + ECC), 711MHz-45ns		128Mx18 (256MB + ECC), 800MHz-45ns	
		Entry Value	Entry	Entry Value	Entry	Entry Value	Entry
0	SPD revision level	1.0	02 h	1.0	02 h	1.0	02 h
1	Total number of bytes in the SPD	256 bytes	08 h	256 bytes	08 h	256 bytes	08 h
2	Device type	DDRDRAM	01 h	DDRDRAM	01 h	DDRDRAM	01 h
3	Module type	RIMM	01 h	RIMM	01 h	RIMM	01 h
4	Row address bit, Column address bit	9.7	97 h	9.7	97 h	9.7	97 h
5	Bank address bits and byte	32 s	C5 h	32 s	C5 h	32s	C5 h
6	Refresh bank bit	5	05 h	5	05 h	5	05 h
7	tREF-Refresh interval	32	20 h	32	20 h	32	20 h
8	Protocol version	2	02 h	2	02 h	2	02 h
9	Miscellaneous device configuration field (Low Power/no-Low Power)	1.5 tSCK S28IECO	05 h	1.5 tSCK S28IECO	05 h	1.5 tSCK S28IECO	05 h
10	tRP-R, Min	8 Cycle	08 h	8 Cycle	08 h	8 Cycle	08 h
11	tRAS-R, Min	20 Cycle	14 h	20 Cycle	14 h	20 Cycle	14 h
12	tRCD-R, Min	8 Cycle	08 h	8 Cycle	08 h	10 Cycle	0A h
13	tRR-R, Min	8 Cycle	08 h	8 Cycle	08 h	8 Cycle	08 h
14	tPP-R, Min	8 Cycle	08 h	8 Cycle	08 h	8 Cycle	08 h
15	Min tCYCLE for range A	3.33 ns	1A h	2.67 ns	15 h	2.43 ns	13 h
16	Max tCYCLE for range A	3.71 ns	1E h	3.71 ns	1E h	3.71 ns	1E h
17	tCDLY range for A	4 - 9	49 h	5 - 9	59 h	5 - 9	59 h
18	tCLS and tCAS range for A	tCLS = 2, tCAS = 2	AA h	tCLS = 2, tCAS = 2	AA h	tCLS = 2, tCAS = 2	AA h
19	Min tCYCLE for range B	—	00 h	3.33 ns	1A h	3.33 ns	1A h
20	Max tCYCLE for range B	—	00 h	3.71 ns	1E h	3.71 ns	1E h
21	tCDLY range for range B	—	00 h	4 - 9	49 h	4 - 9	49 h
22	tCLS and tCAS range for range B	—	00 h	tCLS = 2, tCAS = 2	AA h	tCLS = 2, tCAS = 2	AA h
23	Min tCYCLE range for C	—	00 h	—	00 h	—	00 h
24	Max tCYCLE for range C	—	00 h	—	00 h	—	00 h
25	tCDLY range for range C	—	00 h	—	00 h	—	00 h
26	tCLS and tCAS range for range C	—	00 h	—	00 h	—	00 h
27	Min tCYCLE for range D	—	00 h	—	00 h	—	00 h
28	Max tCYCLE for range D	—	00 h	—	00 h	—	00 h
29	tCDLY range for range D	—	00 h	—	00 h	—	00 h
30	tCLS and tCAS range for range D	—	00 h	—	00 h	—	00 h
31	tPDNxA, Min	4 us	04 h	4 us	04 h	4 us	04 h
32	tPDNxA, Max	9000 Cycles	8D h	9000 Cycles	8D h	9000 Cycles	8D h
33	tNAPxA, Min	50 ns	32 h	50 ns	32 h	50 ns	32 h
34	tNAPxB, Min	40 ns	28 h	40 ns	28 h	40 ns	28 h
35	fIMIN [11:8], fIMAX [11:8]	261,300MHz	11 h	261,357MHz	11 h	261,400MHz	11 h
36	fIMIN [7:0]	261MHz	05 h	261MHz	05 h	261MHz	05 h
37	fIMAX [7:0]	300MHz	2C h	357MHz	65 h	400MHz	90 h
38	ODF Mapping	12.5%	01 h	12.5%	01 h	12.5%	01 h
39	tCCTRL, MAX	100 ms	64 h	100 ms	64 h	100 ms	64 h
40	tTEMP, MAX	100 ms	64 h	100 ms	64 h	100 ms	64 h
41	tTCEN, MIN	150 tCYCLE	96 h	150 tCYCLE	96 h	150 tCYCLE	96 h
42	tRAS-R, MAX	64 us	40 h	64 us	40 h	64 us	40 h
43	tNLIMIT, MAX	10 us	0A h	10 us	0A h	10 us	0A h
44	ACTREFPT, PCHRERPT	6.6 tCYCLE	66 h	6.6 tCYCLE	66 h	6.6 tCYCLE	66 h
45	CPCHREFPT_DC, RDREFPT_DC	5.5 tCYCLE	55 h	5.5 tCYCLE	55 h	5.5 tCYCLE	55 h
46	RETREFPT_DC, WRREFPT_DC	5.13 tCYCLE	5D h	5.13 tCYCLE	5D h	5.13 tCYCLE	5D h
47-49	Reserved		00 h		00 h		00 h
50	fRAS [11:8]	300MHz	01 h	357MHz	01 h	400MHz	01 h
51	fRAS [7:0]	300MHz	2C h	357MHz	65 h	400MHz	90 h
52	PMAX, HI, PMAX, LO, TJ	0,0,100degC	24 h	0,0,100degC	24 h	0,0,100degC	24 h
53	Heat Spreader, Tplate	1,90degC	9A h	1,90degC	9A h	1,90degC	9A h

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		128Mx18 (256MB + ECC), 600MHz-53ns		128Mx18 (256MB + ECC), 711MHz-45ns		128Mx18 (256MB + ECC), 800MHz-45ns	
		Entry Value	Entry	Entry Value	Entry	Entry Value	Entry
54	PSTBY, HI	90 mA	5A h	95 mA	5F h	105 mA	69 h
55	PACTI, HI	125 mA	3F h	140 mA	46 h	150 mA	4B h
56	PACTRW, HI	510 mA	40 h	580 mA	49 h	635 mA	50 h
57	PSTBY, LO	85 mA	55 h	85 mA	55 h	85 mA	55 h
58	PACTI, LO	115 mA	3A h	115 mA	3A h	115 mA	3A h
59	PACTRW, LO	470 mA	3B h	470 mA	3B h	470 mA	3B h
60	PNAP	4.2 mA	21 h	4.2 mA	21 h	4.2 mA	21 h
61	PRESA		00 h		00 h		00 h
62	PRESB		00 h		00 h		00 h
63	Checksum for location 0-62		90 h		4D h		B9 h
64		TOSHIBA	98 h	TOSHIBA	98 h	TOSHIBA	98 h
65-71			00 h		00 h		00 h
72	Module manufacturing location						
73-90	Module part number						
91-92	Module revision code		00 h		00 h		00 h
93	Module manufacturing year						
94	Module manufacturing week						
95-98	Module serial number						
99	Number of devices on module	8	08 h	8	08 h	8	08 h
100	Module data width	18	12 h	18	12 h	18	12 h
101	Device enables	All 8 device enabled	FF h	All 8 device enabled	FF h	All 8 device enabled	FF h
102			00 h		00 h		00 h
103			00 h		00 h		00 h
104			00 h		00 h		00 h
105	Module Vdd, Module Voltage Interface level	2.5V,1.8V	10 h	2.5V,1.8V	10 h	2.5V,1.8V	10 h
106	Module VDD tolerance	5% DC 2% AC	52 h	5% DC 2% AC	52 h	5% DC 2% AC	52 h
107-113	Reserved		00 h		00 h		00 h
114	CDLY0/1 for tCDLY = 3	-	00 h	-	00 h	-	00 h
115	CDLY0/1 for tCDLY = 4	2/0	20 h	2/0	20 h	2/0	20 h
116	CDLY0/1 for tCDLY = 5	3/0	30 h	3/0	30 h	3/0	30 h
117	CDLY0/1 for tCDLY = 6	3/1	31 h	3/1	31 h	3/1	31 h
118	CDLY0/1 for tCDLY = 7	3/2	32 h	3/2	32 h	3/2	32 h
119	CDLY0/1 for tCDLY = 8	4/2	42 h	4/2	42 h	4/2	42 h
120	CDLY0/1 for tCDLY = 9	5/2	52 h	5/2	52 h	5/2	52 h
121	CDLY0/1 for tCDLY = 10	-	00 h	-	00 h	-	00 h
122	CDLY0/1 for tCDLY = 11	-	00 h	-	00 h	-	00 h
123	CDLY0/1 for tCDLY = 12	-	00 h	-	00 h	-	00 h
124	CDLY0/1 for tCDLY = 13	-	00 h	-	00 h	-	00 h
125	CDLY0/1 for tCDLY = 14	-	00 h	-	00 h	-	00 h
126	CDLY0/1 for tCDLY = 15	-	00 h	-	00 h	-	00 h
127	Checksum for location 99-126		C2 h		C2 h		C2 h

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	MIN	MAX	UNIT
$V_{I,ABS}$	Voltage applied to any RSL pin with respect to Gnd	-0.3	$V_{DD} + 0.3$	V
$V_{I,CMOS,ABS}$	Voltage applied to any CMOS pin with respect to Gnd	-0.3	$V_{DD} + 0.3$	V
$V_{DD,ABS}$	Voltage on VDD with respect to Gnd	-0.5	$V_{DD} + 1.0$	V
T_{STORE}	Storage temperature	-50	100	°C

THERMAL PARAMETERS

SYMBOL	PARAMETER and CONDITIONS	MIN	MAX	UNIT
T_J	Junction operating temperature	TBD	TBD	°C
θ_{JA}	Junction-to-Ambient thermal resistance		TBD	°C/Watt

RIMM MODULE CURRENT PROFILE

IDD	RIMM module power conditions	MAX	UNIT
I_{DD1}	One RDRAM in Read, balance in NAP mode	604	mA
I_{DD2}	One RDRAM in Read, balance in Standby mode	1282	mA
I_{DD3}	One RDRAM in Read, balance in Active mode	1611	mA
I_{DD4}	One RDRAM in Write, balance in NAP mode	664	mA
I_{DD5}	One RDRAM in Write, balance in Standby mode	1342	mA
I_{DD6}	One RDRAM in Write, balance in Active mode	1671	mA

Power does not include Refresh Current.

RECOMMENDED CONDITIONS

SYMBOL	PARAMETER and CONDITIONS	MIN	MAX	UNIT
V_{DD}	Supply Voltage	2.50-0.13	2.50 + 0.13	V
V_{CMOS}	CMOS I/O power supply at pad for 2.5V controllers:	2.5 - 0.13	2.5 + 0.25	V
	CMOS I/O power supply at pad for 1.8V controllers:	1.8 - 0.1	1.8 + 0.2	V
V_T	Termination Voltage	1.80-0.1	1.80 + 0.1	V
V_{REF}	Reference Voltage	1.40-0.2	1.40 + 0.2	V
V_{IL}	RSL input low Voltage	$V_{REF} - 0.5$	$V_{REF} - 0.2$	V
V_{IH}	RSL input high Voltage	$V_{REF} + 0.2$	$V_{REF} + 0.5$	V
$V_{IL,CMOS}$	CMOS input low Voltage	-0.3	$0.5V_{CMOS} - 0.25$	V
$V_{IH,CMOS}$	CMOS input high Voltage	$0.5V_{CMOS} + 0.25$	$V_{CMOS} + 0.3$	V
SV_{DD}	SPD power supply	2.2	3.6	V
VS_{IL}	SPD input low Voltage	-0.3	$SV_{DD} \times 0.3$	V
VS_{IH}	SPD input high Voltage	$SV_{DD} \times 0.7$	$SV_{DD} + 0.3$	V

ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER and CONDITIONS	MIN	MAX	UNIT
I _{REF}	VREF current @ VREF, MAX	-80	80	μA
I _{SCK, CMD}	CMOS input leakage current @ (0 ≤ V _{CMOS} ≤ V _{DD})	-80	80	μA
I _{SIN, SOUT}	CMOS input leakage current @ (0 ≤ V _{CMOS} ≤ V _{DD})	-10	10	μA
V _{OL, CMOS}	CMOS output Voltage @ I _{OL, CMOS} = 1.0mA	-	0.3	V
V _{OH, CMOS}	CMOS output high Voltage @ I _{OH, CMOS} = -0.25mA	V _{CMOS} - 0.3	-	V
V _{SOL}	SPD output low Voltage (I _{SOL} = 3mA)	-	0.4	V

TIMING CHARACTERISTICS

SYMBOL	PARAMETER	MIN	MAX	UNIT
t _Q	CTM-to-DQA/DQB output time @ t _{CYCLE} = 3.33ns	-0.350 ^{a,c}	+0.350 ^{a,c}	ns
	CTM-to-DQA/DQB output time @ t _{CYCLE} = 2.81ns	-0.300 ^{b,c}	+0.300 ^{b,c}	ns
	CTM-to-DQA/DQB output time @ t _{CYCLE} = 2.50ns	-0.260 ^c	+0.260 ^c	ns
t _{QR} , t _{QF}	DQA/DQB output rise and fall times	0.2	0.45	ns
t _{Q1}	SCK(neg)-to-SIO0 delay @ C _{LOAD,MAX} = 20pF (SD read data valid).	-	10	ns
t _{HR}	SCK(pos)-to-SIO0 delay @ C _{LOAD,MAX} = 20pF (SD read data hold).	2	-	ns
t _{QR1} , t _{QF1}	SIO _{OUT} rise/fall @ C _{LOAD,MAX} = 20pF	-	5	ns
t _{PROP1}	SIO0-to-SIO1 or SIO1-to-SIO0 delay @ C _{LOAD,MAX} = 20pF	-	10	ns
t _{NAPXA}	NAP exit delay - phase A	-	50	ns
t _{NAPXB}	NAP exit delay - phase B	-	40	ns
t _{PDNXA}	PDN exit delay - phase A	-	4	μs
t _{PDNXB}	PDN exit delay - phase B	-	9000	t _{CYCLE}
t _{AS}	ATTN-to-STBY power state delay	-	1	t _{CYCLE}
t _{SA}	STBY-to-ATTN power state delay	-	0	t _{CYCLE}
t _{ASN}	ATTN/STBY-to-NAP power state delay	-	8	t _{CYCLE}
t _{ASP}	ATTN/STBY-to-PDN power state delay	-	8	t _{CYCLE}

- a. This parameter also applies to a -800 or -711 part when operated with t_{CYCLE} = 3.33ns.
- b. This parameter also applies to a -800 part when operated with t_{CYCLE} = 2.81ns.
- c. t_{Q,MIN} and t_{Q,MAX} for other t_{CYCLE} values can be interpolated between or extrapolated from the timings at the 3 specified t_{CYCLE} values.

RECOMMENDED TIMING CONDITIONS

SYMBOL	PARAMETER	MIN	MAX	UNIT	
t _{CR} , t _{CF}	CTM and CFM input rise and fall times	0.2	0.5	ns	
t _{CYCLE}	CTM and CFM cycle times	600	3.33	3.83	ns
		711	2.80	3.83	ns
		800	2.50	3.83	ns
t _{CH} , t _{CL}	CTM and CFM high and low times	40%	60%	t _{CYCLE}	
t _{TR}	CTM-CFM differential	MSE/MS = 0/0	0.0	1.0	t _{CYCLE}
		MSE/MS = 1/1	0.9	1.0	t _{CYCLE}
t _{DR} , t _{DF}	DQA/DQB/ROW/COL input rese/fall times	0.2	0.65	ns	
t _S , t _H	DQA/DQB/ROW/COL-to-CFM set/hold @ t _{CYCLE} = 3.33ns	0.275	-	ns	
	DQA/DQB/ROW/COL-to-CFM set/hold @ t _{CYCLE} = 2.81ns	0.240	-	ns	
	DQA/DQB/ROW/COL-to-CFM set/hold @ t _{CYCLE} = 2.50ns	0.200	-	ns	
t _{DR1} , t _{DF1}	SIO _{IN} ^a , CMD, SCK input rise and fall times	-	5.0	ns	
t _{CYCLE1}	SCK cycle time-Serial control register transactions	1000	-	ns	
	SCK cycle time-Power transitions	10	-	ns	
t _{CH1} , t _{CL1}	SCK high and low times	4.25	-	ns	
t _{S1}	CMD setup time	1.25	-	ns	
t _{H1}	CMD hold time	1	-	ns	
t _{S2}	SIO _{IN} setup time	40	-	ns	
t _{H2}	SIO _{IN} hold time	40	-	ns	
t _{S3}	PDEV setup time on DQA5..0	0	-	ns	
t _{H3}	PDEV hold time on DQA5..0	5.5	-	ns	
t _{S4}	ROW2..0, COL4..0 setup time for quiet window	-1	-	t _{CYCLE}	
t _{H4}	ROW2..0, COL4..0 hold time for quiet window	5	-	t _{CYCLE}	
t _{CE}	CTM/CFM stable before NAP/PDN exit	2	-	t _{CYCLE}	
t _{CD}	CTM/CFM stable after NAP/PDN entry	100	-	t _{CYCLE}	
t _{FRM}	ROW packet to COL packet ATTN framing delay	7	-	t _{CYCLE}	
t _{NLIMIT}	Maximum time in NAP mode		10.0	μs	
t _{REF}	Refresh interval		32	ms	
t _{RAS}	RAS interval (time a row may stay activated)		64 ^b	μs	
t _{PAUSE}	RDRAM substrate bias generator delay		200.0	μs	

a. SIO_{IN} refers to the SIO0 or SIO1 pin when used as an input.

b. This is constraint imposed by the core, and is therefore in units of μs rather than t_{CYCLE}.

RECOMMENDED TIMING CONDITIONS

SYMBOL	PARAMETER	MIN- -6	MIN- -7	MIN- -8			MAX	UNIT
t _{RC}	Row Cycle time of RDRAM banks-the interval between ROWA packets with ACT commands to the same bank.	28	28	28			-	t _{CYCLE}
t _{RAS}	RAS-asserted time of RDRAM bank-the interval between ROWA packet with ACT command and next ROWR packet with PRER command to the same bank.	20	20	20			-	t _{CYCLE}
t _{RP}	Row Precharge time of RDRAM banks-the interval between ROWR packet with PRER command and next ROWA packet with ACT command to the same bank.	8	8	8			-	t _{CYCLE}
t _{PP}	Precharge-to-precharge time of RDRAM device-the interval between successive ROWR packets with PRER commands to different banks of the same device.	8	8	8			-	t _{CYCLE}
t _{RR}	RAS-to-RAS time of RDRAM device-the interval between successive ROWA packets with ACT commands to different banks of the same device.	8	8	8			-	t _{CYCLE}
t _{RCD}	RAS-to-CAS Delay-the interval from ROWA packet with ACT command to COLC packet with RD or WR command). Note-the RAS-to-CAS delay seen by the RDRAM core (t _{RCD, CORE}) is equal to t _{RCD, CORE} = 1 + t _{RCD} because of differences in the row and column paths through the RDRAM interface.	7	7	9			-	t _{CYCLE}
t _{RAC}	RAS Access delay-effective interval from ROWA packet with ACT command to Q read data. This is equal to : t _{RAC} = 1 + t _{RCD} + t _{CAC} .	16	16	18			-	t _{CYCLE}
t _{CAC}	CAS Access delay-the minimum interval from RD command to Q read data.	8	8	8			12	t _{CYCLE}
t _{CWD}	CAS Write Delay (interval from WR command to D write data.	6	6	6			6	t _{CYCLE}
t _{CC}	CAS-to-CAS time of RDRAM bank-the interval between successive COLC commands.	4	4	4			-	t _{CYCLE}
t _{PACKET}	Length of ROWA, ROWR, COLC, COLM or COLX packet.	4	4	4			4	t _{CYCLE}
t _{TR}	Interval from COLC packet with WR command to COLC packet which causes retire. and to optional COLM packet with bytemask.	8	8	8				t _{CYCLE}
t _{OFFP}	Interval from last COLC packet with RD or automatic retire command to ROWR packet with PRER. Also, the interval (offset) from COLC packet with RDA command, or from COLC packet with retire command(after WRA automatic precharge), or from COLX packet with PREX command to the equivalent ROWR packet with PRER.	4	4	4				t _{CYCLE}

RSL CLOCKING AND BIT TRANSPORT

Figure 2 shows the timing required to receive or transmit a pair of RSL bits. A single clock cycle T_2 from the central figure is expanded to show the details associated with a falling edge and rising edge of the CFM and CTM clock inputs (the CFMN and CTMN inputs will always be at the opposite signal level). Note that RSL signals are low-true; a high voltage is logic zero.

Figure 2a shows the rise/fall requirements of RSL input signals, and the rise/fall characteristics of RSL output signals.

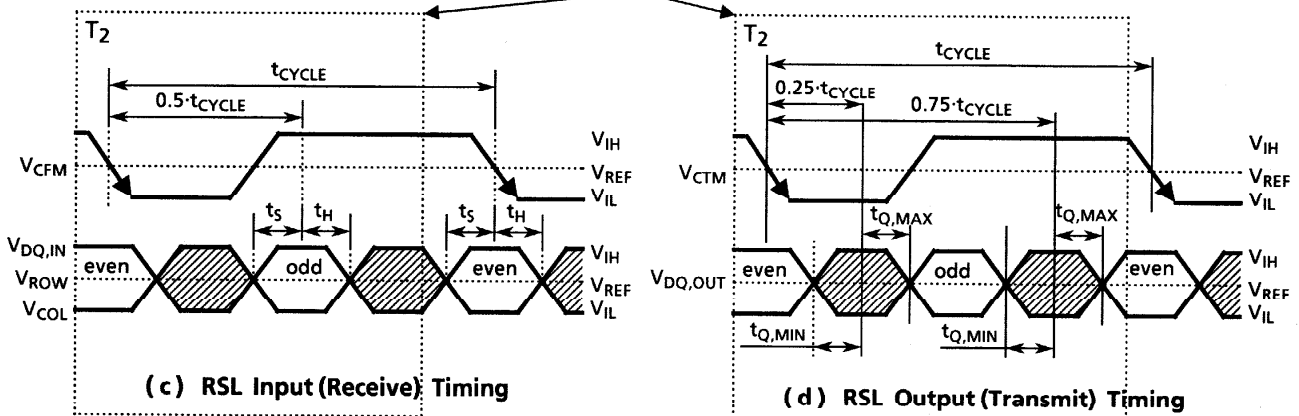
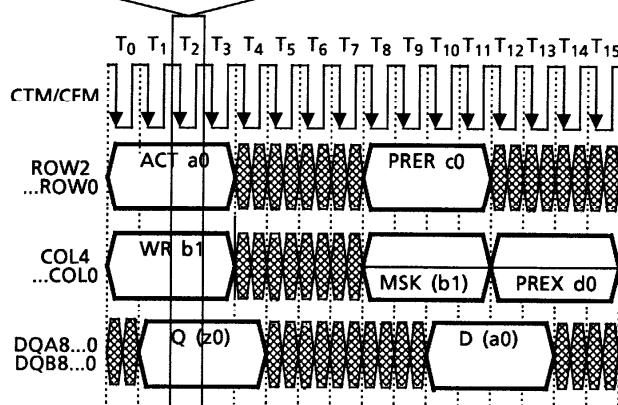
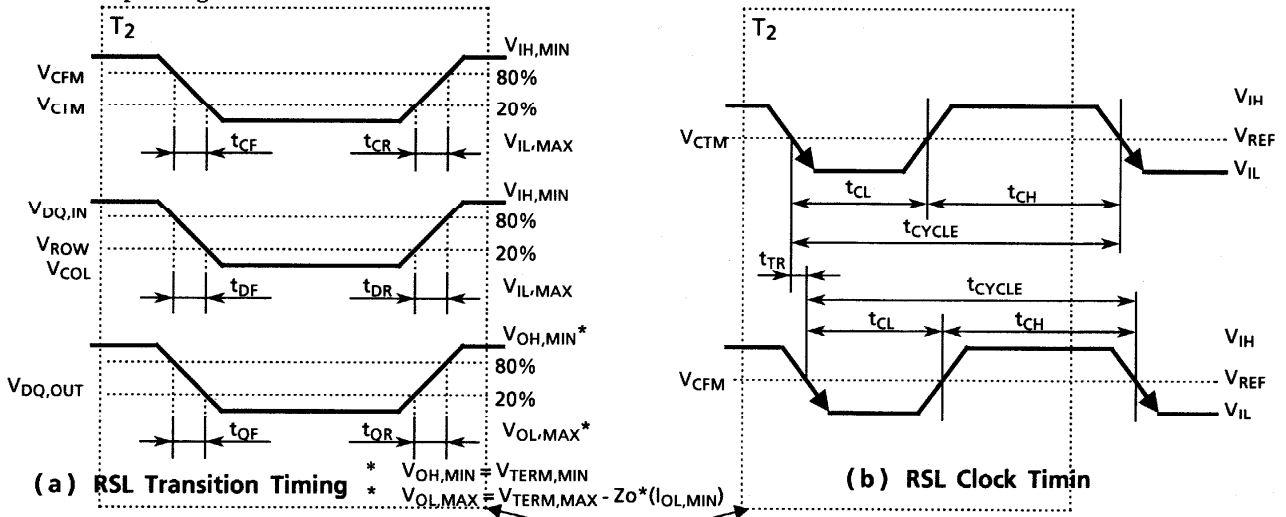


Figure 2: RSL Timing - Clocking and Bit Transport

Figure 2b shows the duty cycle requirements of the RSL clock inputs. It also shows the t_{TR} skew parameter (the amount of time by which CTM may lead CFM).

Figure 2c shows the setup and hold requirements of RSL inputs. Even bits are sampled on the falling edge of CFM and odd bits are sampled at the half-cycle (50%) point. The RDRAM synthesizes the 25%, 50%, and 75% timing points so that tow bits may be received or transmitted per clock cycle per signal wire.

Figure 2d shows the valid window of RSL outputs. Even bits are driven from the 75% point and odd bits from the 25% point.

CMOS CLOCKING AND BIT TRANSPORT

Figure 3 shows the timing required to receive or transmit a CMOS bit. A single clock cycle is expanded to show the details associated with a falling edge of the SCK clock input. Note that all CMOS signals are lowtrue ; a high voltage is logic zero.

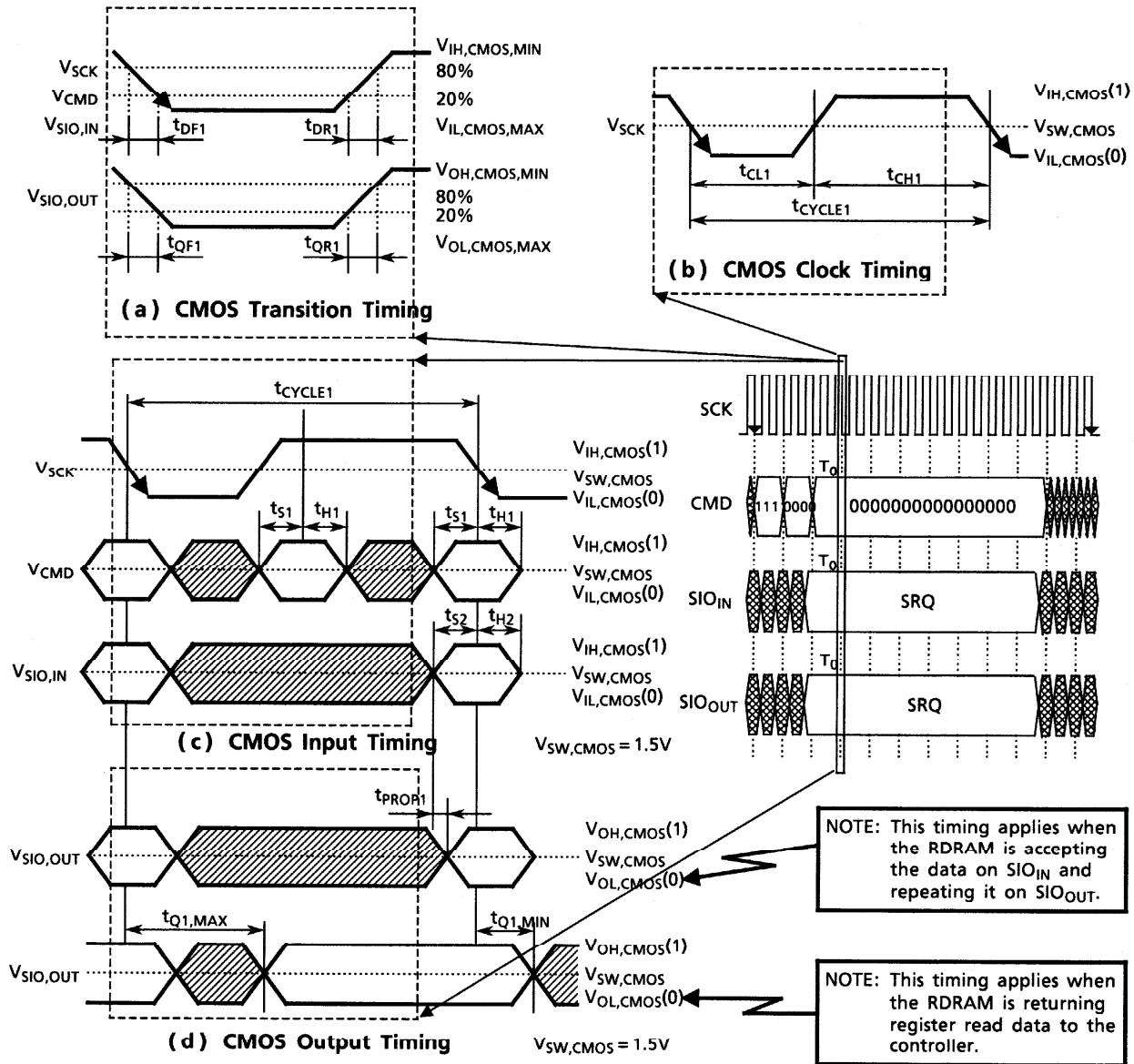
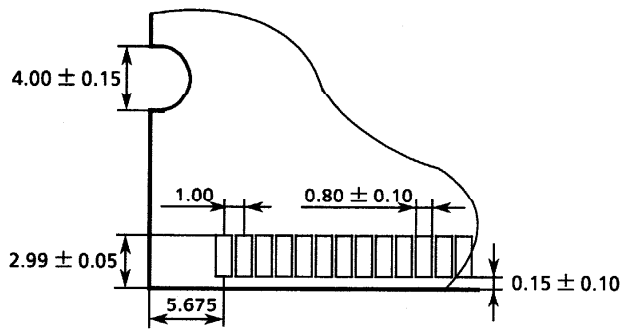
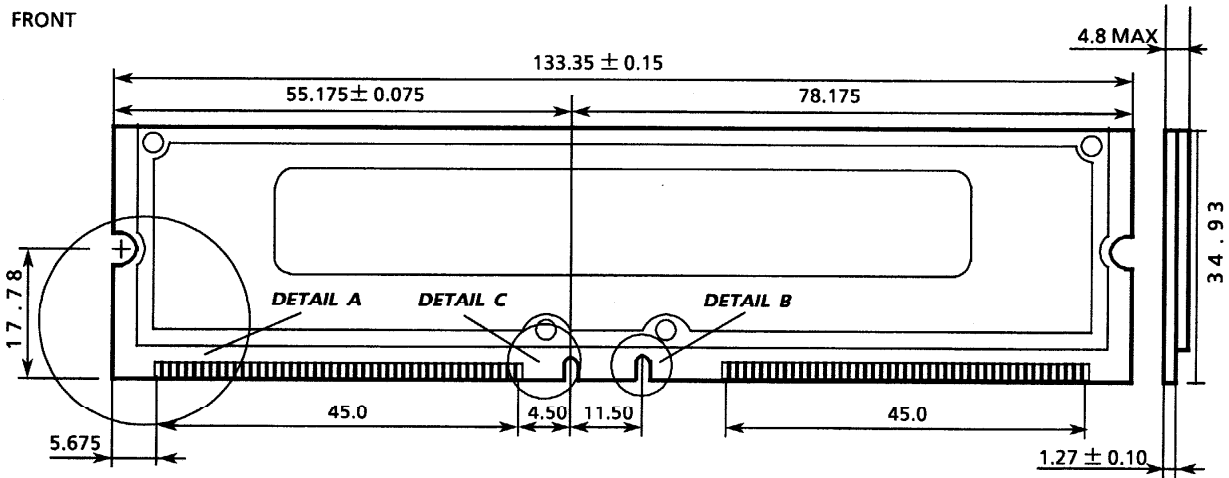


Figure 3: CMOS Timing - Clocking and Bit Transport

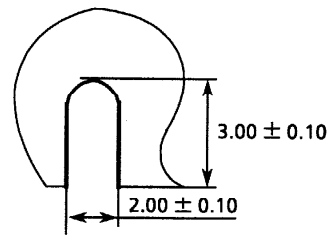
PACKAGE DIMENSIONS (THMR2E8Z)

Unit: mm

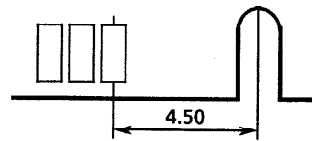
The dimensions without tolerance specification use the default tolerance of ± 0.127 .



DETAIL A



DETAIL B



DETAIL C