REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Technical change for I_{DDQ} and ΔI_{DDQ} in table I. - PHN	07-04-02	Thomas M. Hess
B	Add die requirements with appendix A. Correct low and high level bounce noise test condition for subgroup in the table IA. Update boilerplate paragraphs to current MIL-PRF-38535 requirements. - MAA	09-02-10	Charles F. Saffle
C	Update electrical test requirements in table IIA for group C and D. Update radiation features in section 1.5 and table IB. Update boilerplate paragraphs to current requirements of MIL-PRF-38535. - MAA	11-06-14	David J. Corbett
D	Add equivalent test circuits footnotes to figure 6. Delete class M requirements per updated boilerplate paragraphs. - MAA	12-11-19	Thomas M. Hess

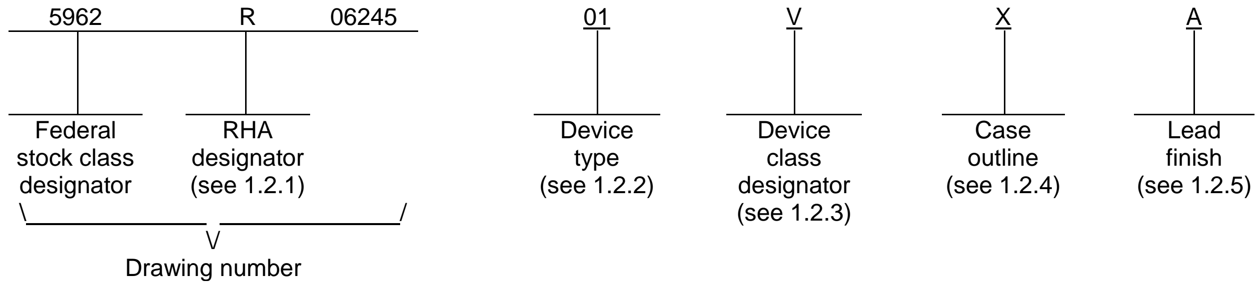
REV																				
SHEET																				
REV	D	D	D	D	D	D	D	D	D	D	D									
SHEET	15	16	17	18	19	20	21	22	23	24	25									
REV STATUS			REV			D	D	D	D	D	D	D	D	D	D	D	D	D	D	
OF SHEETS			SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A	PREPARED BY Phu H. Nguyen	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.landandmaritime.dla.mil**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Charles F. Saffle	
	APPROVED BY Thomas M. Hess	MICROCIRCUIT, DIGITAL, RADIATION HARDENED CMOS, 16-BIT D FLIP FLOP, TTL COMPATIBLE INPUTS, AND THREE-STATE OUTPUTS, MONOLITHIC SILICON
	DRAWING APPROVAL DATE 07-01-24	
	REVISION LEVEL **D**	SIZE A | CAGE CODE **67268** | **5962-06245**
		SHEET 1 OF 25

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	UT54ACTQ16374	16-bit D flip-flop, TTL compatible inputs, and three-state outputs.

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	48	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.
.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{DD}).. -0.3 V to 6.0 V
Voltage on any pin during operation ($V_{I/O}$) .... -0.3 V to V_{DD} + 0.3 V
Maximum DC input current (I_I) .... ±10 mA
Maximum power dissipation (P_D) .... 310 mW
Thermal resistance, junction to case (θ_{JC}): .... 20°C/W
Storage temperature range (T_{STG}) .... -65°C to 150°C
Maximum junction temperature (T_J) .... 175°C

1.4 Recommended operating conditions.

Supply voltage range (V_{DD}).. 4.5 V to 5.5 V
Input voltage any pin (V_{IN}) .... 0 V to V_{DD}
Maximum input rise or fall time (t_{INRISE}, t_{INFALL}).. 20 ns
Temperature range (T_C).. -55°C to 125°C

1.5 Radiation features.

Maximum total dose available (dose rate = 50 – 300 rads(Si)/s) .... 100 Krad(Si)
Single event phenomena (SEP):
No Single Event Latchup (SEL) occurs at effective LET (see 4.4.4.5)................... ≤ 108 MeV-cm^2/mg 2/
No Single Event Upset (SEU) occurs at effective LET (see 4.4.4.5) .... ≤ 95 MeV-cm^2/mg 2/
Neutron fluence .... 1 x 10^{14} n/cm^2 2/

____

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Limits are guaranteed by design or process, but not production tested unless specified by the customer through the purchase order or contract.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

ASTM INTERNATIONAL (ASTM)

ASTM F1192- Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Copies of this document is available online at http://www.astm.org/ or from ASTM International, P. O. Box C700, 100 Barr Harbor Driver, West Conshohocken, PA 19428-2959).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements for microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Function table. The function table shall be as specified on figure 3.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 4.

3.2.5 Ground bounce waveforms and test circuit. The ground bounce waveforms and test circuit shall be as specified on figure 5.

3.2.6 Switching waveform and test circuit. The switching waveform and test circuit shall be as specified on figure 6.

3.2.7 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein. The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics. 1/

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$ $4.5\ V \leq V_{DD} \leq 5.5\ V$ unless otherwise specified		Group A subgroups	Limits Min	Limits Max	Unit
Low level input voltage 2/	V_{IL}			1, 2, 3		0.8	V
High level input voltage 2/	V_{IH}			1, 2, 3	2.0		
Input leakage current	I_{IN}	$V_{IN} = V_{DD}$ or V_{SS}		1, 2, 3	-1	1	µA
Three state output leakage current 3/	I_{OZ}	$V_{IN} = V_{DD}$ or V_{SS}		1, 2, 3	-10	10	
Short circuit output current 3/ 4/	I_{OS}	$V_O = V_{DD}$ or V_{SS}		1, 2, 3	-600	600	mA
Low level output voltage	V_{OL1}	$V_{IH} = 2.0$ V or $V_{IL} = 0.8$ V	$I_{OL} = +24$ mA	1, 3		0.36	V
				2		0.5	
			$I_{OL} = +100$ µA	1, 2, 3		0.2	
Low level output voltage 5/	V_{OL2}	$V_{DD} = 5.5$ V, $I_{OL} = +50$ mA $V_{IN} = 2.0$ V or 0.8 V		1, 3		0.8	V
				2		1.0	
High level output voltage	V_{OH1}	$V_{IH} = 2.0$ V or $V_{IL} = 0.8$ V	$I_{OH} = -24$ mA	1, 2, 3	$V_{DD} - 0.64$		V
			$I_{OH} = -100$ µA	1, 2, 3	$V_{DD} - 0.8$		
High level output voltage 5/	V_{OH2}	$V_{DD} = 5.5$ V, $I_{OH} = -50$ mA $V_{IH} = 2.0$ V or $V_{IL} = 0.8$ V		1, 3	$V_{DD} - 1.1$		V
				2	$V_{DD} - 1.3$		
Positive input clamp voltage	V_{IC+}	For input under test, $I_{IN} = 18$ mA $V_{DD} = 0.0$ V		1, 2, 3	0.4	1.5	V
Negative input clamp voltage	V_{IC-}	For input under test, $I_{IN} = -18$ mA V_{DD} = open		1, 2, 3	-1.5	-0.4	V
Power dissipation 6/ 7/ 8/	P_{total}	$C_L = 20$ pF		1, 2, 3		0.5	mW/ MHz
Standby supply current V_{DD}	I_{DDQ}	$V_{IN} = V_{DD}$ or V_{SS}, $V_{DD} = 5.5$ V $\overline{OEn} = V_{DD}$		1		10	µA
				2, 3		160	
			M, D, P, L, R	1		160	
Quiescent supply current delta, TTL input level	ΔI_{DDQ}	For input under test $V_{IN} = V_{DD} - 2.1$ V For other inputs: $V_{IN} = V_{DD}$ or V_{SS} $V_{DD} = 5.5$ V		1, 2, 3		1.6	mA
			M, D, P, L, R	1		1.6	
Input capacitance	C_{IN}	f = 1 MHz @ 0 V		4		15	pF
Output capacitance	C_{OUT}					15	
Functional tests		See 4.4.1b		7, 8	L	H	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Low level V_{SS} bounce noise 9/	V_{OLP}	V_{IH} = 3.0 V, V_{IL} = 0.0 V, T_A = 25°C, V_{DD} = 5.0 V See figure 5	4		1100	mV
	V_{OLV}				-1300	
High level V_{DD} bounce noise 9/	V_{OHP}				(V_{OH} + 1200)	
	V_{OHV}				(V_{OH} – 1400)	
Maximum clock frequency 10/	f_{MAX}		9, 10, 11		100	MHz
Propagation delay time, CPn to On	t_{PLH}	See figure 6	9, 10, 11	2	10	ns
	t_{PHL}			2	10	
Output enable time, $\overline{OEn}$ to On	t_{PZL}			2	9	
	t_{PZH}			2	9	
Output disable time, $\overline{OEn}$ to On high impedance	t_{PLZ}			2	9	
	t_{PHZ}			2	9	
Setup time, high or low, In to CPn	t_S			1.5		
Hold time, high or low, IN from CPn	t_H			0.5		
Clock pulse, high or low, CPn	t_W			5.0		
Output to output skew 11/	t_{SKEW}	See figure 6	9, 10, 11		1.25	
Differential skew between outputs 12/	t_{DSKEW}				1.5	
Part-to-part output skew between outputs on multiple device under identical system conditions 6/ 11/	$t_{DSKEWPP}$	See figure 6	9, 10, 11		500	ps

1/ Device supplied to this drawing have been characterized through all levels M, D, P, L, and R of irradiation. However, this device only tested at the 'R' level. Pre and Post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

2/ Functional tests are conducted in accordance with the MIL-STD-883 with the following input test conditions: $V_{IH} = V_{IH(min)}$ +20%. -0%; . $V_{IL} = V_{IL(max)}$ +0%. -50%; as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to $V_{IH(min)}$ and $V_{IL(max)}$.

3/ Not more than one output may be shorted at a time for maximum duration of one second.

4/ Supplied as a design limit, but not guaranteed or tested.

5/ Transmission driving tests are performed at V_{DD} = 5.5 V, only one output loaded at a time with a duration not to exceed 2 ms. The test is guaranteed, if not tested, for $V_{IN} = V_{IH}$ minimum or V_{IL} maximum.

TABLE IA. Electrical performance characteristics – Continued.

6/ Guaranteed by characterization.

7/ Power does not include power contribution of any CMOS output sink current.

8/ Power dissipation specified per switching output.

9/ This test is for qualification only. Ground and V_{DD} bounce tests are performed on a non-switching (quiescent) output and are used to measure the magnitude of induced noise caused by other simultaneously switching outputs. The test is performed on a low noise bench test fixture. For the device under test, all outputs shall be loaded with 500Ω of load resistance and a minimum of 50 pF of load capacitance (see figure 5). Only chip capacitors and resistors shall be used. The output load components shall be located as close as possible to the device outputs. It is suggested, that whenever possible, this distance be kept to less than 0.25 inches. Decoupling capacitors shall be placed in parallel from V_{CC} to ground. The values of these decoupling capacitors shall be determined by the device manufacturer. The low and high level ground and V_{CC} bounce noise is measured at the quiet output using a 1 GHz minimum bandwidth oscilloscope with 50Ω input impedance.

The device inputs shall be conditioned such that all outputs are at a high nominal V_{OH} level. The device inputs shall then be conditioned such that they switch simultaneously and the output under test remains at V_{OH} as all other outputs possible are switched from V_{OH} to V_{OL}. V_{OHV} and V_{OHP} are then measured from the nominal V_{OH} level to the largest negative and positive peaks, respectively (see figure 5). This is then repeated with the same outputs not under test switching from V_{OL} to V_{OH}.

The device inputs shall be conditioned such that all outputs are at a low nominal V_{OL} level. The device inputs shall then be conditioned such that they switch simultaneously and the output under test remains at V_{OL} as all other outputs possible are switched from V_{OL} to V_{OH}. V_{OLP} and V_{OLV} are then measured from the nominal V_{OL} level to the largest positive and negative peaks, respectively (see figure 5). This is then repeated with the same outputs not under test switching from V_{OH} to V_{OL}.

10/ Verified by functional testing.

11/ Output skew is defined as a comparison of any two output transitions high-to-low vs high-to-low and low-to-high vs low-to-high.

12/ Differential skew is defined as a comparison of any two output transitions high-to-low vs low-to-high and low-to-high vs high-to-low.

TABLE IB. SEP test limits. 1/ 2/ 3/

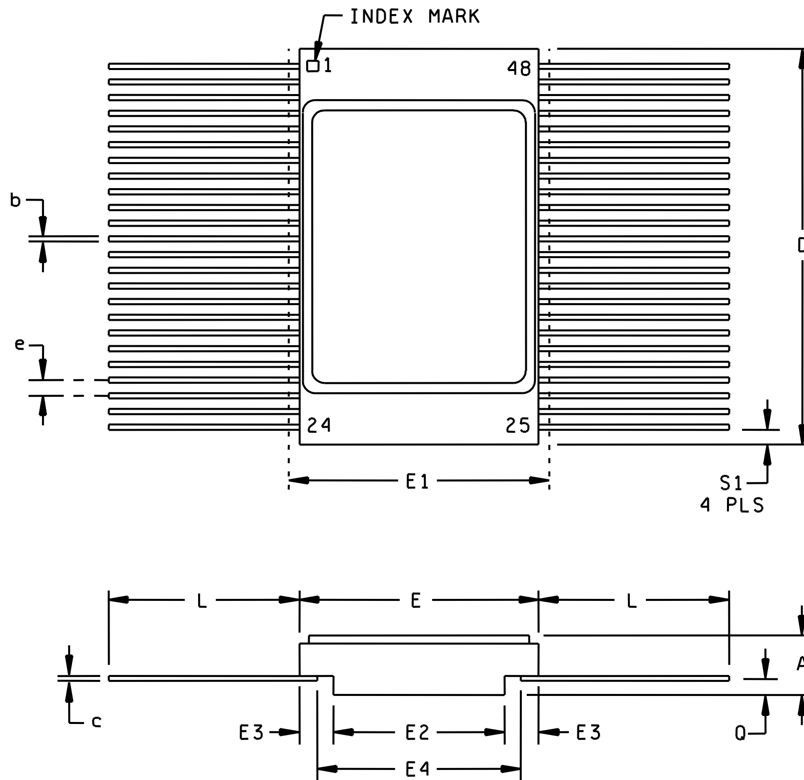
Device type	Bias V_{DD} = 4.5 V		Bias V_{DD} = 5.5 V
	Effective LET no SEU [MeV/(mg/cm^2)]	Maximum device cross section (cm^2)	Effective LET no SEL [MeV/(mg/cm^2)]
All	LET≤ 95	4.8 x 10^7	LET ≤ 108

1/ Devices that contain cross coupled resistance must be tested at the maximum rated T_A. For SEP test conditions, see 4.4.4.5 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.

3/ Worst case temperature for latch up test T_A = +125°C ±10°C and worst case operating temperature for SEU test T_A = 25°C±10°C

Case X



Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A	.095	.115	2.41	2.92	E2	.274	.286	6.96	7.26
b	.006	.010	0.15	0.25	E3	.030		0.76	
c	.004	.006	0.10	0.15	E4	.315 TYP		8.00	
D	.624	.636	15.85	16.15	L	.300	.320	7.62	8.13
e	.025 BSC		0.63 BSC		Q	.026	.045	0.66	1.14
E	.375	.385	9.52	9.78	S1	.005		0.127	
E1		.450		11.43					

Notes:

1. All exposed metalized areas are gold plated to 225 microinches thick over electroplated nickel undercoating 100 to 350 microinches per MIL-PRF-38535.
2. Seal ring is electrically connected to V_{SS}.

FIGURE 1. Case outline.

Case X

Terminal number	Terminal name	Terminal number	Terminal name	Terminal number	Terminal name	Terminal number	Terminal name
1	$\overline{OE1}$	13	O8	25	CP2	37	I7
2	O0	14	O9	26	I15	38	I6
3	O1	15	V_{SS}	27	I14	39	V_{SS}
4	V_{SS}	16	O10	28	V_{SS}	40	I5
5	O2	17	O11	29	I13	41	I4
6	O3	18	V_{DD}	30	I12	42	V_{DD}
7	V_{DD}	19	O12	31	V_{DD}	43	I3
8	O4	20	O13	32	I11	44	I2
9	O5	21	V_{SS}	33	I10	45	V_{SS}
10	V_{SS}	22	O14	34	V_{SS}	46	I1
11	O6	23	O15	35	I9	47	I0
12	O7	24	$\overline{OE2}$	36	I8	48	CP1

Pin description

Pin names	Description
$\overline{OEn}$	Output enable input (active low)
CPn	Clock pulse input
I0-I15	Inputs
O0-O15	Outputs

FIGURE 2. Terminal connections.

Inputs			Output	Operation
$\overline{OEn}$	CPn	In	On	
H	H	L	Z	Hold
H	H	H	Z	Hold
H	↑	L	Z	Load
H	↑	H	Z	Load
L	↑	L	L	Data Available
L	↑	H	H	Data Available
L	H	L	Q_O	No change in data
L	H	H	Q_O	No change in data

L = Low level voltage.
H = High level voltage.
X = Irrelevant.
↑ = High edge to clock pulse.
Z = High impedance state.
Q_O = Previous on before high to low transition of clock pulse.

FIGURE 3. Function table.

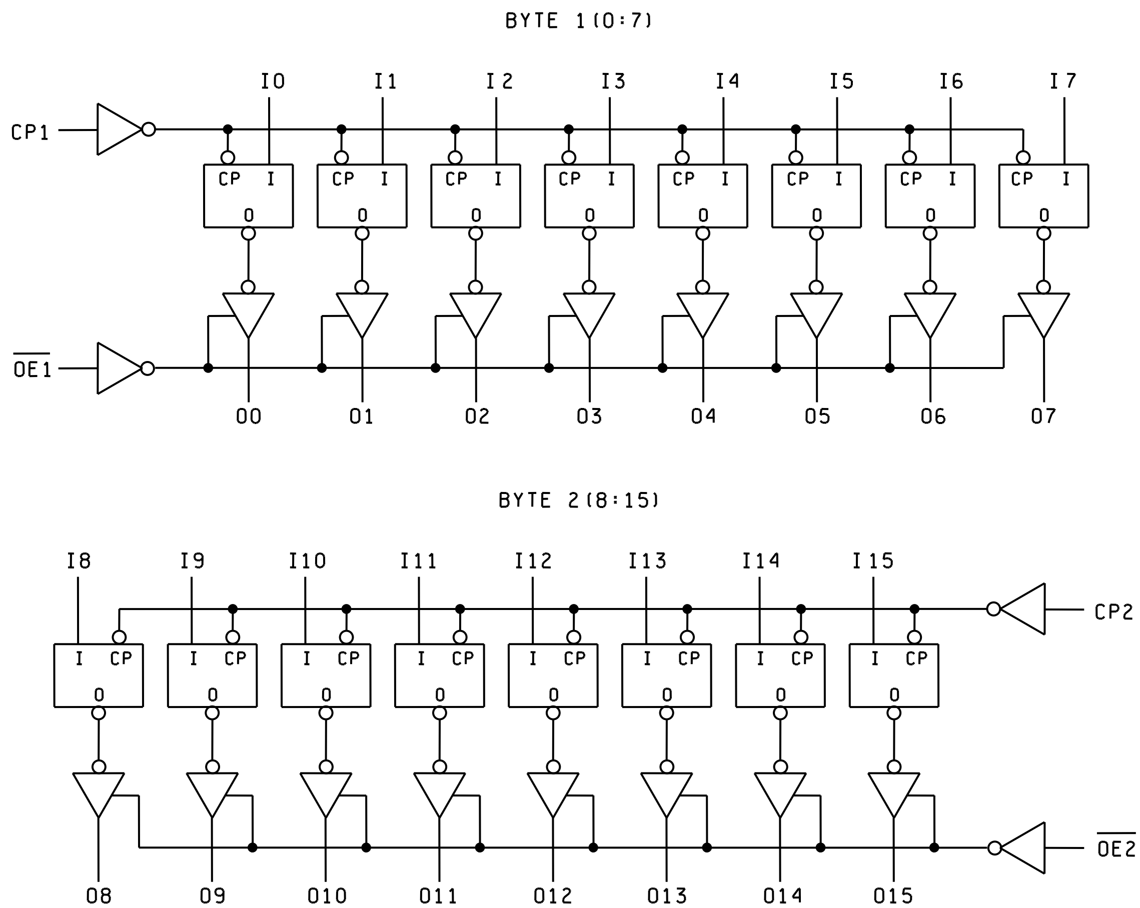
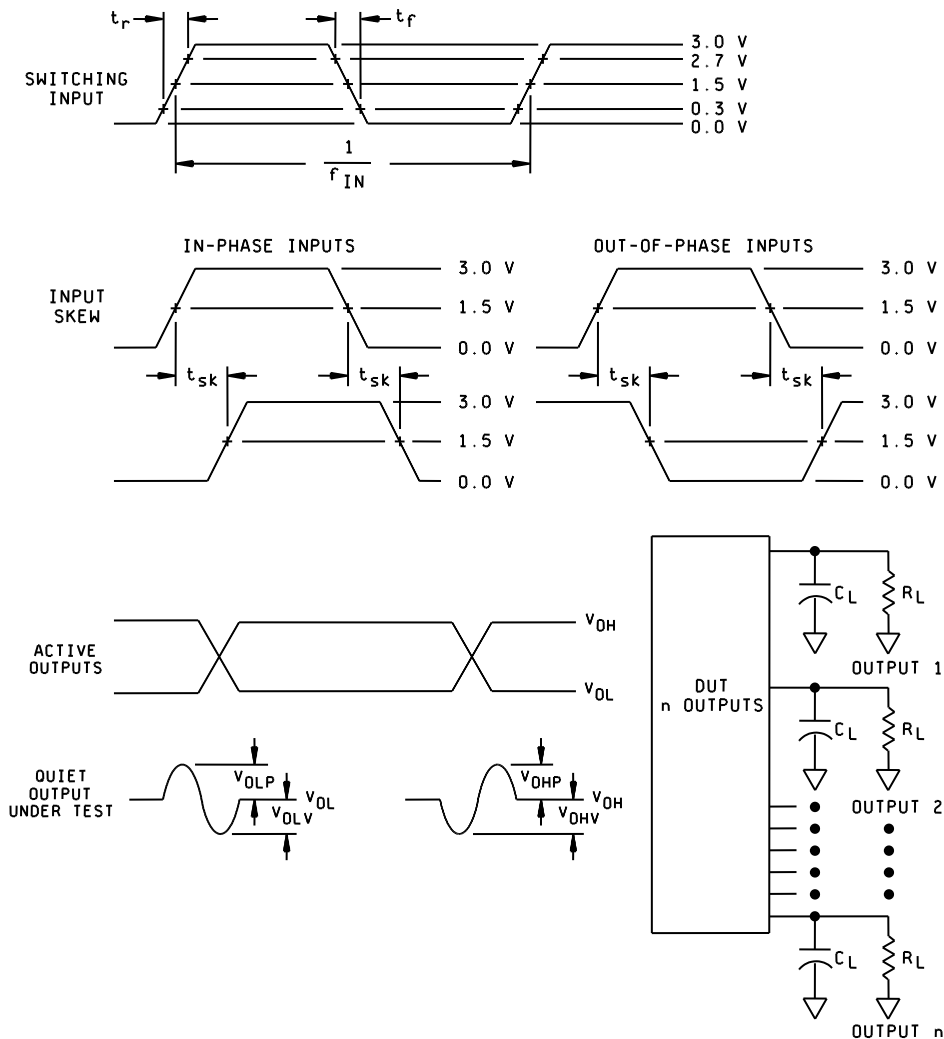


FIGURE 4. Logic diagram.



NOTES:

1. C_L includes a 47 pF chip capacitor (-0 percent, +20 percent) and at least 3 pF of equivalent capacitance from the test jig and probe.
2. R_L = 450Ω ±1 percent, chip resistor in series with a 50Ω termination. For monitored outputs, the 50Ω termination shall be the 50Ω characteristic impedance of the coaxial connector to the oscilloscope.
3. Input signal to the device under test:
   a. V_{IN} = 0.0 V to 3.0 V; duty cycle = 50 percent; $f_{IN} \geq 1$ MHz.
   b. t_r, t_f = 3 ns ±1.0 ns. For input signal generators incapable of maintaining these values of t_r and t_f, the 3.0 ns limit may be increased up to 10 ns, as needed, maintaining the ±1.0 ns tolerance and guaranteeing the results at 3.0 ns ±1.0 ns; skew between any two switching input signals (t_{sk}) ≤ 250 ps.

FIGURE 5. Ground bounce waveforms and test circuit.

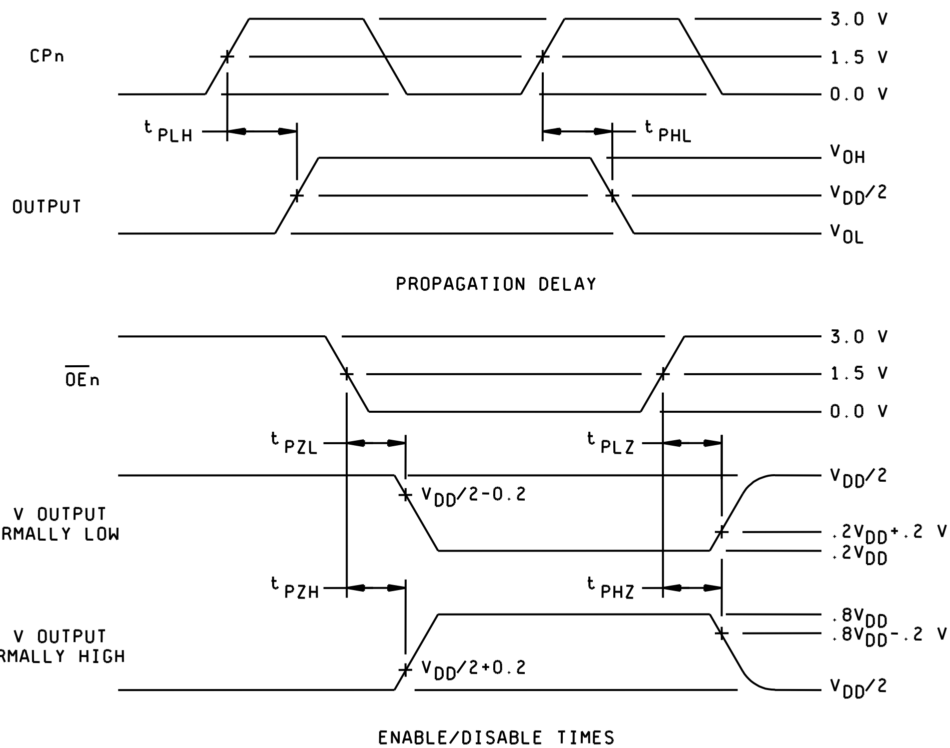
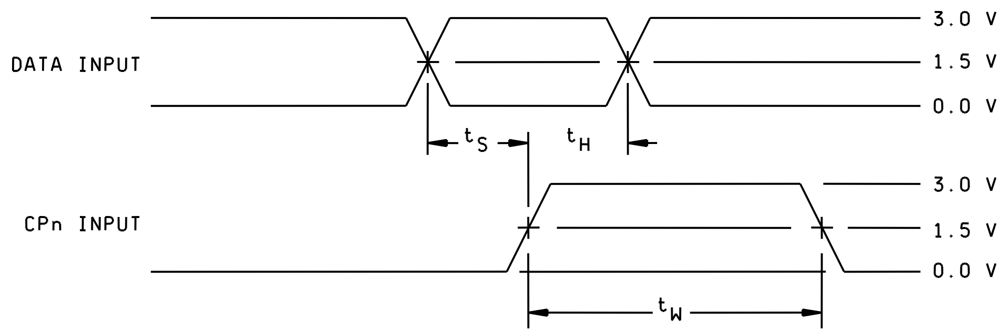
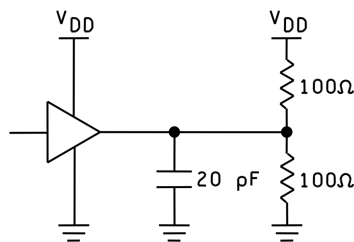


FIGURE 6. Switching waveform and test circuit.



SETUP AND HOLD MEASUREMENTS



TEST LOAD OR EQUIVALENT

NOTES:

1. C_L includes test jig and probe capacitance.
2. Equivalent test circuit means that DUT performance will be correlated and remain guaranteed to the applicable test circuit, above, whenever a test platform change necessitates a deviation from the applicable test circuit.

FIGURE 6. Switching waveform and test circuit - Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. Subgroup 4 (C_{IN} and C_{OUT}) shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} and C_{OUT} shall be measured between the designated terminal and V_{SS} at a frequency of 1 MHz. A minimum sample size of five devices with zero rejects shall be required.

d. Ground and V_{CC} bounce tests are required for all device classes. These tests shall be performed only for initial qualification, after process or design changes which may affect the performance of the device, and any changes to the test fixture. V_{OLP}, V_{OLV}, V_{OHP}, and V_{OHV} shall be measured for the worst case outputs of the device. All other outputs shall be guaranteed, if not tested, to the limits established for the worst case outputs. The worst case outputs tested are to be determined by the manufacturer. Test 5 devices assembled in worst case package type supplied to this document. All other package types shall be guaranteed, if not tested, to the limits established for the worst case package. The package type to be tested shall be determined by the manufacturer. The device manufacturer will submit to DLA Land and Maritime-VA data that shall include all measured peak values for each device tested and detailed oscilloscope plots for each V_{OLP}, V_{OLV}, V_{OHP}, and V_{OHV} from one sample part per function. The plot shall contain the waveforms of both a switching output and the output under test.

Each device manufacturer shall test product on the fixtures they currently use. When a new fixture is used, the device manufacturer shall inform DLA Land and Maritime-VA of this change and test 5 devices on both the new and old test fixtures. The device manufacturer shall then submit to DLA Land and Maritime-VA data from testing on both fixtures that shall include all measured peak values for each device tested and detailed oscilloscope plots for each V_{OLP}, V_{OLV}, V_{OHP}, and V_{OHV} from one sample part per function. The plot shall contain the waveforms of both a switching output and the output under test.

For V_{OLP}, V_{OLV}, V_{OHP}, and V_{OHV}, a device manufacturer may qualify devices by functional groups. A specific functional group shall be composed of function types that, by design, will yield the same test values when tested in accordance with table I herein. The device manufacturer shall set a functional group limit for the V_{OLP}, V_{OLV}, V_{OHP}, and V_{OHV} tests. The device manufacturer may then test one device function from a functional group to the limits and conditions specified herein. All other device functions in that particular functional group shall be guaranteed, if not tested, to the limits and conditions specified in table I herein. The device manufacturer shall submit to DLA Land and Maritime -VA the device functions listed in each functional group and the test results, along with the oscilloscope plots, for each device tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 7, 9	1, 7, 9
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11 2/ 3/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 7, 8	1, 2, 3, 7, 8A, 8B, 9, 10, 11 3/
Group D end-point electrical parameters (see 4.4)	1, 2, 7, 8A	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1 and 7.
2/ PDA applies to subgroups 1, 7 and deltas.
3/ Delta limits, as specified in table IIB, shall be required where specified, and the Delta values shall be completed with reference to the zero hour electrical parameter.

TABLE IIB. Burn in delta parameters (+25°C).

Parameter 1/	Symbol	Condition	Limits 2/ 3/
Standby supply current	I_{DDQ}	$T_A = 25°C$	10 µA 4/
Quiescent supply current delta	ΔI_{DDQ}		± 10% of measured value or 100 µA whichever is greater

1/ The above parameters shall be recorded before and after the required burn-in and life tests to determine the delta.
2/ Devices having delta drift values in excess of the device specification or drawing limits shall be rejected.
3/ When expressed as a percentage value, it should be calculated as a proportion of the previous measured value.
4/ I_{DDQ} limits were tightened from 100µA to 10µA for pre/post burn-in to determine the delta at 25°C. These tighter limits were implemented to more effectively screen out marginal parts upstream from group A and allow elimination of Deltas.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 (condition A) and as specified herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Neutron testing. When required by the customer, Neutron testing shall be performed in accordance with method 1017 of MIL-STD-883 and herein. All device classes must meet the post irradiation end-point electrical parameter limits as defined in table IA, for the subgroups specified in table IIA herein at T_A = +25°C ±5°C after an exposure of 2 x 10^{12} neutrons/cm^2 (minimum).

4.4.4.3 Dose rate induced latchup testing. When required by the customer, dose rate induced latch-up testing shall be performed in accordance with method 1020 of MIL-STD-883 and as specified herein. Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may affect the RHA capability of the process.

4.4.4.4 Dose rate upset testing. When required by the customer, dose rate upset testing shall be performed in accordance with method 1021 of MIL-STD-883 and herein.

a. Transient dose rate upset testing for class M devices shall be performed at initial qualification and after any design or process changes which may affect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535. Device parametric parameters that influence upset immunity shall be monitored at the wafer level in accordance with the wafer level hardness assurance plan and MIL-PRF-38535.

4.4.4.5 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failure. ASTM F1192 may be used as a guide line when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related affects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥20 microns in silicon.

e. The test temperature shall be +25ºC and the maximum rated operating temperature ±10ºC.

f. Bias conditions shall be V_{DD} = 4.5 V dc for the upset measurements and V_{DD} = 5.5 V dc for the latchup measurements.

g. For SEP test limits, see table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

6.7 Additional information. When specified in the purchase order or contract, a copy of the following additional data shall be supplied.

a. RHA test conditions (SEP).

b. Number of upsets (SEU).

c. Number of transients (SET).

d. Occurrence of latch-up (SEL).

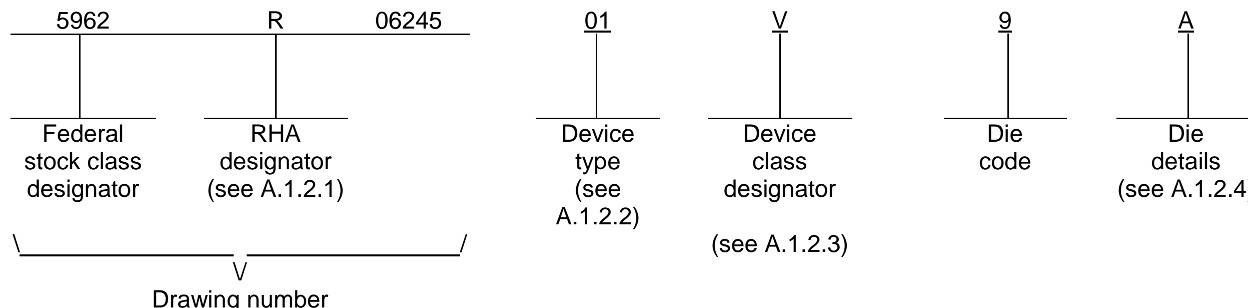
APPENDIX A

APPENDIX A FORMS A PART OF SMD 5962-06245

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device Class V) are reflected in the Part or Identification Number (PIN). When available a choice of Radiation Hardiness Assurance (RHA) levels is reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die shall meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	UT54ACTQ16374	16-bit D flip-flop and three-state outputs, TTL compatible inputs

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535.

A.1.2.4 Die Details. The die details designation shall be a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
01	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
01	A-1

A.1.2.4.3 Interface materials.

Die type	Figure number
01	A-1

A.1.2.4.4 Assembly related information.

Die type	Figure number
01	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specifications, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits Manufacturing, General Specification For.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer’s Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction and physical dimensions shall be as specified in MIL-PRF-38535 and the manufacturer’s QM plan, for device classes Q and V and herein.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and figure A-1.

A.3.2.5 Truth table. The truth table shall be as defined in paragraph 3.2.3 herein.

A.3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.6 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stacks of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not effect the form, fit or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum it shall consist of:

a) Wafer lot acceptance for Class V product using the criteria defined in MIL-STD-883 method 5007.

b) 100% wafer probe (see paragraph A.3.4 herein).

c) 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883 method 2010 or the alternate procedures allowed in MIL-STD-883 test method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table II herein. Group E tests and conditions are as specified in paragraphs 4.4.4 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications and logistics purposes.

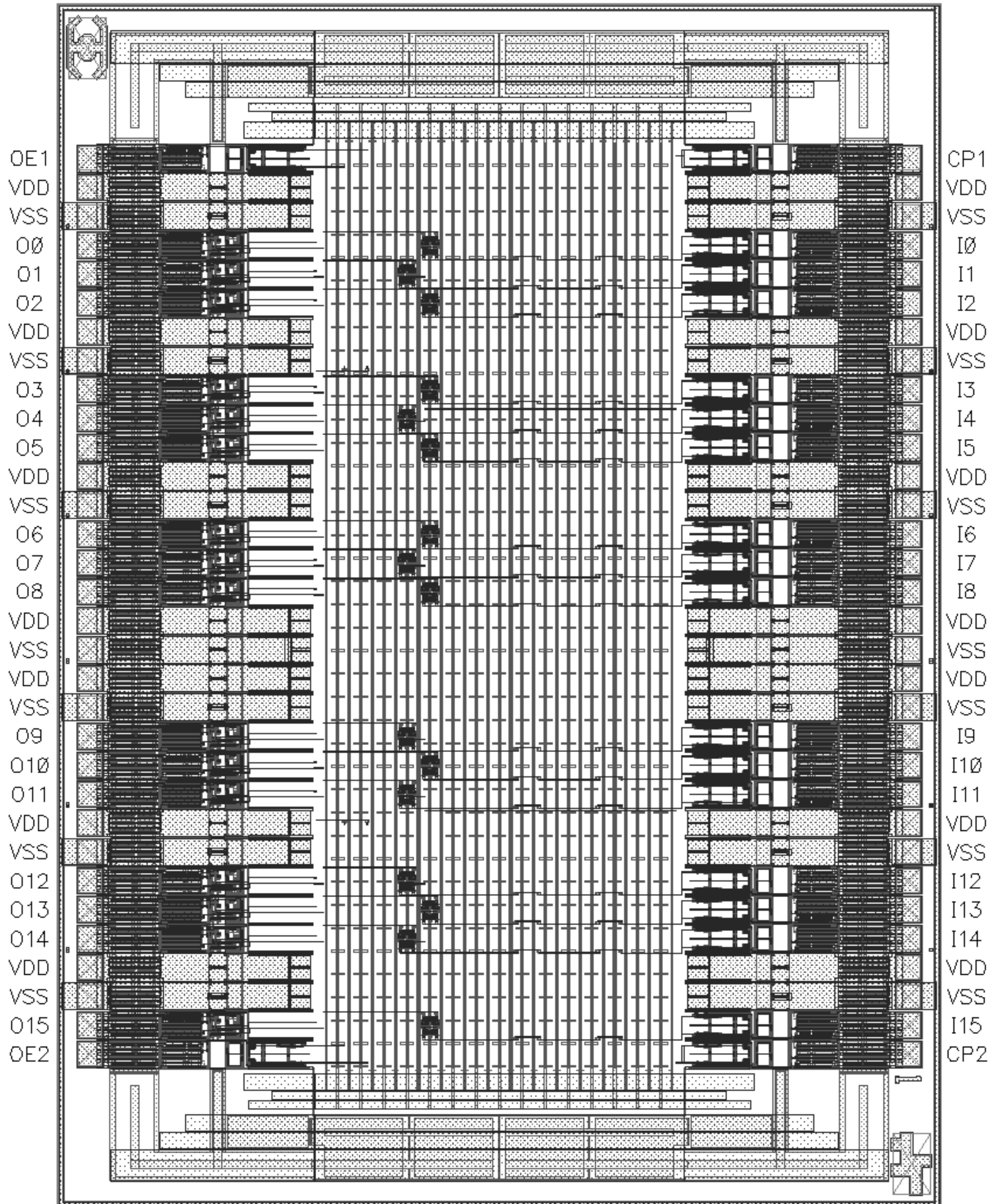
A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime -VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0547.

A.6.3 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

APPENDIX A

APPENDIX A FORMS A PART OF SMD 5962-06245



Note: Pad numbers reflect terminal numbers when placed in case outline X (see figure 1).

FIGURE A-1. Die bonding pad locations and electrical functions.

Die physical dimensions.

Die size:	112 x 152 mils
Die thickness:	17 ± 1 mil

Interface materials.

Top metallization:	Si Al Cu
Thickness:	9.0 kÅ – 12.5 kÅ
Backside metallization:	None

Glassivation:

Type:	Nitride
Thickness:	9.0 kÅ – 11.0 kÅ

Substrate: Epitaxial Layer on Single Crystal Silicon

Assembly related information.

Substrate potential:	Tied to Vss
Special assembly instructions:	Bond a Vss pad first.

FIGURE A-1. Die bonding pad locations and electrical functions – Continued.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 12-11-19

Approved sources of supply for SMD 5962-06245 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R0624501QXA	65342	UT54ACTQ16374-UCA
5962R0624501QXC	65342	UT54ACTQ16374-UCC
5962R0624501VXA	65342	UT54ACTQ16374-UCA
5962R0624501VXC	65342	UT54ACTQ16374-UCC
5962R0624501Q9A	65342	UT54ACTQ16374-Q-DIE
5962R0624501V9A	65342	UT54ACTQ16374-V-DIE

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
65342	Aeroflex Colorado Springs, Inc. 4350 Centennial Boulevard Colorado Springs, CO 80907-3486

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.