Quantum38K™ ISR™ CPLD Family

PRELIMINARY

CPLDs at ASIC Prices™

Features

- **High density**
  - **15K to 100K usable gates**
  - **256 to 1536 macrocells**
  - **92 to 302 maximum I/O pins**
  - **8 Dedicated Inputs including 4 clock pins and 4 global control signal pins; 4 JTAG interface pins for reconfigurability**
- **Embedded Memory**
  - **8K to 48K bits embedded dual-port Channel memory**
- **83 MHz in-system operation**
- **AnyVolt™ interface**
  - **3.3V and 2.5V V_{CC} operation**
  - **3.3V, 2.5V and 1.8V I/O capability**
- **Low Power Operation**
  - **0.18-μm 6-layer metal SRAM-based logic process**
  - **Full-CMOS implementation of product term array**
- **Simple timing model**
  - **No penalty for using full 16 product terms / macrocell**
  - **No delay for single product term steering or sharing**
- **Flexible clocking**
  - **4 synchronous clocks per device**
  - **Locally generated Product Term clock**
  - **Clock polarity control at each register**
- **Carry-chain logic for fast and efficient arithmetic operations**
- **Multiple I/O standards supported:**
  - **LVCMOS (3.3/3.0/2.5/1.8V), LVTTL, 3.3V PCI**
- **Compatible with NOBL™, ZBT™, and QDR™ SRAMs**
- **Programmable slew rate control on each I/O pin**
- **User-Programmable Bus Hold capability on each I/O pin**
- **Fully PCI compliant (as per PCI spec rev. 2.2)**
- **Compact PCI hot swap compatible**
- **Multiple package/pinout offering across all densities**
  - **144 to 484 pins in PQFP and FBGA packages**
  - **Simplifies design migration across density**
- **In-System Reprogrammable™ (ISR™)**
  - **JTAG-compliant on-board configuration**
  - **Design changes don't cause pinout changes**
- **IEEE1149.1 JTAG boundary scan**

Development Software

- ***Warp®***
  - **IEEE 1076/1164 VHDL or IEEE 1364 Verilog context sensitive editing**
  - **Active-HDL FSM graphical finite state machine editor**
  - **Active-HDL SIM post-synthesis timing simulator**
  - **Architecture Explorer for detailed design analysis**
  - **Static Timing Analyzer for critical path analysis**
  - **Available on Windows 95, 98 & NT for $99**
  - **Supports all Cypress Programmable Logic Products**

Quantum38K™ ISR CPLD Family Members

Device	Typical Gates[1]	Macrocells	Channel memory (Kbits)	Maximum I/O Pins	f_{MAX2} (MHz)	Speed — t_{PD} Pin-to-Pin (ns)	Standby I_{CC}[2] T_A=25°C
							3.3/2.5V
38K15	8K–24K	256	8	134	83	15	10 mA
38K30	16K–48K	512	16	176	83	15	10 mA
38K50	23K–72K	768	24	218	83	15	10 mA
38K100	46K–144K	1536	48	302	83	15	10 mA

Note:
1. Upper limit of typical gates is calculated by assuming only 50% of the channel memory is used.
2. Standby I_{CC} values are with no output load and stable inputs.

Quantum38K Speed Bins[3]

Device	83	66
38K15	X	X
38K30	X	X
38K50	X	X
38K100	X	X

Device Package Offering and I/O Count Including Dedicated Clock and Control Inputs

Device	208-EQFP 28x28 mm 0.5-mm pitch	144-FBGA 13x13 mm 1.0-mm pitch	256-FBGA 17x17 mm 1.0-mm pitch	484-FBGA 23x23 mm 1.0-mm pitch
38K15	134	92	134	
38K30	136	92	176	
38K50	136		180	218
38K100	136		180	302

Note:
3. Speed bins shown here are available in Commercial and Industrial operating ranges.

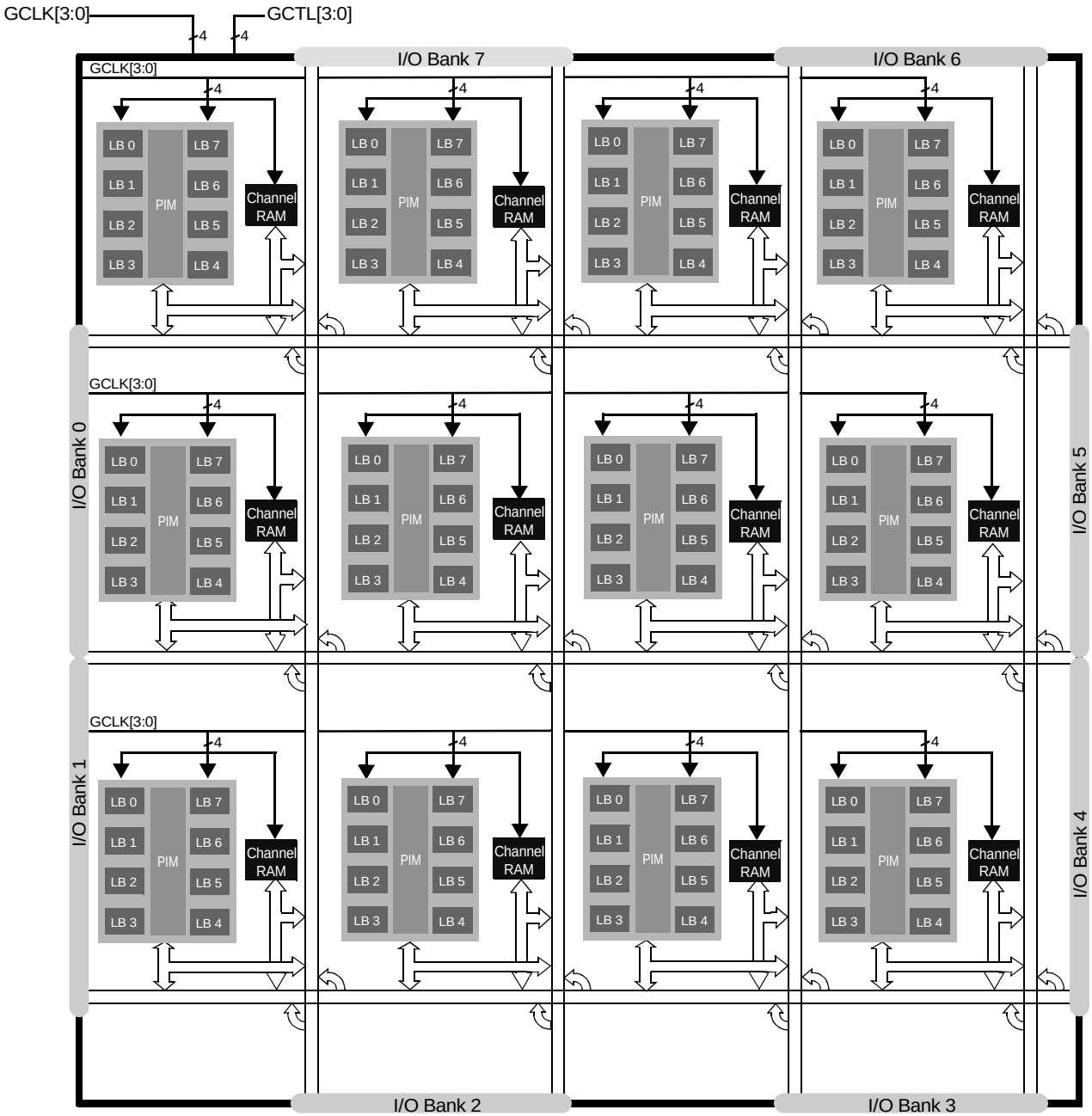


Figure 1. Quantum38K100 Block Diagram (3 Rows x 4 Columns) with I/O Bank Structure

General Description

The Quantum38K family, based on a 0.18-µm, 6-layer metal CMOS logic process, offers a wide range of solutions at very high system performance. With devices ranging from 256 to 1536 macrocells, Quantum38K is the highest density CPLD in the market besides Cypress's Delta39K. Specifically designed to address low-cost applications, this family also integrates Cypress's dual-port memory technology onto a CPLD.

The architecture is based on Logic Block Clusters (LBC) that are connected by Horizontal and Vertical (H&V) routing channels. Each LBC features eight individual Logic Blocks (LB). Adjacent to each LBC is a channel memory block, which can be accessed directly from the I/O pins. These channel memory blocks are highly configurable and can be cascaded in width and depth. See *Figure 1* for a block diagram of the Quantum38K architecture.

All the members of the Quantum38K family have Cypress's highly regarded In-System Reprogrammability (ISR) feature, which simplifies both design and manufacturing flows, thereby reducing costs. The ISR feature provides the ability to reconfigure the devices without having design changes cause pinout or timing changes in most cases. The Cypress ISR function is implemented through a JTAG-compliant serial interface. Data is shifted in and out through the TDI and TDO pins respectively. Superior routability, simple timing, and the ISR allows users to change existing logic designs while simultaneously fixing pinout assignments and maintaining system performance.

The entire family features JTAG for ISR and boundary scan, and is compatible with the PCI Local Bus specification, meeting the electrical and timing requirements. The Quantum38K family also features user programmable bus-hold and slew rate control capabilities on each I/O pin.

AnyVolt Interface

All Quantum38K devices feature an on-chip regulator, which accepts 3.3V or 2.5V on the V_{CC} supply pins and steps it down to 1.8V internally, the voltage level at which the core operates.

With Quantum38K's AnyVolt technology, the I/O pins can be connected to either 1.8V 2.5V, or 3.3V. All Quantum38K devices are 3.3V tolerant regardless of V_{CCIO} or V_{CC} settings.

Device	V_{CC}	V_{CCIO}
38K	3.3V or 2.5V	3.3V or 2.5V or 1.8V

Global Routing Description

The routing architecture of the Quantum38K is made up of horizontal and vertical (H&V) routing channels. These routing channels allow signals from each of the Quantum38K architectural components to communicate with one another. In addition to the horizontal and vertical routing channels that interconnect the I/O banks, channel memory blocks, and logic block clusters, each LBC contains a Programmable Interconnect Matrix (PIM™), which is used to route signals among the logic blocks.

Figure 2 is a block diagram of the routing channels that interface within the Quantum38K architecture. The LBC is exactly the same for every member of the Quantum38K CPLD family.

Logic Block Cluster (LBC)

The Quantum38K architecture consists of several logic block clusters, each of which have 8 Logic Blocks (LB) connected via a Programmable Interconnect Matrix (PIM) as shown in *Figure 3*. All LBCs interface with each other via horizontal and vertical routing channels.

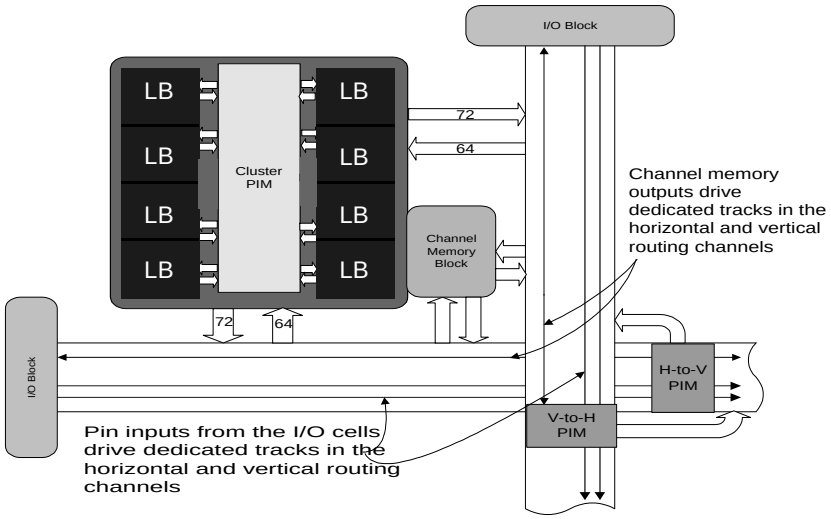


Figure 2. Quantum38K Routing Interface

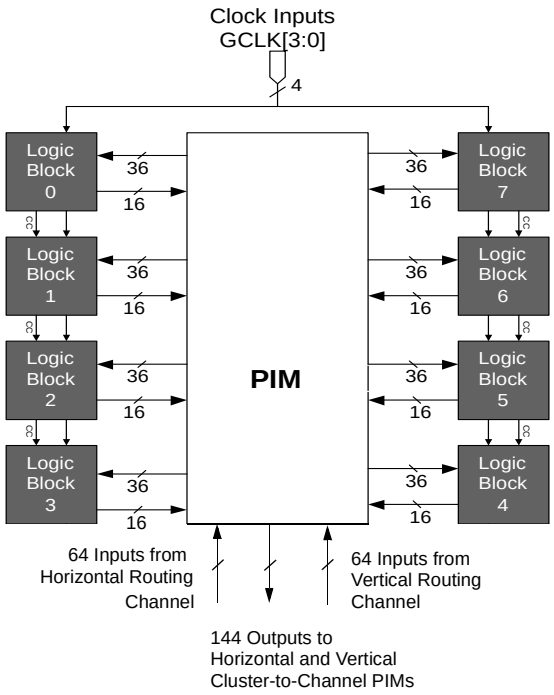


Figure 3. Quantum38K Logic Block Cluster Diagram

Logic Block (LB)

The logic block is the basic building block of the Quantum38K architecture. It consists of a product term array, an intelligent product-term allocator, and 16 macrocells.

Product Term Array

Each logic block features a 72 x 83 programmable product term array. This array accepts 36 inputs from the PIM. These inputs originate from device pins and macrocell feedbacks as well as channel memory feedbacks. Active LOW and active HIGH versions of each of these inputs are generated to create the full 72-input field. The 83 product terms in the array can be created from any of the 72 inputs.

Of the 83 product terms, 80 are for general-purpose use for the 16 macrocells in the logic block. Two of the remaining three product terms in the logic block are used as asynchronous set and asynchronous reset product terms. The final product term is the Product Term clock (PTCLK) and is shared by all 16 macrocells within a logic block.

Product Term Allocator

Through the product term allocator, *Warp* software automatically distributes the 80 product terms as needed among the 16 macrocells in the logic block. The product term allocator provides two important capabilities without affecting performance: product term steering and product term sharing.

Product Term Steering

Product term steering is the process of assigning product terms to macrocells as needed. For example, if one macrocell requires ten product terms while another needs just three, the product term allocator will “steer” ten product terms to one macrocell and three to the other. On Quantum38K devices, product terms are steered on an individual basis. Any number between 1and 16 product terms can be steered to any macrocell.

Product Term Sharing

Product term sharing is the process of using the same product term among multiple macrocells. For example, if more than one function has one or more product terms in its equation that are common to other functions, those product terms are only programmed once. The Quantum38K product term allocator allows sharing across groups of four macrocells in a variable fashion. The software automatically takes advantage of this capability so that the user does not have to intervene.

Note that neither product term sharing nor product term steering have any effect on the speed of the product. All steering and sharing configurations have been incorporated in the timing specifications for the Quantum38K devices.

Macrocell

Within each logic block there are 16 macrocells. Each macrocell accepts a sum of up to 16 product terms from the product term array. The sum of these 16 product terms can be output in either registered or combinatorial mode. *Figure 4* displays the block diagram of the macrocell. The register can be asynchronously preset or asynchronously reset at the macrocell level with the separate preset and reset product terms. Each of these product terms features programmable polarity. This allows the registers to be preset or reset based on an AND expression or an OR expression.

An XOR gate in the Quantum38K macrocell allows for many different types of equations to be realized. It can be used as a polarity mux to implement the true or complement form of an equation in the product term array or as a toggle to turn the D flip-flop into a T flip-flop. The carry-chain input mux allows additional flexibility for the implementation of different types of logic. The macrocell can utilize the carry chain logic to implement adders, subtractors, magnitude comparators, parity tree, or even generic XOR logic. The output of the macrocell is either registered or combinatorial.

Carry Chain Logic

The Quantum38K macrocell features carry chain logic which is used for fast and efficient implementation of arithmetic operations. The carry logic connects macrocells in up to 4 logic blocks for a total of 64 macrocells. Effective data path operations are implemented through the use of carry-in arithmetic, which drives through the circuit quickly. *Figure 4* shows that the carry chain logic within the macrocell consists of two product terms (CPT0 and CPT1) from the PTA and an input carry-in for carry logic. The inputs to the carry chain mux are connected directly to the product terms in the PTA. The output of the carry chain mux generates the carry-out for the next macrocell in the logic block as well as the local carry input that is connected to an input of the XOR input mux. Carry-in and a configuration bit are inputs to an AND gate. This AND gate provides a method of segmenting the carry chain in any macrocell in the logic block.

Macrocell Clocks

Clocking of the register is highly flexible. Four global synchronous clocks (GCLK[3:0]) and a Product Term clock (PTCLK) are available at each macrocell register. Furthermore, a clock polarity mux within each macrocell allows the register to be clocked on the rising or the falling edge (see macrocell diagram in *Figure 4*).

PRESET/RESET Configurations

The macrocell register can be asynchronously preset and reset using the PRESET and RESET mux. Both signals are active high and can be controlled by either of two Preset/Reset product terms (PRC[1:0] in *Figure 4*) or GND. In situations where the PRESET and RESET are active at the same time, RESET takes priority over PRESET.

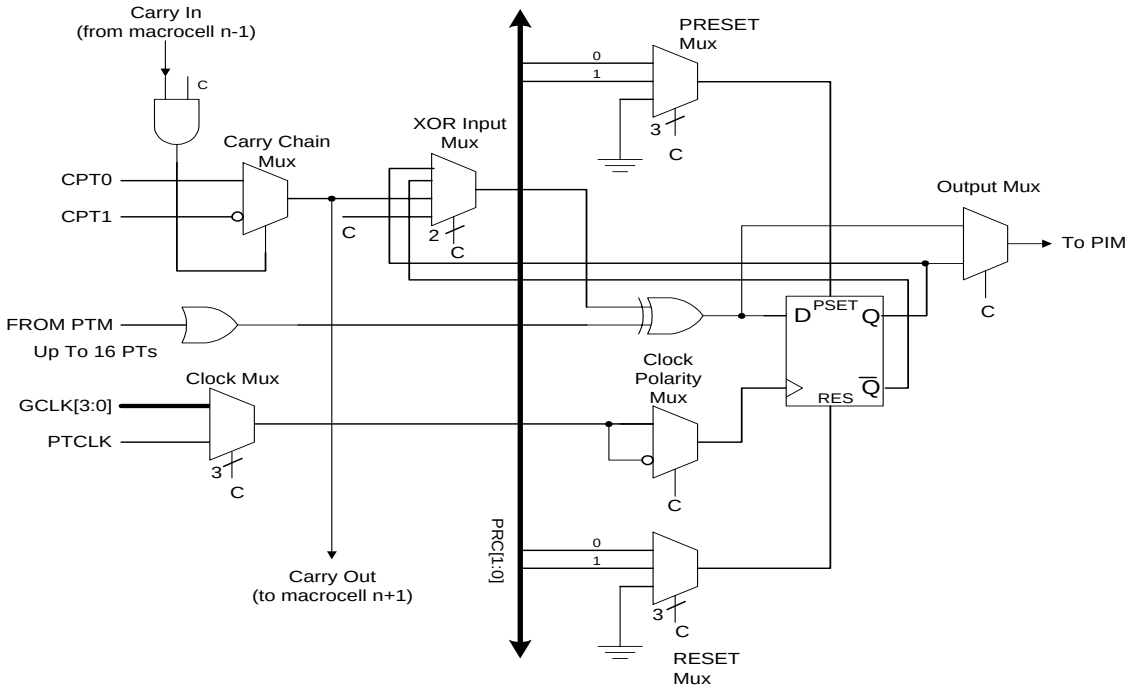


Figure 4. Quantum38K Macrocell

Embedded Memory

The Quantum38K architecture includes an embedded channel memory block at each crossing point of horizontal and vertical routing channels. The channel memory is a 4096-bit memory block that can be configured as asynchronous or synchronous Single-Port RAM, Dual-Port RAM, or Read-Only memory (ROM). The memory organization is configurable as 4Kx1, 2Kx2,1Kx4 or 512x8.

Data, address, and control inputs to the channel memory are driven from horizontal and vertical routing channels. All data logic outputs drive dedicated tracks in the horizontal and vertical routing channels. The clocks for the channel memory block are selected from four global clocks and pin inputs from the horizontal and vertical channels. The clock muxes also include a polarity mux for each clock so that the user can choose an inverted clock.

Dual-Port (Channel Memory) Configuration

Each port has distinct address inputs, as well as separate data and control inputs that can be accessed simultaneously. The inputs to the Dual-Port memory are driven from the horizontal and vertical routing channels. The data outputs drive dedicated tracks in the routing channels. The interface to the routing is such that Port A of the Dual-Port interfaces primarily with the horizontal routing channel and Port B interfaces primarily with the vertical routing channel.

The clocks for each port of the Dual-Port configuration are selected from four global clocks and two local clocks. One local clock is sourced from the horizontal channel and the other from the vertical channel. The data outputs of the dual-port memory can also be registered. Clocks for the output registers are also selected from four global clocks and two local clocks. One clock polarity mux per port allows the use of true or complement polarity for input and output clocking purposes.

Arbitration

The Dual-Port configuration of the Channel Memory Block provides arbitration when both ports access the same address at the same time. Depending on the memory operations being attempted, one port always gets priority. See *Table 1* for details on which port gets priority for read and write operations. An active-LOW 'Address Match' signal is generated when an address collision occurs.

Table 1. Arbitration Result: Address Match Signal Becomes Active

Port A	Port B	Result of Arbitration	Comment
Read	Read	No arbitration required	Both ports read at the same time
Write	Read	Port A gets priority	If Port B requests first then it will read the current data. The output will then change to the newly written data by Port A
Read	Write	Port B gets priority	If Port A requests first then it will read the current data. The output will then change to the newly written data by Port B
Write	Write	Port A gets priority	Port B is blocked until Port A is finished writing

Channel Memory Initialization

The channel memory powers up in an undefined state, but is set to a user-defined known state during configuration. To facilitate the use of look-up-table (LUT) logic and ROM applications, the channel memory blocks can be initialized with a given set of data when the device is configured at power up. For LUT and ROM applications, the user cannot write to memory blocks.

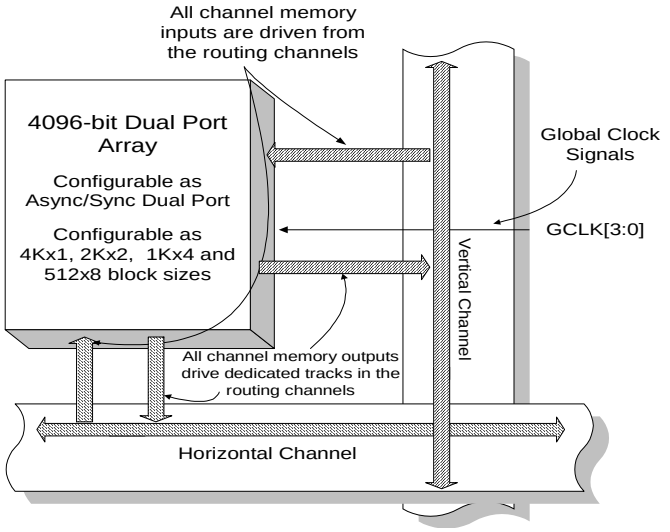


Figure 5. Block Diagram of Channel Memory Block

Channel Memory Routing Interface

Similar to LBC outputs, the channel memory blocks feature dedicated tracks in the horizontal and vertical routing channels for the data outputs and the flag outputs, as shown in *Figure 5*. This allows the channel memory blocks to be expanded easily. These dedicated lines can be routed to I/O pins as chip outputs or to other logic block clusters to be used in logic equations.

I/O Banks

The Quantum38K interfaces the horizontal and vertical routing channels to the pins through I/O banks. There are 8 I/O banks per device as shown in *Figure 6*, and all I/Os from an I/O bank are located in the same section of a package for PCB layout convenience.

For each package type, Quantum38K devices of different densities keep given pins in the same I/O banks. This supports and simplifies design migration across densities.

Each I/O bank contains several I/O cells, and each I/O cell contains an input/output register, an output enable register, programmable slew rate control and programmable bus hold control logic. Each I/O cell drives a pin output of the device; the cell also supplies an input to the device that connects to a dedicated track in the associated routing channel.

There are four dedicated inputs (GCTL[3:0]) that are used as Global Control Signals available to every I/O cell. These global control signals may be used as output enables, register resets and register clock enables as shown in *Figure 7*.

Each I/O bank can use any supported I/O standard by supplying appropriate V_{CCIO} voltages. All the V_{CCIO} pins in an I/O bank must be connected to the same V_{CCIO} voltage. This requirement restricts the number of I/O standards supported by an I/O bank at any given time.

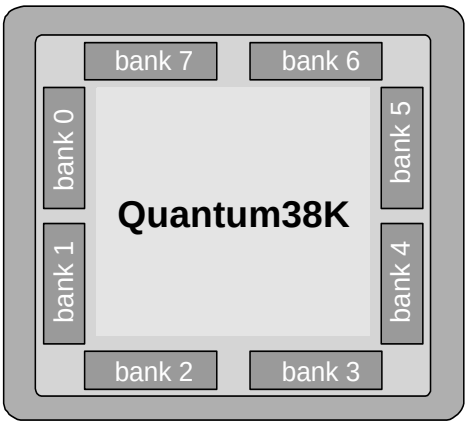


Figure 6. Quantum38K I/O Bank Block Diagram

IO Standards

I/O Standard	V_{CCIO}
LVTTL	3.3V
LVCMOS	3.3V
LVCMOS3	3.0V
LVCMOS2	2.5V
LVCMOS18	1.8V
3.3V PCI	3.3V

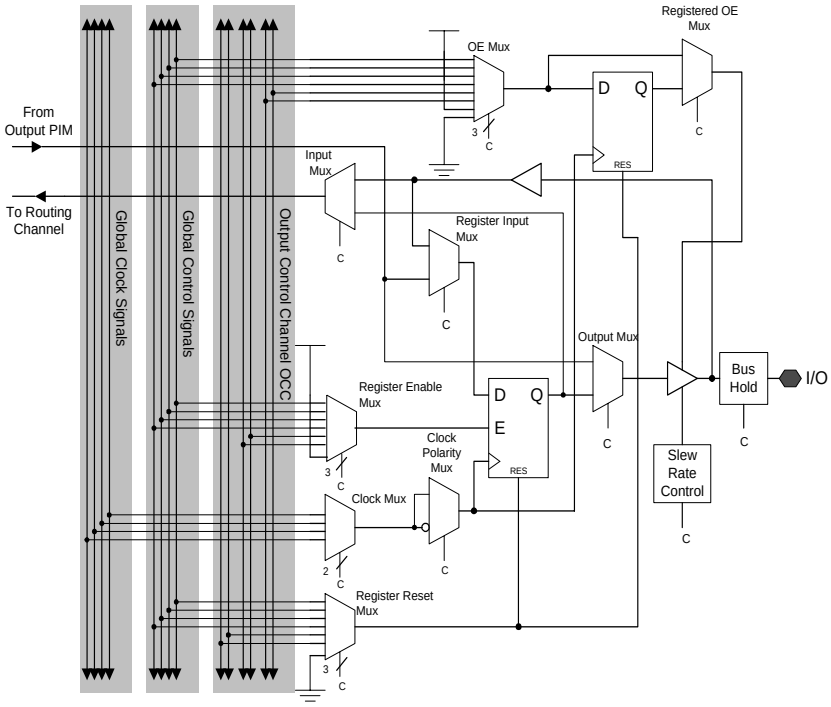


Figure 7. Block Diagram of I/O Cell

I/O Cell

Figure 7 is a block diagram of the Quantum38K I/O cell. The I/O cell contains a three-state input buffer, an output buffer, and a register that can be configured as an input or output register. The output buffer has a slew rate control option that can be used to configure the output for a slower slew rate. The input of the device and the pin output can each be configured as registered or combinatorial; however, only one path can be configured as registered in a given design.

The output enable can be selected from one of the four global control signals or from one of two Output Control Channel (OCC) signals. The output enable can be configured as always enabled or always disabled or it can be controlled by one of the remaining inputs to the mux. The selection is done via a mux that includes V_{CC} and GND as inputs.

One of the global clocks can be selected as the clock for the I/O cell register. The clock mux output is an input to a clock polarity mux that allows the input/output register to be clocked on either edge of the clock.

Slew Rate Control

The ouput buffer has a slew rate control option. This allows the output buffer to slew at a fast rate (3 V/ns) or a slow rate (1 V/ns). All I/Os default to fast slew rate. For designs concerned with meeting FCC emissions standards the slow edge provides for lower system noise. For designs requiring very high performance the fast edge rate provides maximum system performance.

Programmable Bus Hold

On each I/O pin, user-programmable-bus-hold is included. Bus-hold, which is an improved version of the popular internal pull-up resistor, is a weak latch connected to the pin that does not degrade the device's performance. As a latch, bus-hold maintains the last state of a pin when the pin is placed in a high-impedance state, thus reducing system noise in bus-interface applications. Bus-hold additionally allows unused device pins to remain unconnected on the board, which is particularly useful during prototyping as designers can route new signals to the device without cutting trace connections to V_{CC} or GND. For more information, see the application note "Understanding Bus-Hold – A Feature of Cypress CPLDs."

Clocks

Quantum38K has four dedicated clock input pins (GCLK[3:0]) to accept system clocks.

The global clock tree for a Quantum38K device is driven by the dedicated clock pins, consisting of four global clocks that go to every macrocell, memory block, and I/O cell.

Clock Tree Distribution

The clock tree distributes the four global clocks to every cluster, channel memory, and I/O block on the die. The global clock tree is designed such that the clock skew is minimized while maintaining an acceptable clock delay.

Timing Model

One important feature of the Quantum38K family is the simplicity of its timing. All combinatorial and registered/synchronous delays are worst case and system performance is static (as shown in the AC specs section) as long as data is routed through the same horizontal and vertical channels. *Figure 8* illustrates the true timing model for the 38K100 devices. For synchronous clocking of macrocells, a delay is incurred from macrocell clock to macrocell clock of separate Logic Blocks within the same cluster, as well as separate Logic Blocks within different clusters. This is respectively shown as t_{SCS} and t_{SCS2} in *Figure 8.* For combinatorial paths, any input to any output (from corner to corner on the device), incurs a worst-case delay in the 38K100 regardless of the amount of logic or which horizontal and vertical channels are used. This is the t_{PD} shown in *Figure 8.* For synchronous systems, the input set-up time to the output macrocell register and the clock to output time are shown as the parameters t_{MCS} and t_{MCCO} shown in the *Figure 8.* These measurements are for any output and synchronous clock, regardless of the logic placement.

The Quantum38K features:

- no dedicated vs. I/O pin delays
- no penalty for using 0–16 product terms
- no added delay for steering product terms
- no added delay for sharing product terms
- no output bypass delays

The simple timing model of the Quantum38K family eliminates unexpected performance penalties.

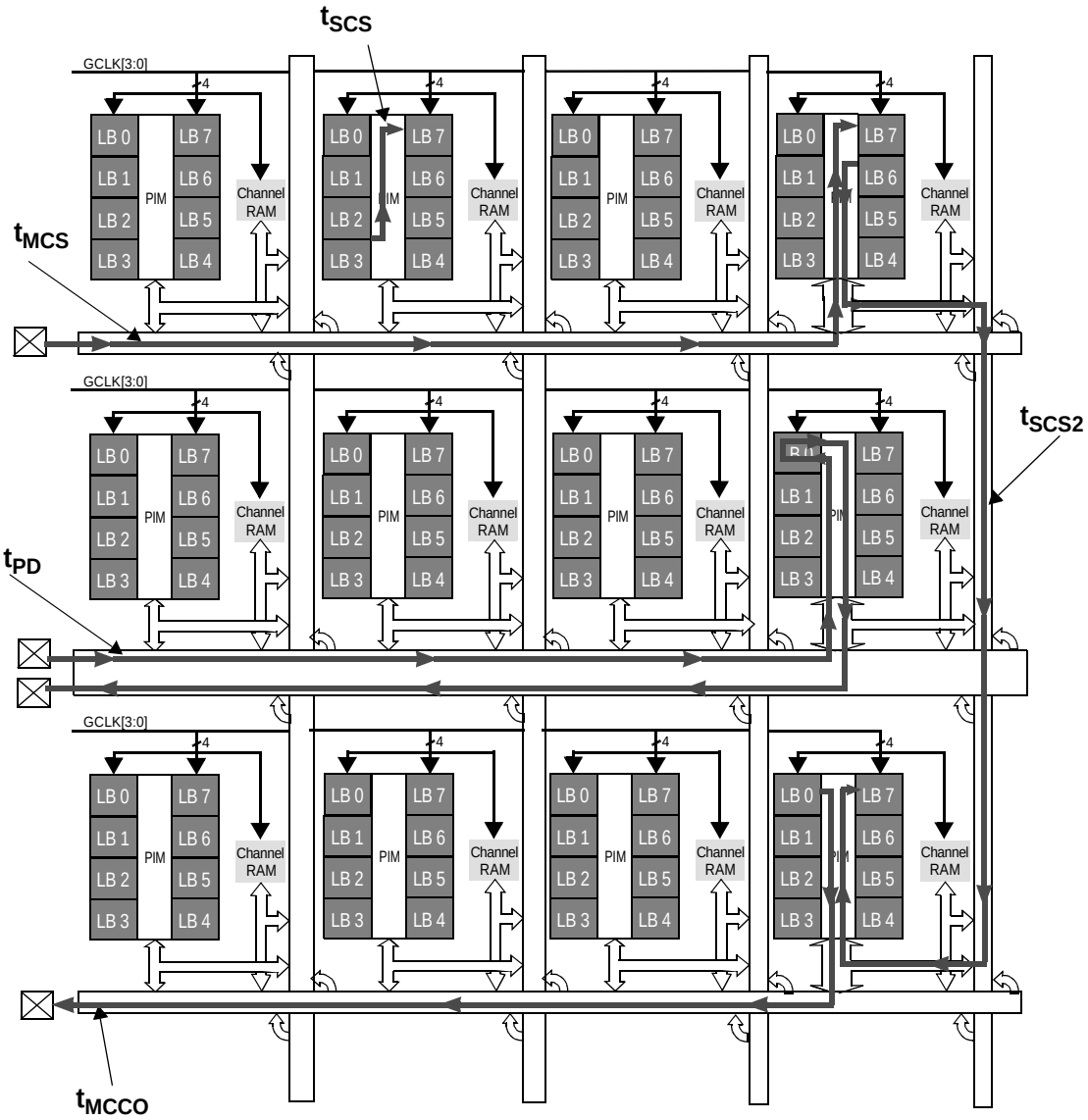


Figure 8. Timing Model for 38K100 Device

IEEE 1149.1 Compliant JTAG Operation

The Quantum38K family has an IEEE 1149.1 JTAG interface for both Boundary Scan and ISR operations.

Four dedicated pins are reserved on each device for use by the Test Access Port (TAP).

Boundary Scan

The Quantum38K family supports Bypass, Sample/Preload, Extest, Intest, Idcode and Usercode boundary scan instructions. The JTAG interface is shown in *Figure 9*.

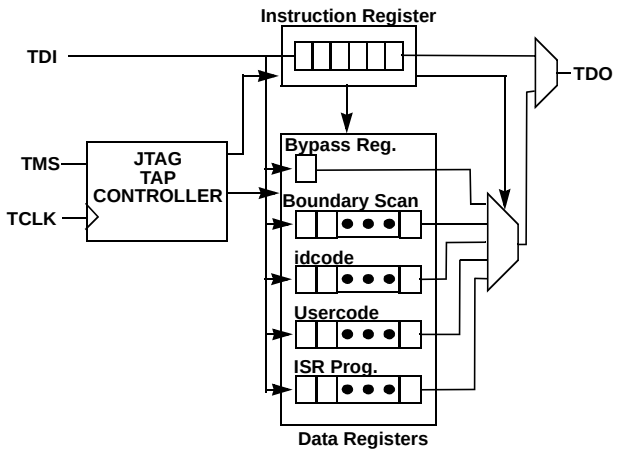


Figure 9. JTAG Interface

In-System Reprogramming (ISR)

In-System Reprogramming is the combination of the capability to program or reprogram a device on-board, and the ability to support design changes without changing the system timing or device pinout. This combination means design changes during debug or field upgrades do not cause board respins. The Quantum38K family implements ISR by providing a IEEE std 1149.1 JTAG compliant interface for on-board configuration. Robust routing resources offer pinout flexibility and a simple timing model provides consistent system performance.

Configuration

Quantum38K is a SRAM based volatile device family that uses Cypress's CY3LV series of CPLD boot EEPROM to store configuration data. Please refer to the data sheet titled "CPLD Boot EEPROM" and the application note titled "Configuring Delta39K/Quantum38K" for more details on configuration and interface set-up between Quantum38K & CPLD boot PROM. These documents can be found at http://www.cypress.com

For Quantum38K design, configuration is defined as the loading of a user's design into the volatile Quantum38K die. Programming, on the other hand, is the loading of a user's design into the serial boot PROM.

Device configuration can begin in two ways. It can be initiated by toggling the *Reconfig* pin from LOW to HIGH, or by issuing the appropriate IEEE std 1149.1 JTAG instruction to the Quantum38K device via the JTAG interface. There are two IEEE std 1149.1 JTAG instructions that initiate configuration of the Quantum38K. The *Self Config* instruction causes the Quantum38K to (re)configure with data stored in the serial boot PROM. The *Load Config* instruction causes the Quantum38K to (re)configure according to data provided by other sources such as a PC, automatic test equipment (ATE), or an embedded micro-controller/processor via the JTAG interface.

There are two configuration options available for issuing the IEEE std 1149.1 JTAG instructions to the Quantum38K. The first method is to use a PC with the C3 ISR programming cable and software. With this method, the ISR pins of the Quantum38K devices in the system are routed to a connector at the edge of the printed circuit board. The C3 ISR programming cable is then connected between the PC and this connector. A simple configuration file instructs the ISR software of the programming operations to be performed on the Quantum38K devices in the system. The ISR software then automatically completes all of the necessary data manipulations required to accomplish configuration, reading, verifying, and other ISR functions. For more information on the Cypress ISR interface, see the ISR Programming Kit data sheet (CY3900i).

The second configuration option for the Quantum38K is to utilize the embedded controller or processor that already exists in the system. The Quantum38K ISR software assists in this method by converting the device HEX file into the ISR serial stream that contains the ISR instruction information and the addresses and data of locations to be configured. The embedded controller then simply directs this ISR stream to the chain of Quantum38K devices to complete the desired reconfiguration or diagnostic operations. Contact your local sales office for information on availability of this option.

Programming

There are multiple methods available for programming the serial boot PROM. The first method uses Cypress's CYDH2200E CPLD Boot PROM Programming Kit to program via a two-wire interface.

The second method is through third-party programmers. Programming support for CY3LV series of boot PROMs is available on a wide variety of third-party programmers. All major programmers (including BP Micro, Data I/O, System General, Hi-Lo) support boot PROM programming.

Development Software Support

Warp

Warp is a state-of-the-art design environment for designing with Cypress programmable logic. *Warp* utilizes a subset of IEEE 1076/1164 VHDL and IEEE 1364 as the Hardware Description Language (HDL) for design entry. *Warp* accepts VHDL or Verilog input, synthesizes and optimizes the entered design, and outputs a configuration bitstream for the desired Quantum38K device. For simulation, *Warp* provides a graphical waveform simulator as well as VHDL and Verilog Timing Models.

VHDL and Verilog are open, powerful, non-proprietary Hardware Description Languages (HDLs) that are standards for behavioral design entry and simulation. HDL allows designers to learn a single language that is useful for all facets of the design process.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Soldering Temperature..... 220°C

Ambient Temperature with Power Applied..... –40°C to +85°C

Junction Temperature..... 135°C

V_{CC} to Ground Potential..... –0.5V to 4.6V

V_{CCIO} to Ground Potential..... –0.5V to 4.6V

DC Voltage Applied to Outputs in High Z State –0.5V to 4.5V

DC Input voltage..... –0.5V to 4.5V

DC Current into Outputs..... ±20 mA

Static Discharge Voltage (per MIL-STD-8883, Method 3015)..... >2001V

Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature	Junction Temperature	Output Condition	V_{CCIO}	V_{CC}	V_{CCJTAG}/ V_{CCCNFG}
Commercial	0°C to +70°C	0°C to +85°C	3.3V	3.3V ± 0.3V	3.3V ± 0.3V or 2.5V ± 0.2V	Same as V_{CCIO}
			2.5V	2.5V ± 0.2V		
			1.8V	1.8 ± 0.15V		
Industrial	–40°C to +85°C	–40°C to +100°C	3.3V	3.3V ± 0.3V		
			2.5V	2.5V ± 0.2V		
			1.8V	1.8 ± 0.15V		

DC Characteristics

Parameter	Description	Test Conditions	V_{CCIO} = 3.3 V		V_{CCIO} = 2.5 V		V_{CCIO} = 1.8 V		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V_{DRINT}	Data Retention V_{CC} Voltage (config data may be lost below this)		1.5		1.5		1.5		V
V_{DRIO}	Data Retention V_{CCIO} Voltage (config data may be lost below this)		1.2		1.2		1.2		V
I_{IX}	Input Leakage Current	$GND \le V_I \le 3.6V$	–10	10	–10	10	–10	10	µA
I_{OZ}	Output Leakage Current	$GND \le V_O \le V_{CCIO}$	–10	10	–10	10	–10	10	µA
I_{OS}[4]	Output Short Circuit Current	V_{CCIO} = Max., V_{OUT} = 0.5V		–160		–160		–160	mA
I_{BHL}	Input Bus Hold LOW Sustaining Current	V_{CC} = Min., $V_{PIN} = V_{IL}$	+40		+30		+25		µA
I_{BHH}	Input Bus Hold HIGH Sustaining Current	V_{CC} = Min., $V_{PIN} = V_{IH}$	–40		–30		–25		µA
I_{BHLO}	Input Bus Hold LOW Overdrive Current	V_{CC} = Max.		+250		+200		+150	µA
I_{BHHO}	Input Bus Hold HIGH Overdrive Current	V_{CC} = Max.		–250		–200		–150	µA

Note:

4. Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V_{OUT}=0.5V has been chosen to avoid test problems caused by tester ground degradation. Tested initially and after any design or process changes that may affect this parameter.

Capacitance

Parameter	Description	Test Conditions	Min.	Max.	Unit
$C_{I/O}$	Input/Output Capacitance	$V_{in}=V_{CCIO}$ @ f=1MHz 25°C		10	pF
C_{CLK}	Clock Signal Capacitance	$V_{in}=V_{CCIO}$ @ f=1MHz 25°C	5	12	pF
C_{PCI}	PCI Compliant[5] Capacitance	$V_{in}=V_{CCIO}$ @ f=1MHz 25°C		8	pF

DC Characteristics[6] (IO)

Input/ Output Standard	V_{CCIO} (V)	V_{OH} (V)		V_{OL} (V)		V_{IH} (V)		V_{IL} (V)	
		@ I_{OH} =	V_{OH} (min.)	@ I_{OL} =	V_{OL} (max.)	Min.	Max.	Min.	Max.
LVTTL	3.3	–4 mA	2.4	4 mA	0.4	2.0 V	V_{CCIO}+0.3	–0.3V	0.8V
LVCMOS	3.3	–0.1 mA	V_{CCIO}–0.2v	0.1 mA	0.2	2.0 V	V_{CCIO}+0.3	–0.3V	0.8V
LVCMOS3	3.0	–0.1 mA	V_{CCIO}–0.2v	0.1mA	0.2	2.0 V	V_{CCIO}+0.3	–0.3V	0.8V
LVCMOS2	2.5	–0.1 mA	2.1	0.1 mA	0.2	1.7 V	V_{CCIO}+0.3	–0.3V	0.7V
		–1.0 mA	2.0	1.0 mA	0.4				
		–2.0 mA	1.7	2.0 mA	0.7				
LVCMOS18	1.8	–0.1 mA	V_{CCIO}–0.2v	0.1 mA	0.2	$0.65V_{CCIO}$	V_{CCIO}+0.3	–0.3V	$0.35V_{CCIO}$
		–2 mA	V_{CCIO}–0.45v	2.0 mA	0.45				
3.3V PCI	3.3	–0.5 mA	$0.9V_{CCIO}$	1.5 mA	$0.1V_{CCIO}$	$0.5V_{CCIO}$	V_{CCIO}+0.5	–0.5V	$0.3V_{CCIO}$

Configuration Parameters

Parameter	Description	Min.	Unit
$t_{RECONFIG}$	*Reconfig* pin LOW time before it goes HIGH	200	ns

Power-up Sequence Requirements

- Upon power-up, all the outputs remain three-stated until all the V_{CC} pins have powered-up to the nominal voltage and the part has completed configuration.
- The part will not start configuration until V_{CC}, V_{CCIO}, V_{CCJTAG}, and V_{CCCNFG} have reached nominal voltage.
- V_{CC} pins can be powered up in any order. This includes V_{CC}, V_{CCIO}, V_{CCJTAG}, and V_{CCCNFG}.
- All V_{CCIO}s on a bank should be tied to the same potential and powered up together.
- All V_{CCIO}s (even the unused banks) need to be powered up to at least 1.5V before configuration has completed.
- Maximum ramp time for all V_{CC}s should be 0V to nominal voltage in 100 ms.

Note:

5. PCI spec (rev 2.2) requires the IDSEL pin to have capacitance less than or equal to 8 pF. Document titled “Quantum38K Pin Tables” identifies all the I/O pins, in a given package, which can be used as IDSEL in a PCI design. All other I/O pins meet the PCI requirement of capacitance less than or equal to 10pF.
6. The number of I/Os which can be used in each I/O bank depends on the type of I/O standards and the number of V_{CCIO} and GND pins being used. Please refer to the application note titled “Delta39K and Quantum38K Device I/O Standards and Configurations” for details.
   - The source current limit per I/O bank per Vccio pin is 165 mA
   - The sink current limit per I/O bank per GND pin is 230 mA

Switching Characteristics - Parameter Descriptions Over the Operating Range [7]

Parameter	Description
Combinatorial Mode Parameters	
t_{PD}	Delay from any pin input, through any cluster on the channel associated with that pin input, to any pin output on the horizontal or vertical channel associated with that cluster
t_{EA}	Global control to output enable
t_{ER}	Global control to output disable
t_{PRR}	Asynchronous macrocell RESET or PRESET recovery time from any pin input on the horizontal or vertical channel associated with the cluster the macrocell is in
t_{PRO}	Asynchronous macrocell RESET or PRESET from any pin input on the horizontal or vertical channel associated with the cluster that the macrocell is in to any pin output on those same channels
t_{PRW}	Asynchronous macrocell RESET or PRESET minimum pulse width, from any pin input to a macrocell in the farthest cluster on the horizontal or vertical channel the pin is associated with
Synchronous Clocking Parameters	
t_{MCS}	Set-up time of any input pin to a macrocell in any cluster on the channel associated with that input pin, relative to a global clock
t_{MCH}	Hold time of any input pin to a macrocell in any cluster on the channel associated with that input pin, relative to a global clock
t_{MCCO}	Global clock to output of any macrocell to any output pin on the horizontal or vertical channel associated with the cluster that macrocell is in
t_{IOS}	Set-up time of any input pin to the I/O cell register associated with that pin, relative to a global clock
t_{IOH}	Hold time of any input pin to the I/O cell register associated with that pin, relative to a global clock
t_{IOCO}	Clock to output of an I/O cell register to the output pin associated with that register
t_{SCS}	Macrocell clock to macrocell clock through array logic within the same cluster
t_{SCS2}	Macrocell clock to macrocell clock through array logic in different clusters on the same channel
t_{ICS}	I/O register clock to any macrocell clock in a cluster on the channel the I/O register is associated with
t_{OCS}	Macrocell clock to any I/O register clock on the horizontal or vertical channel associated with the cluster that the macrocell is in
t_{CHZ}	Clock to output disable (high-impedance)
t_{CLZ}	Clock to output enable (low-impedance)
f_{MAX}	Maximum frequency with internal feedback—within the same cluster
f_{MAX2}	Maximum frequency with internal feedback—within different clusters at the opposite ends of a horizontal or vertical channel
Product Term Clock	
t_{MCSPT}	Set-up time for macrocell used as input register, from input to product term clock
t_{MCHPT}	Hold time of macrocell used as an input register
t_{MCCOPT}	Product term clock to output delay from input pin
t_{SCS2PT}	Register to register delay through array logic in different clusters on the same channel using a product term clock
Channel Interconnect Parameters	
t_{CHSW}	Adder for a signal to switch from a horizontal to vertical channel and vice-versa
t_{CL2CL}	Cluster to Cluster delay adder (through channels and channel PIM)

Note:
7. Add t_{CHSW} to signals making a horizontal to vertical channel switch or vice-versa.

Switching Characteristics - Parameter Descriptions Over the Operating Range [7] (continued)

Parameter	Description
Miscellaneous Delays	
t_{CPLD}	Delay from the input of a cluster PIM, through a macrocell in the cluster, back to a cluster PIM input. This parameter can be added to the t_{PD} and t_{SCS} parameters for each extra pass through the AND/OR array required by a given signal path
t_{MCCD}	Adder for carry chain logic per macrocell
t_{IOD}	Delay from the input of the output buffer to the I/O pin
t_{IOIN}	Delay from the I/O pin to the input of the channel buffer
t_{CKIN}	Delay from the clock pin to the input of the clock driver
$t_{IOREGPIN}$	Delay from the I/O pin to the input of the I/O register
JTAG Parameters	
t_{JCKH}	TCLK HIGH time
t_{JCKL}	TCLK LOW time
t_{JCP}	TCLK clock period
t_{JSU}	JTAG port set-up time (TDI/TMS inputs)
t_{JH}	JTAG port hold time (TDI/TMS inputs)
t_{JCO}	JTAG port clock to output time (TDO)
t_{JXZ}	JTAG port valid output to high impedance (TDO)
t_{JZX}	JTAG port high impedance to valid output (TDO)

Channel Memory Timing Parameter Descriptions Over the Operating Range

Parameter	Description
Dual Port Asynchronous Mode Parameters	
t_{CHMAA}	Channel memory access time. Delay from address change to read data out
t_{CHMPWE}	Write enable pulse width
t_{CHMSA}	Address set-up to the beginning of write enable
t_{CHMHA}	Address hold after the end of write enable with both signals from the same I/O block
t_{CHMSD}	Data set-up to the end of write enable
t_{CHMHD}	Data hold after the end of write enable
t_{CHMBA}	Channel memory asynchronous dual port address match (busy access time)
Dual Port Synchronous Mode Parameters	
$t_{CHMCYC1}$	Clock cycle time for flow through read and write operations (from macrocell register through channel memory back to a macrocell register in the same cluster)
$t_{CHMCYC2}$	Clock cycle time for pipelined read and write operations (from channel memory input register through the memory to channel memory output register)
t_{CHMS}	Address, data, and WE set-up time of pin inputs, relative to a global clock
t_{CHMH}	Address, data, and WE hold time of pin inputs, relative to a global clock
t_{CHMDV1}	Global clock to data valid on output pins for flow through data
t_{CHMDV2}	Global clock to data valid on output pins for pipelined data
t_{CHMBDV}	Channel memory synchronous dual-port address match (busy, clock to data valid)
$t_{CHMMACS1}$	Channel memory input clock to macrocell clock in the same cluster
$t_{CHMMACS2}$	Channel memory output clock to macrocell clock in the same cluster
$t_{MACCHMS1}$	Macrocell clock to channel memory input clock in the same cluster
$t_{MACCHMS2}$	Macrocell clock to channel memory output clock in the same cluster
Internal Parameters	
$t_{CHMCHAA}$	Asynchronous channel memory access time from input of channel memory to output of channel memory

Switching Characteristics - Parameter Values Over the Operating Range

Parameter	83		66		Unit
	Min.	Max.	Min.	Max.	
Combinatorial Mode Parameters					
t_{PD}		15		18.9	ns
t_{EA}		10		12.6	ns
t_{ER}		10		12.6	ns
t_{PRR}	10		12.6		ns
t_{PRO}	15		18.9		ns
t_{PRW}	7.0		8.8		ns
Synchronous Clocking Parameters					
t_{MCS}	6.0		7.5		ns
t_{MCH}	0.0		0.0		ns
t_{MCCO}		12		15	ns
t_{IOS}	2.5		3.1		ns
t_{IOH}	2.5		3.1		ns
t_{IOCO}		8.0		10	ns
t_{SCS}	9.6		12.1		ns
t_{SCS2}	12		15		ns
t_{ICS}	12		15		ns
t_{OCS}	12		15		ns
t_{CHZ}		7.0		8.8	ns
t_{CLZ}	2.0		2.0		ns
f_{MAX}		104		83	MHz
f_{MAX2}		83		66	MHz
Product Term Clocking Parameters					
t_{MCSPT}	6.0		7.5		ns
t_{MCHPT}	2.5		3.1		ns
t_{MCCOPT}		15.0		18.9	ns
t_{SCS2PT}	15.0		18.9		ns
Channel Interconnect Parameters					
t_{CHSW}		2.0		2.5	ns
t_{CL2CL}		3.0		3.8	ns
Miscellaneous Parameters					
t_{CPLD}		5.0		6.3	ns
t_{MCCD}		0.38		0.48	ns

Switching Characteristics - Parameter Values Over the Operating Range (continued)

Parameter	83		66		Unit
	Min.	Max.	Min.	Max.	
JTAG Parameters					
t_{JCKH}	25		25		ns
t_{JCKL}	25		25		ns
t_{JCP}	50		50		ns
t_{JSU}	10		10		ns
t_{JH}	10		10		ns
t_{JCO}		20		20	ns
t_{JXZ}		20		20	ns
t_{JZX}		20		20	ns

Input & Output Standard Timing Delay Adjustments

All the timing specifications in this data sheet are specified based on 3.3V PCI compliant inputs and outputs (fast slew rates[8]). Apply the following adjustments if the inputs and outputs are configured to operate at the following standards:

Input/Output Standard	Output Delay Adjustments			Input Delay Adjustments		
	t_{IOD}	t_{EA}	t_{ER}	t_{IOIN}	t_{CKIN}	$t_{IOREGPIN}$
LVTTL – 2 mA	0.2	0	0	0	0	0
LVTTL – 4 mA	2.6	0	0	0	0	0
LVTTL – 6 mA	2.0	0	0	0	0	0
LVTTL – 8 mA	1.2	0	0	0	0	0
LVTTL – 12 mA	1.0	0	0	0	0	0
LVTTL – 16 mA	0.5	0	0	0	0	0
LVTTL – 24 mA	0.2	0	0	0	0	0
LVCMOS	0.2	0	0	0	0	0
LVCMOS3	0.3	0.05	0	0.1	0.1	0.2
LVCMOS2	0.5	0.1	0	0.2	0.2	0.4
LVCMOS18	2.1	0.7	0.1	0.5	0.4	0.3
3.3V PCI	0	0	0	0	0	0

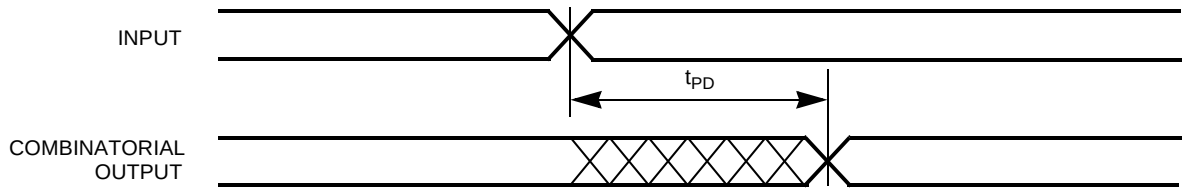
Note:
8. For “slow slew rate” output delay adjustments, refer to *Warp* software’s static timing analyzer results.

Channel Memory Timing Parameter Values

Parameter	83		66		Unit
	Min.	Max.	Min.	Max.	
Dual-Port Asynchronous Mode Parameters					
t_{CHMAA}		20		25	ns
t_{CHMPWE}	12		15		ns
t_{CHMSA}	4.0		5.0		ns
t_{CHMHA}	2.0		2.5		ns
t_{CHMSD}	12		5.0		ns
t_{CHMHD}	1.0		1.3		ns
t_{CHMBA}		16.0		20.1	ns
Dual-Port Synchronous Mode Parameters					
$t_{CHMCYC1}$	20		25		ns
$t_{CHMCYC2}$	10.6		13.3		ns
t_{CHMS}	6.0		7.5		ns
t_{CHMH}	0.0		0.0		ns
t_{CHMDV1}		20		25	ns
t_{CHMDV2}		15		19	ns
t_{CHMBDV}		16.0		20.1	ns
$t_{CHMMACS1}$	16.0		20.1		ns
$t_{CHMMACS2}$	10		12.6		ns
$t_{MACCHMS1}$	9.0		11.3		ns
$t_{MACCHMS2}$	13.0		16.3		ns
Internal Parameters					
$t_{CHMCHAA}$	13.0		16.3		ns

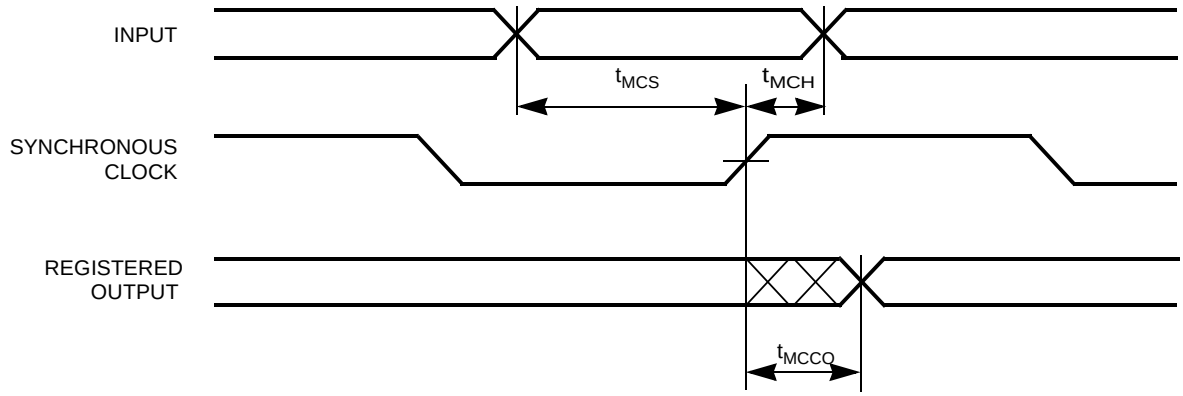
Switching Waveforms

Combinatorial Output



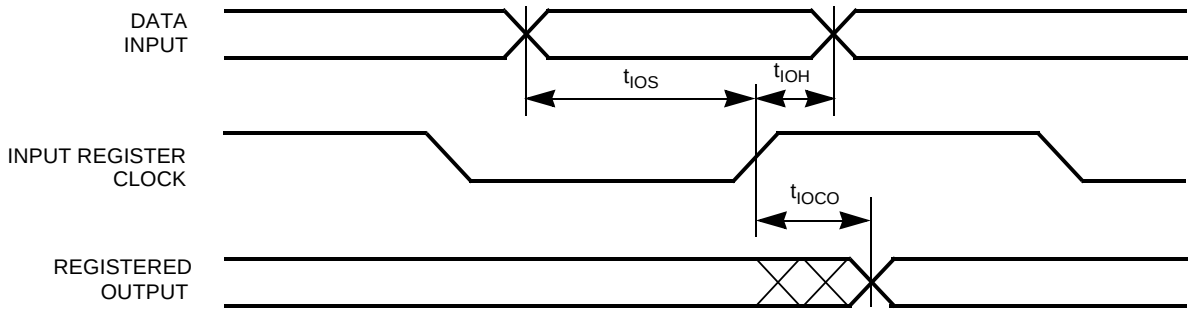
Quantum38K-1

Registered Output with Synchronous Clocking (Macrocell)



Quantum38K-2

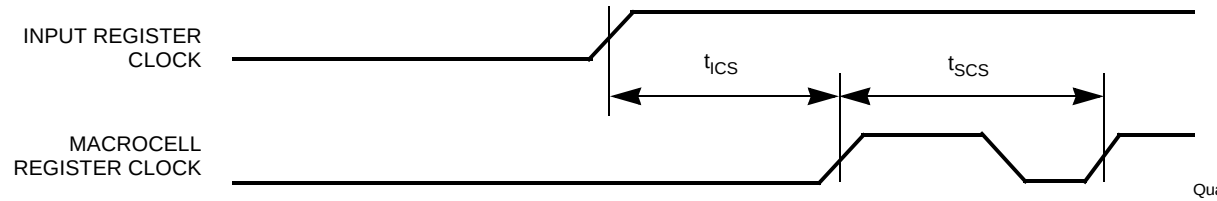
Registered Input in I/O Cell



Quantum38K-3

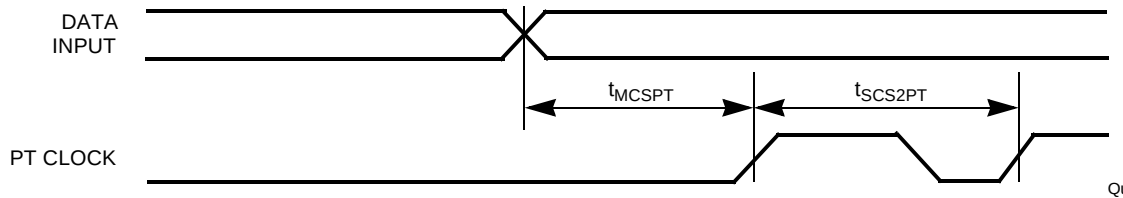
Switching Waveforms (continued)

Clock to Clock



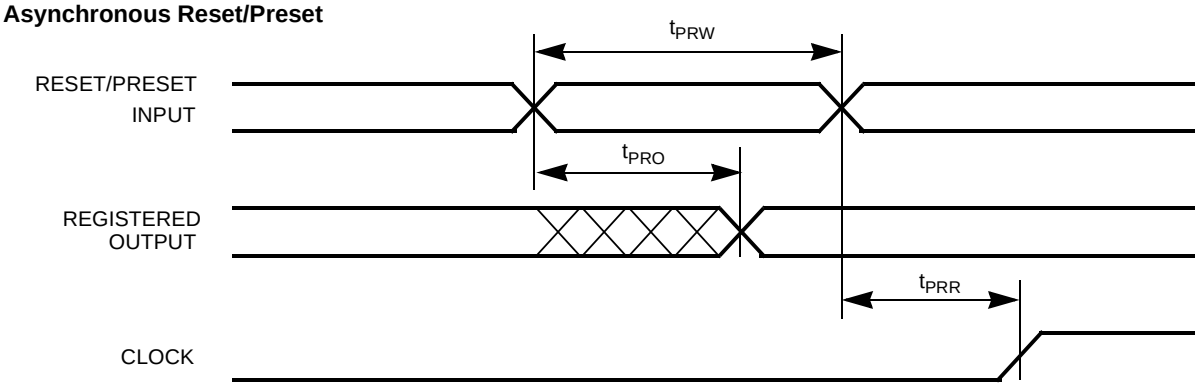
Quantum38K-4

PT Clock to PT Clock



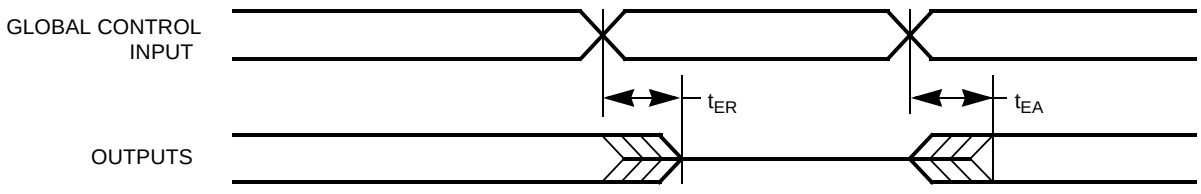
Quantum38K-5

Asynchronous Reset/Preset



Quantum38K-6

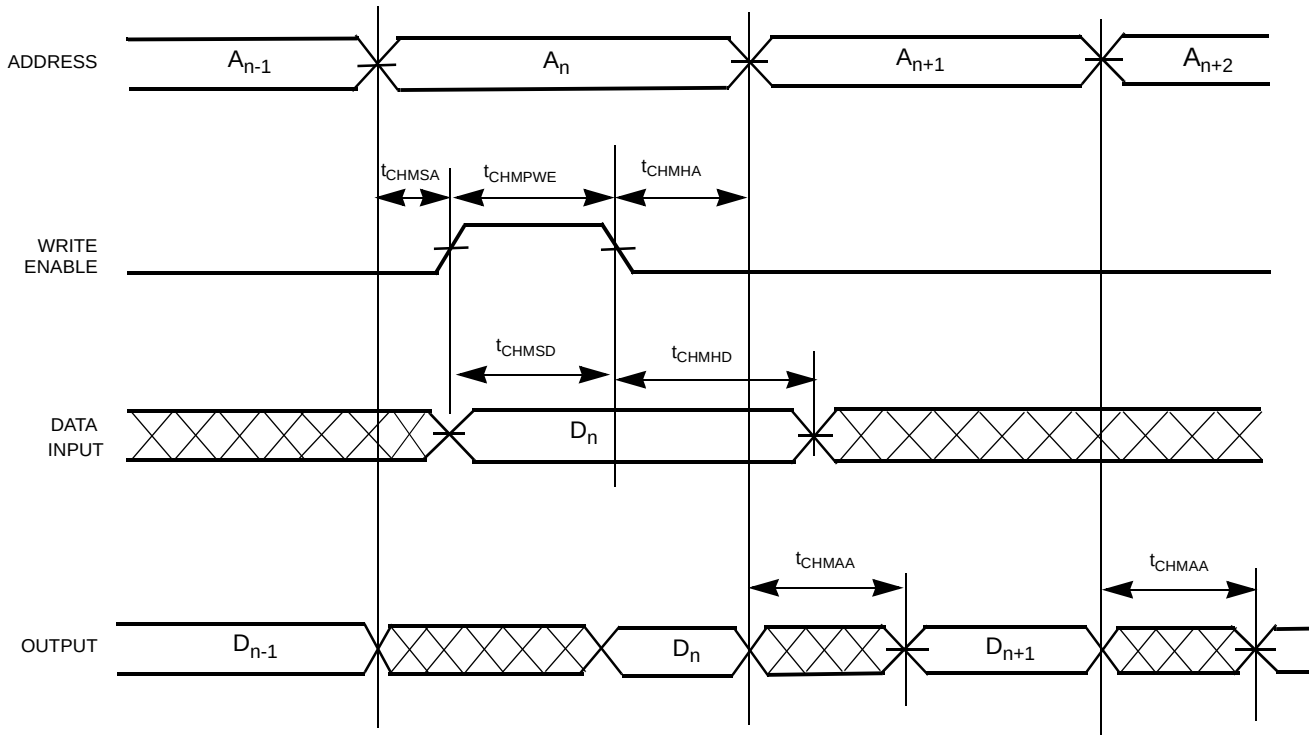
Output Enable/Disable



Quantum38K-7

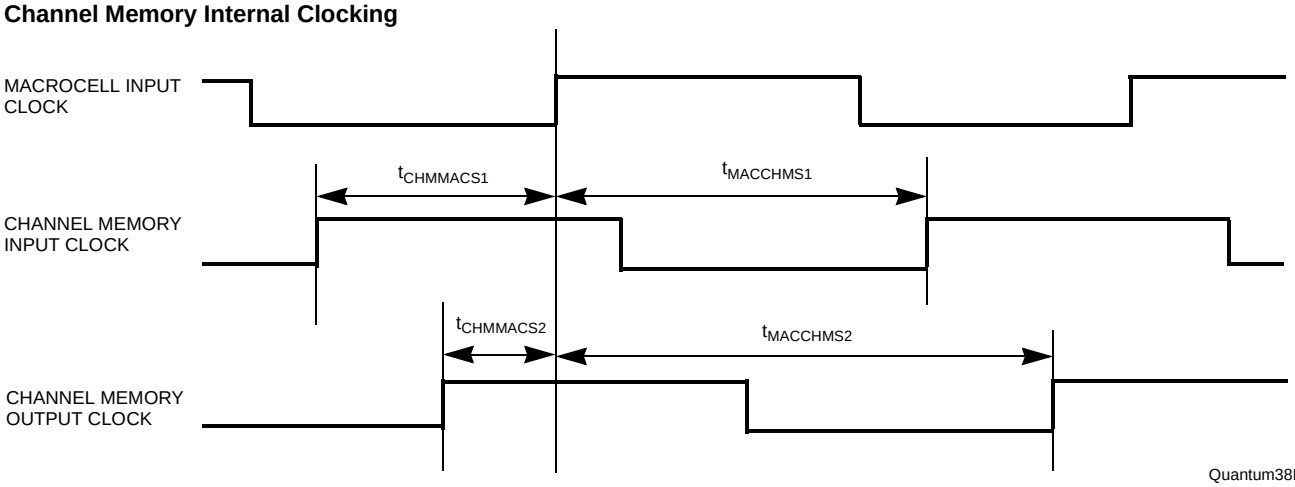
Switching Waveforms (continued)

Channel Memory DP Asynchronous Timing



Quantum38K-8

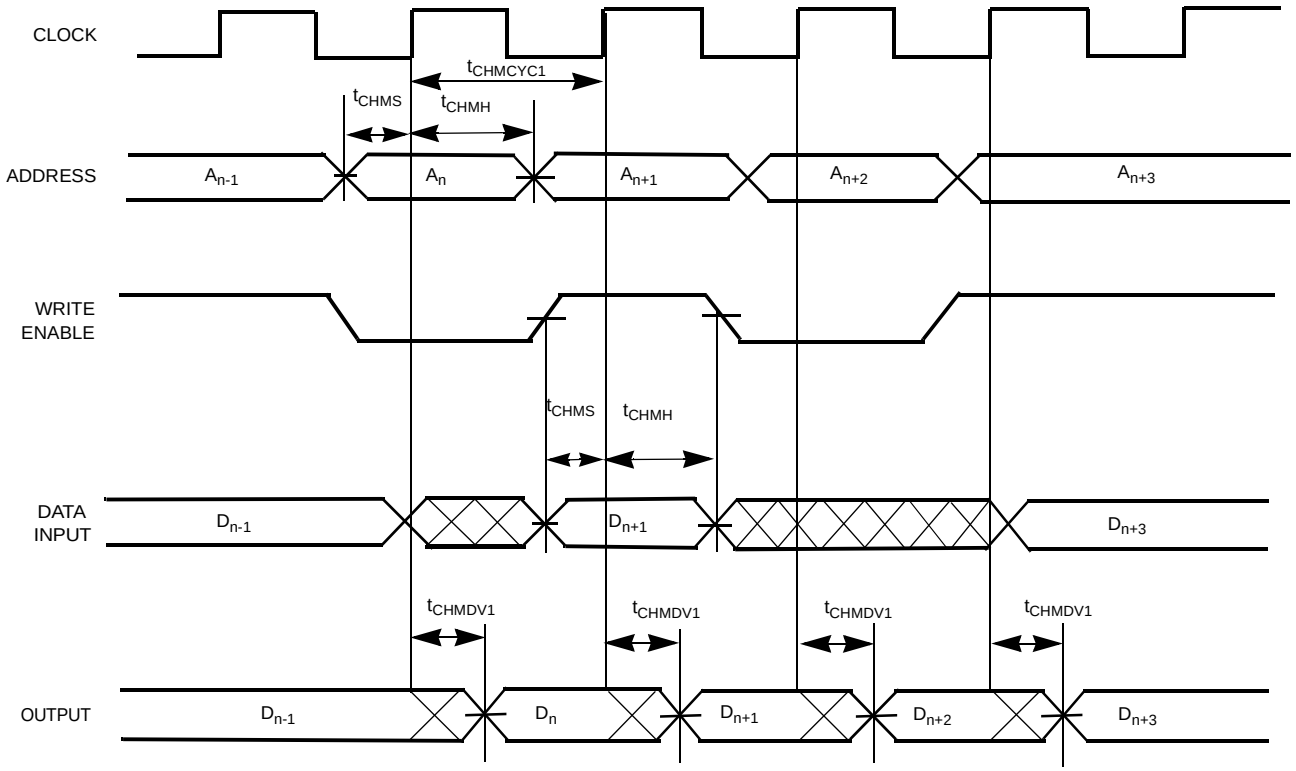
Channel Memory Internal Clocking



Quantum38K-9

Switching Waveforms (continued)

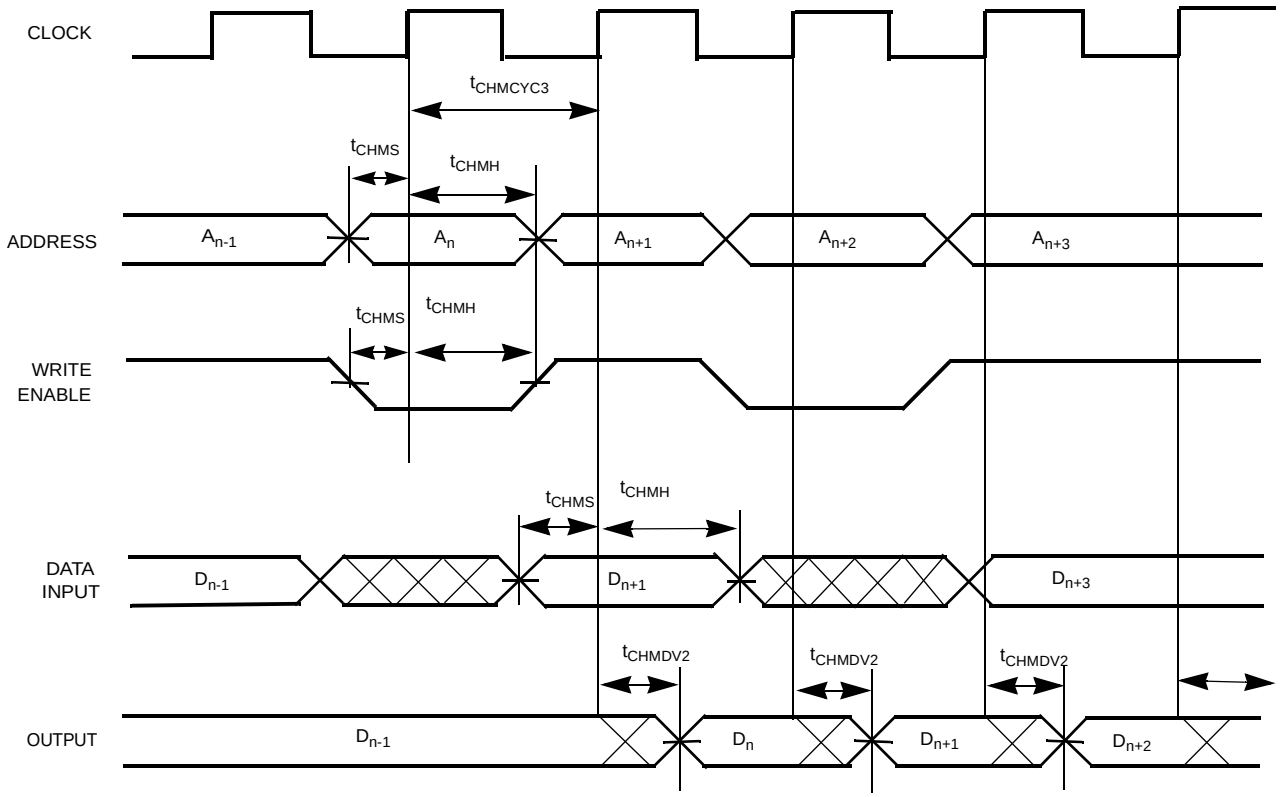
Channel Memory DP SRAM Flow Through R/W Timing



Quantum38K-10

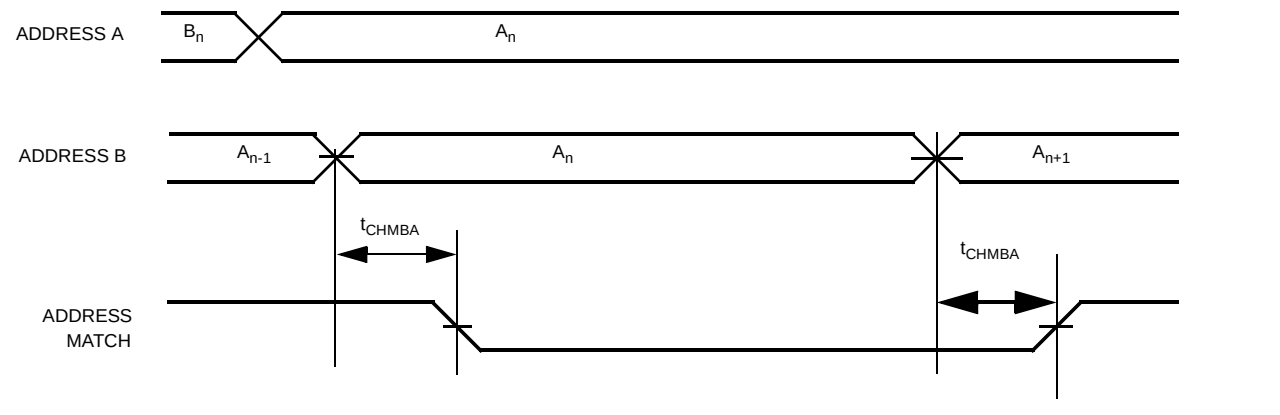
Switching Waveforms (continued)

Channel Memory DP SRAM Pipeline R/W Timing



Quantum38K-11

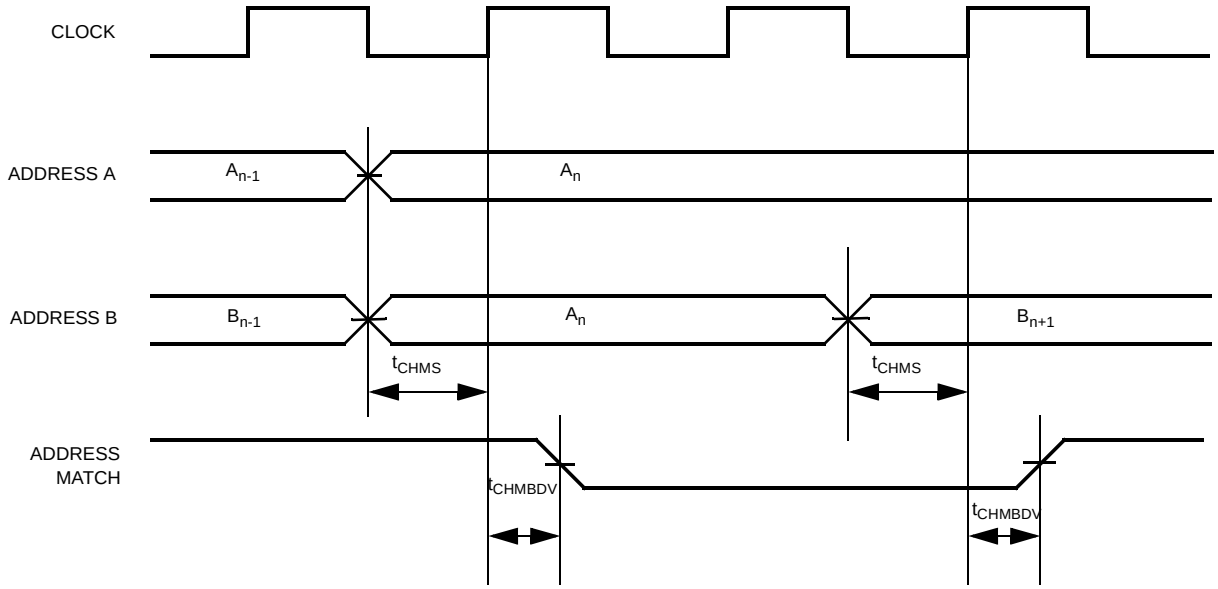
Dual-Port Asynchronous Address Match Busy Signal



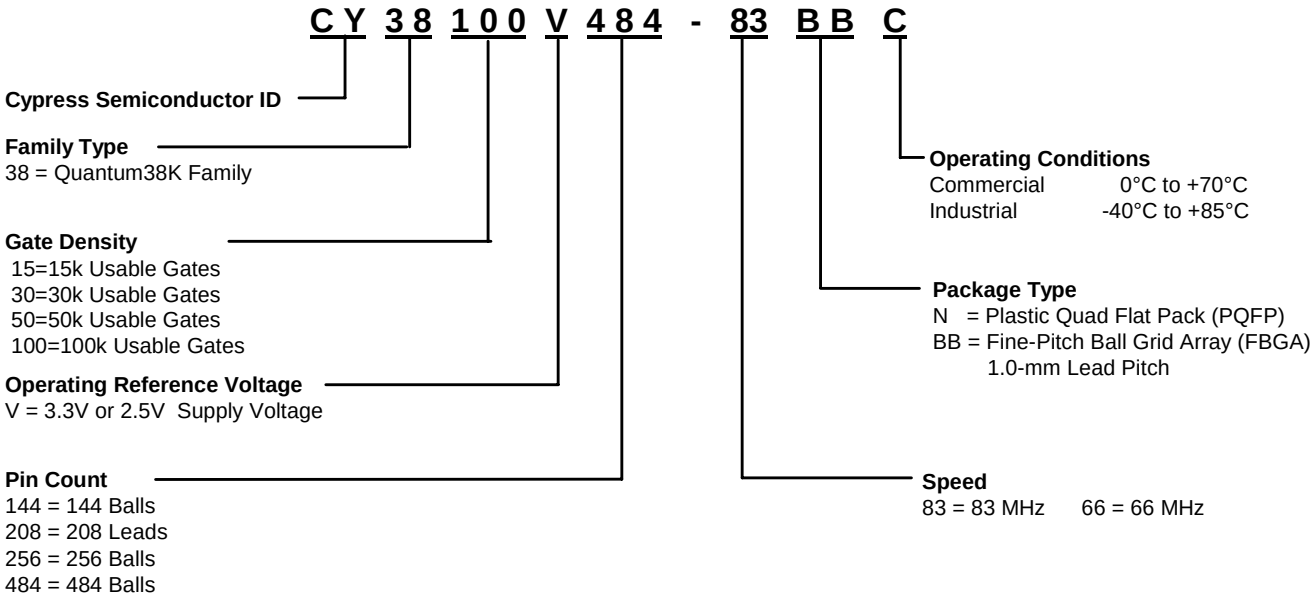
Quantum38K-12

Switching Waveforms (continued)

Dual-Port Synchronous Address Match Busy Signal



Quantum38K-13



Quantum38K Pin Table

Please refer to the document titled “Quantum38K Pin Tables” for pinouts of all the packages of all Quantum38K family members. You can access this document on the internet at: http://www.cypress.com/pld/datasheets.html.

Quantum38K Part Numbers (Ordering Information)

Device	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
38K15	66	CY38015V208-66NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY38015V144-66BBC	BB144	144-Lead Fine Pitch Ball Grid Array	
		CY38015V256-66BBC	BB256	256-Lead Fine Pitch Ball Grid Array	
		CY38015V208-66NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY38015V144-66BBI	BB144	144-Lead Fine Pitch Ball Grid Array	
		CY38015V256-66BBI	BB256	256-Lead Fine Pitch Ball Grid Array	
38K15	83	CY38015V208-83NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY38015V144-83BBC	BB144	144-Lead Fine Pitch Ball Grid Array	
		CY38015V256-83BBC	BB256	256-Lead Fine Pitch Ball Grid Array	
		CY38015V208-83NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY38015V144-83BBI	BB144	144-Lead Fine Pitch Ball Grid Array	
		CY38015V256-83BBI	BB256	256-Lead Fine Pitch Ball Grid Array	
38K30	66	CY38030V208-66NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY38030V144-66BBC	BB144	144-Lead Fine Pitch Ball Grid Array	
		CY38030V256-66BBC	BB256	256-Lead Fine Pitch Ball Grid Array	
		CY38030V208-66NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY38030V144-66BBI	BB144	144-Lead Fine Pitch Ball Grid Array	
		CY38030V256-66BBI	BB256	256-Lead Fine Pitch Ball Grid Array	

Quantum38K Part Numbers (Ordering Information) (continued)

Device	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
38K30	83	CY38030V208-83NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY38030V144-83BBC	BB144	144-Lead Fine Pitch Ball Grid Array	
		CY38030V256-83BBC	BB256	256-Lead Fine Pitch Ball Grid Array	
		CY38030V208-83NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY38030V144-83BBI	BB144	144-Lead Fine Pitch Ball Grid Array	
		CY38030V256-83BBI	BB256	256-Lead Fine Pitch Ball Grid Array	
38K50	66	CY38050V208-66NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY38050V256-66BBC	BB256	256-Lead Fine Pitch Ball Grid Array	
		CY38050V484-66BBC	BB484	484-Lead Fine Pitch Ball Grid Array	
		CY38050V208-66NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY38050V256-66BBI	BB256	256-Lead Fine Pitch Ball Grid Array	
		CY38050V484-66BBI	BB484	484-Lead Fine Pitch Ball Grid Array	
38K50	83	CY38050V208-83NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY38050V256-83BBC	BB256	256-Lead Fine Pitch Ball Grid Array	
		CY38050V484-83BBC	BB484	484-Lead Fine Pitch Ball Grid Array	
		CY38050V208-83NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY38050V256-83BBI	BB256	256-Lead Fine Pitch Ball Grid Array	
		CY38050V484-83BBI	BB484	484-Lead Fine Pitch Ball Grid Array	
38K100[9]	66	CY38100V208-66NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY38100V256-66BBC	BB256	256-Lead Fine Pitch Ball Grid Array	
		CY38100V484-66BBC	BB484	484-Lead Fine Pitch Ball Grid Array	
		CY38100V208-66NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY38100V256-66BBI	BB256	256-Lead Fine Pitch Ball Grid Array	
		CY38100V484-66BBI	BB484	484-Lead Fine Pitch Ball Grid Array	
		CY38100V208B-66NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY38100V256B-66BBC	BB256	256-Lead Fine Pitch Ball Grid Array	
		CY38100V484B-66BBC	BB484	484-Lead Fine Pitch Ball Grid Array	
		CY38100V208B-66NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY38100V256B-66BBI	BB256	256-Lead Fine Pitch Ball Grid Array	
		CY38100V484B-66BBI	BB484	484-Lead Fine Pitch Ball Grid Array	
38K100[9]	83	CY38100V208-83NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY38100V256-83BBC	BB256	256-Lead Fine Pitch Ball Grid Array	
		CY38100V484-83BBC	BB484	484-Lead Fine Pitch Ball Grid Array	
		CY38100V208-83NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY38100V256-83BBI	BB256	256-Lead Fine Pitch Ball Grid Array	
		CY38100V484-83BBI	BB484	484-Lead Fine Pitch Ball Grid Array	
		CY38100V208B-83NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY38100V256B-83BBC	BB256	256-Lead Fine Pitch Ball Grid Array	
		CY38100V484B-83BBC	BB484	484-Lead Fine Pitch Ball Grid Array	
		CY38100V208B-83NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY38100V256B-83BBI	BB256	256-Lead Fine Pitch Ball Grid Array	
		CY38100V484B-83BBI	BB484	484-Lead Fine Pitch Ball Grid Array	

9. Refer to the section titled “Quantum38K100 Revisions” below

Quantum38K100 Revisions/Errata

Two revisions of Quantum38K100 are currently offered which are marked as CY38100Vxxx and CY38100VxxxB. CY38100VxxxB devices operate exactly as specified in this datasheet. Following is the operation of the CY38100Vxxx parts:

1. The internal regulator takes several seconds to power down. Hence, cycling the power supply (within 8 seconds) may cause a high standby current (200 mA to 1A) until the part is configured.
2. The part always configures on power-up and will reconfigure on HIGH to LOW edge of the *Reconfig* pin. Please refer to the application note titled "Configuring Delta39K/Quantum38K" for more details at http://www.cypress.com.
3. The *Self Config* instruction starts reconfiguring the CPLD upon execution of the *Update-IR* state of the JTAG TAP controller state machine. In CY38100VxxxB parts, *Self Config* instruction is executed upon execution of *Test-Logic-Reset* state of the TAP controller.
4. An ESD failure is very unlikely. CDM ESD passes 1000V. HBM ESD passes 3300V with all I/O bank's V_{CCIO} shorted together. If V_{CCIO}s in a bank are tested separately a percentage of parts will fail HBM ESD over 500V.

CPLD Boot EEPROM [10] Part Numbers (Ordering Information)

CPLD Boot EEPROM Density	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
1Mbit	15	CY3LV010-10JC	20J	20-Lead Plastic Leaded Chip Carrier	Commercial
	10	CY3LV010-10JI	20J	20-Lead Plastic Leaded Chip Carrier	Industrial
512Kbit	15	CY3LV512-10JC	20J	20-Lead Plastic Leaded Chip Carrier	Commercial
	10	CY3LV512-10JI	20J	20-Lead Plastic Leaded Chip Carrier	Industrial

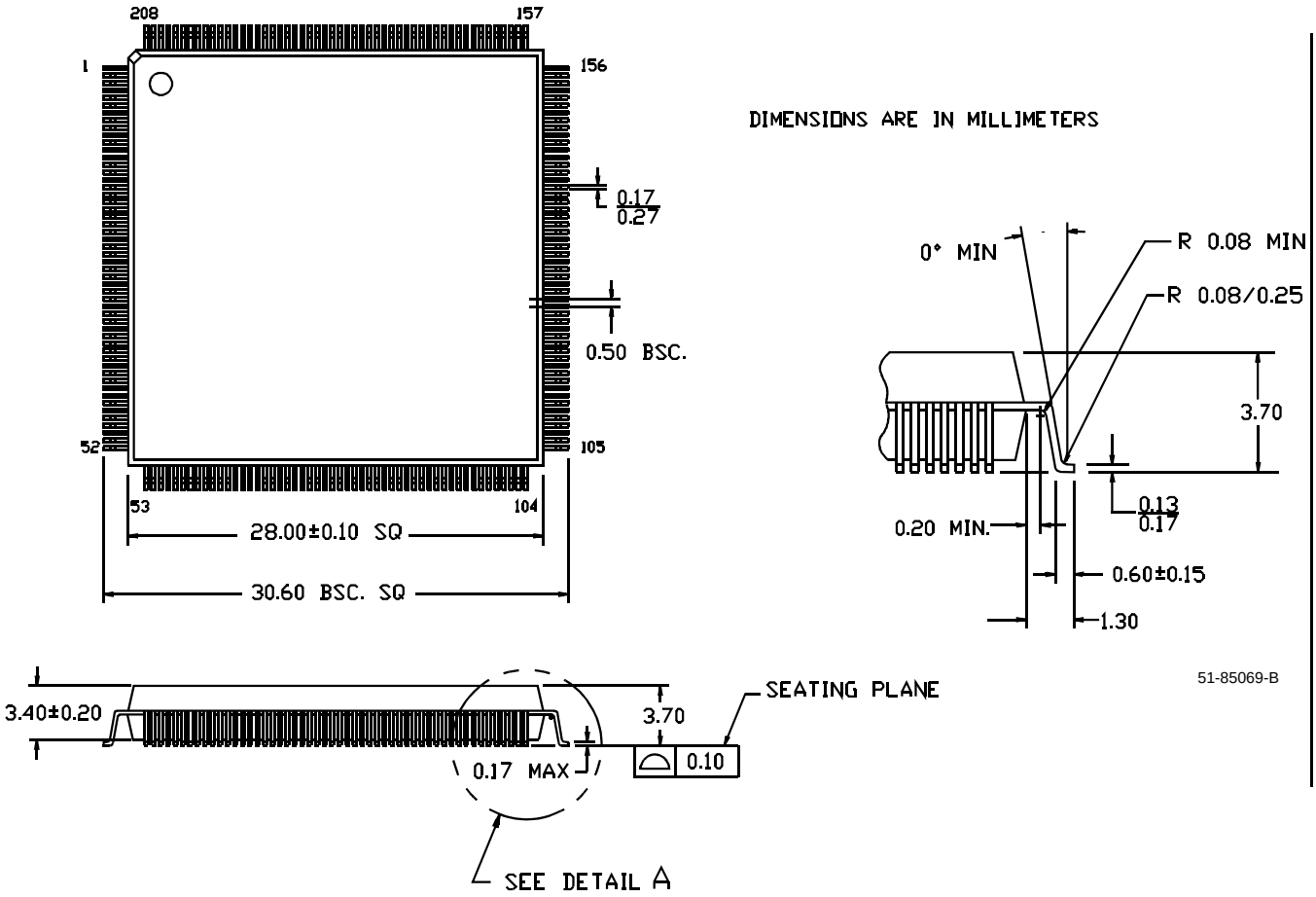
Recommended CPLD Boot EEPROM for Corresponding Quantum38K CPLDs

CPLD Device	Recommended Boot EEPROM
38K15	CY3LV256
38K30	CY3LV512
38K50	CY3LV512
38K100	CY3LV010

Note:
10. See the data sheet titled "CPLD Boot EEPROM" for detailed architectural and timing information.

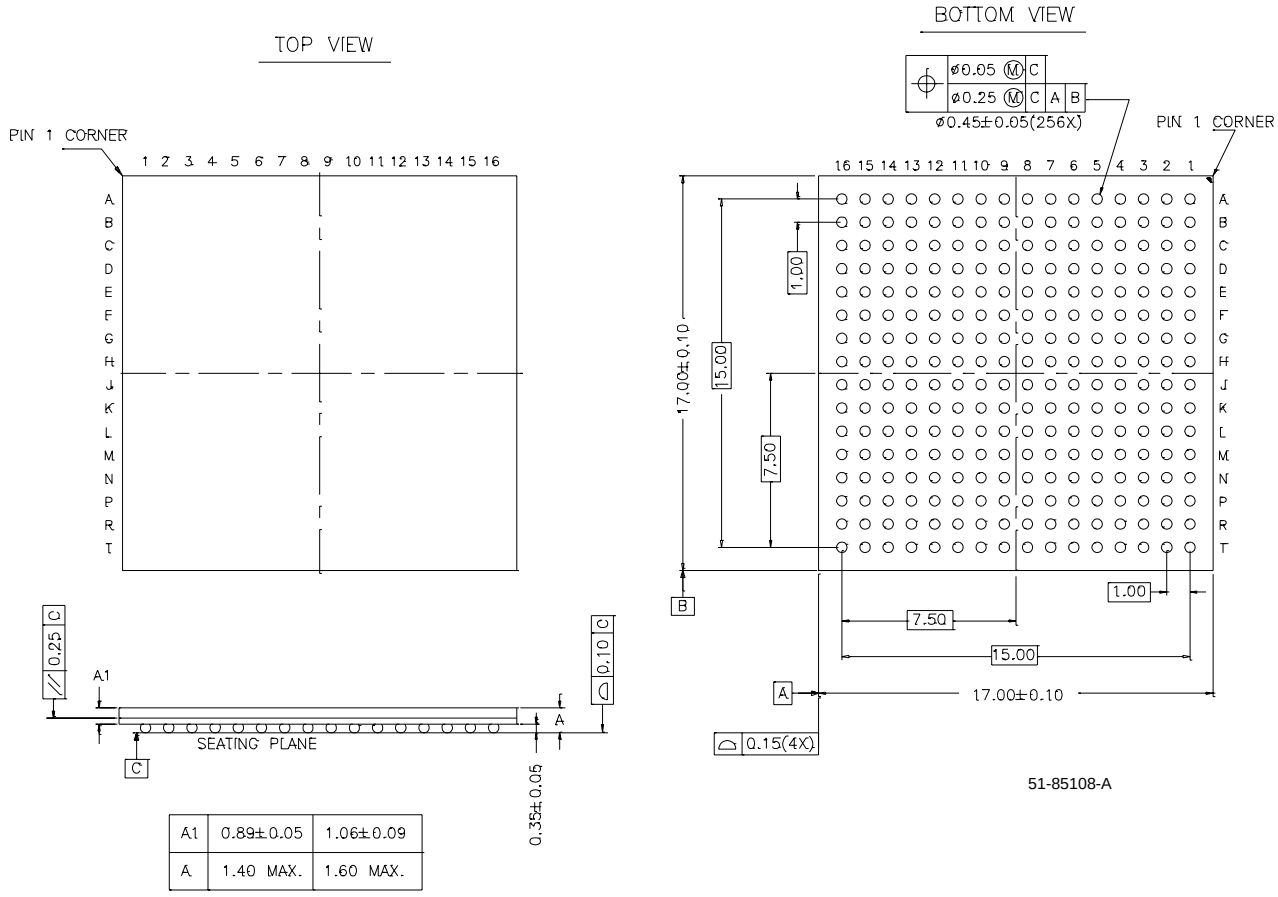
Package Diagrams

208-Lead Plastic Quad Flatpack (PQFP) N208



Package Diagrams (continued)

256-Ball Thin Ball Grid Array (17 x 17 x 1.6 mm) BB256/MB256

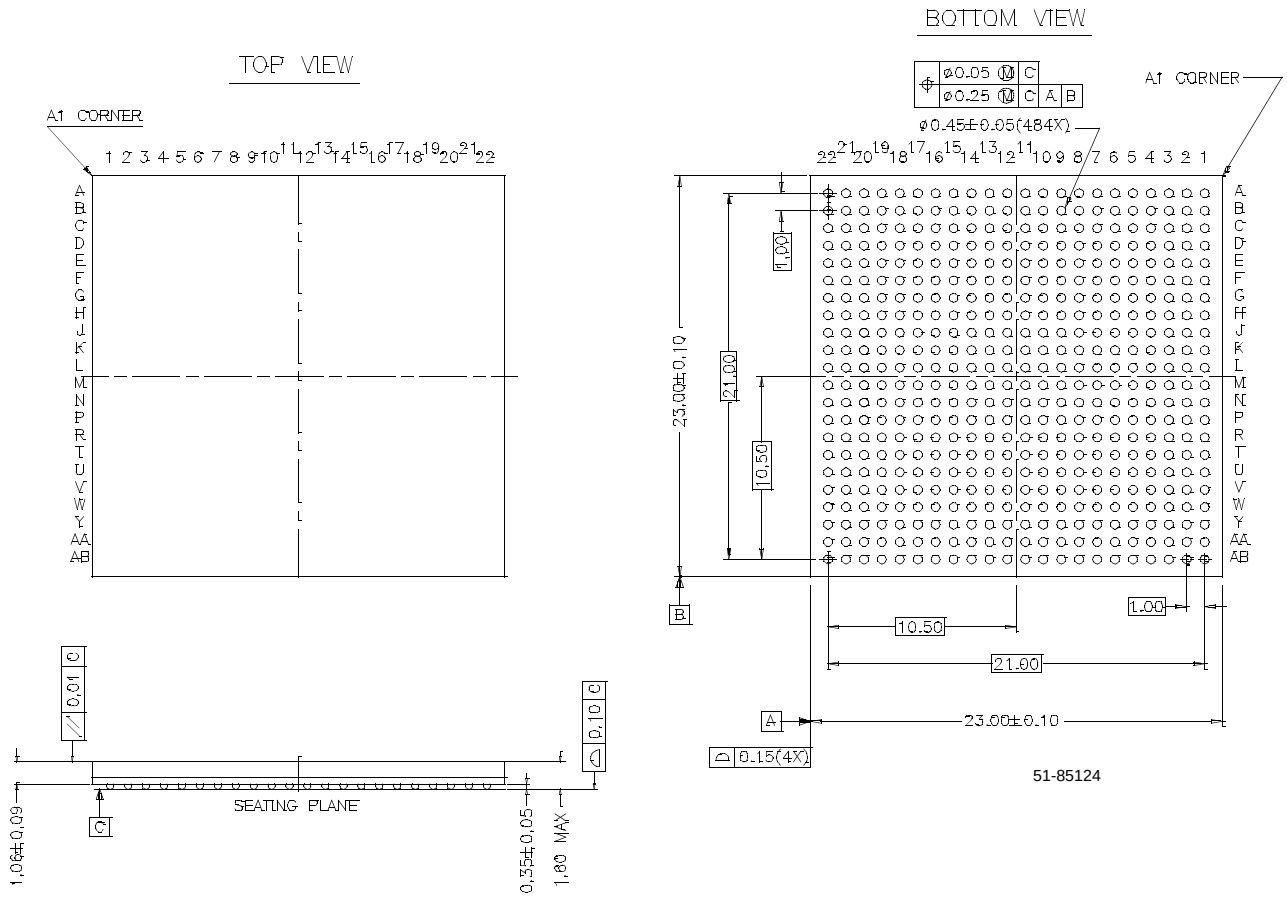


A1	0.89±0.05	1.06±0.09
A	1.40 MAX.	1.60 MAX.

51-85108-A

Package Diagrams (continued)

484-Ball Thin Ball Grid Array (23 x 23 x 1.6 mm) BB484/MB484



Mechanical drawings of 144-Ball FBGA will be available soon.
For package sizes and ball pitch see page 2.

Document Title: Quantum38K™ ISR™ CPLD Family CPLDs at ASIC Prices Document Number: 38-03043				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	106747	04/25/01	SZV	1. New Data Sheet 2. Convert from Spec number 38-01058 to 38-03043