TOSHIBA CMOS Digital Integrated Circuits Silicon Monolithic

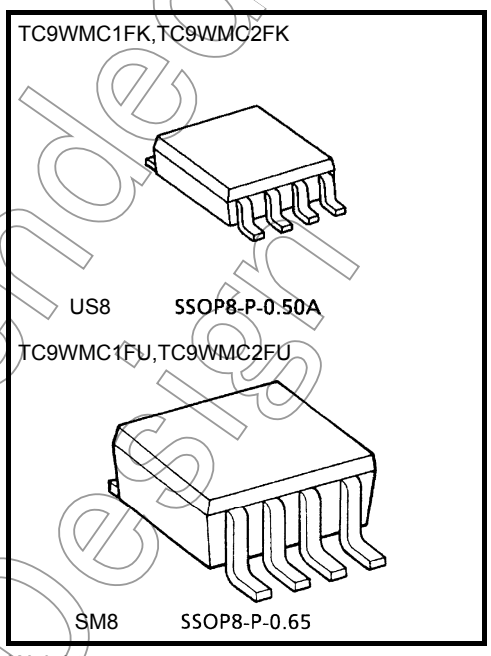
TC9WMC1FK,TC9WMC1FU,TC9WMC2FK,TC9WMC2FU

TC9WMC1FK/FU: 1024-Bit (64 × 16-Bit) 3-Wire Serial EEPROM
TC9WMC2FK/FU: 2048-Bit (128 × 16-Bit) 3-Wire Serial EEPROM

The TC9WMC1 and TC9WMC2 are electrically erasable/programmable three-wire serial nonvolatile memories (EEPROMs).

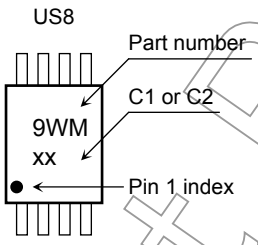
Features

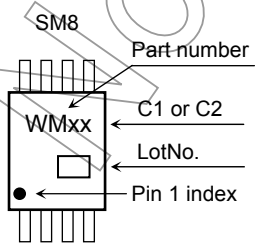
- Three-wire serial interface (MICROWIRE)
- Automatic address incrementing during read operation
- Hardware and software data protection
- READY/$\overline{\text{BUSY}}$ signal during programming
- Single power supply and low power consumption
  Read: V_{CC} = 1.8 to 3.6 V
  Write: V_{CC} = 2.3 to 3.6 V
- Wide operating temperature range (–40 to 85°C)



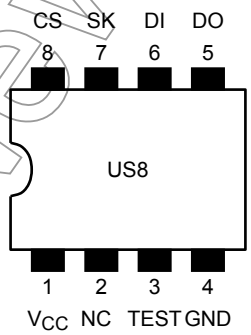
Weight:
SSOP8-P-0.50A: 0.01 g (typ.)
SSOP8-P-0.65: 0.02 g (typ.)

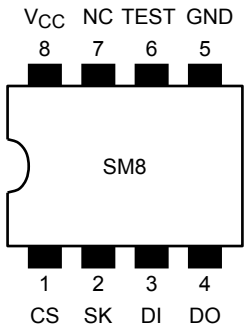
Product Marking





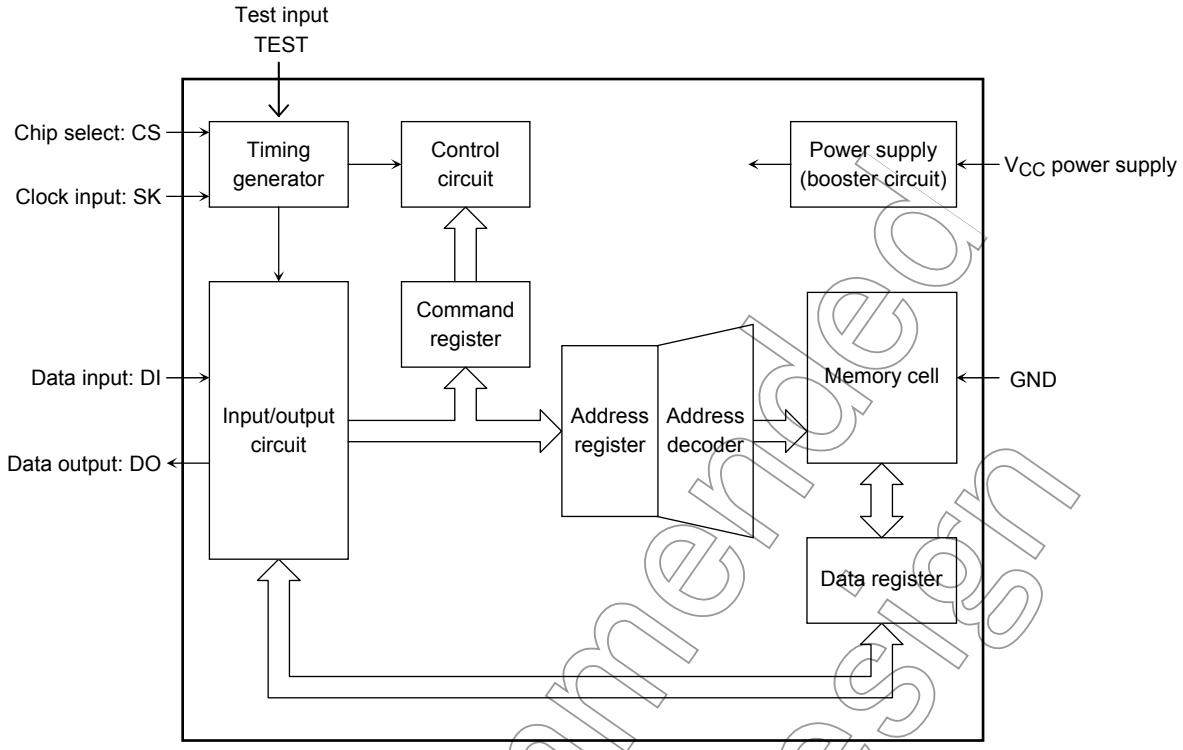
Pin Assignment (top view)





Not Recommended for New Design

Block Diagram



Pin Function

Pin Name	Input/Output	Function
CS	Input	Chip select input The device receives an instruction set when this pin is driven High. This pin must be driven Low before execution of an instruction.
SK	Input	Serial clock input Data is latched on the rising edge of SK. Data is transferred on the rising edge of SK. This pin is valid when CS is driven High.
DI	Input	Serial data input (start bit, op code, address and data)
DO	Output	Serial data output
TEST	Input	Test mode input (internal pull-down resistor) Normally kept open. (Can be connected to GND.)
NC	—	No connection (not connected internally)
V_{CC}	Power supply	1.8 to 3.6 V (for reading) 2.3 to 3.6 V (for writing)
GND		0 V (GND)

Not Recommended for New Design

1. Instruction Set

Instruction	Start Bit	Op Code	Address		Data
			TC9WMC1	TC9WMC2	
READ (Read)	1	10	A5 to A0	xA6 to A0	D15 to D0 outputs
WRITE (Write)	1	01	A5 to A0	xA6 to A0	D15 to D0 inputs
ERASE (Erase)	1	11	A5 to A0	xA6 to A0	—
WRAL (Write All)	1	00	01xxxx	01xxxxxx	D15 to D0 inputs
ERAL (Erase All)	1	00	10xxxx	10xxxxxx	—
EWEN (Program Enable)	1	00	11xxxx	11xxxxxx	—
EWDS (Program Disable)	1	00	00xxxx	00xxxxxx	—

x: Don't care

2. Functional Description

All instructions are executed when the DI input is received on the rising edge of SK after the CS input is driven High. An instruction starts with a start bit followed by an op code, address and data bits. The instruction transfer is completed when the CS input is driven Low. The CS must be driven Low during the tCS cycle period between instruction transfers. When the CS is Low, the device is in standby mode. The SK and DI inputs are disabled and the device does not respond to any instructions.

(1) Start bit

After the CS is driven High, a High on the DI input on the rising edge of SK indicates a start bit. A start bit is not identified if the DI is driven Low even after the CS is driven High and the SK pulse is applied.

Refer to (2) Dummy cycle in Section 3, Notes on Use.

(2) Read operation (READ)

The Read instruction reads data at specified addresses. After the CS is driven High, a start bit, READ instruction and address are transferred to the device. After the least significant bit of address (A0) is received, the DO output changes from high impedance to logic Low on the 9th rising edge of SK. On the 10th rising edge of SK, the 16 bits of data appear on the DO output.

(2.1) Sequential read

After the 16 bits of data are driven onto the DO output, the device will automatically increment the internal address counter and clock out data in the next memory location as long as the CS is held High and the SK pulse is applied. In this way, data in all the memory locations can be read in sequence. After the data in the last memory address is read, the address counter rolls over to the first memory address.

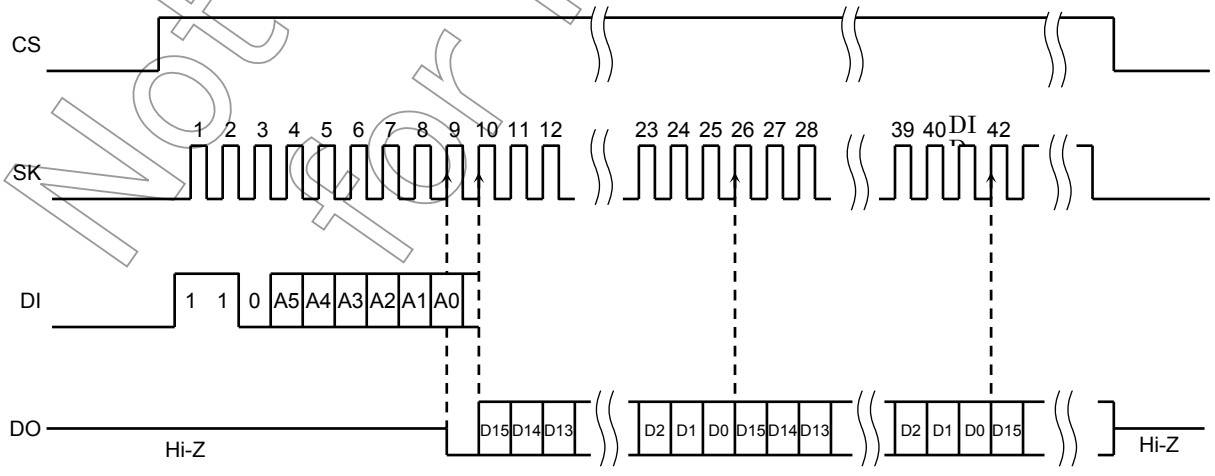


Figure 1. Read Timing Diagram (TC9WMC1)

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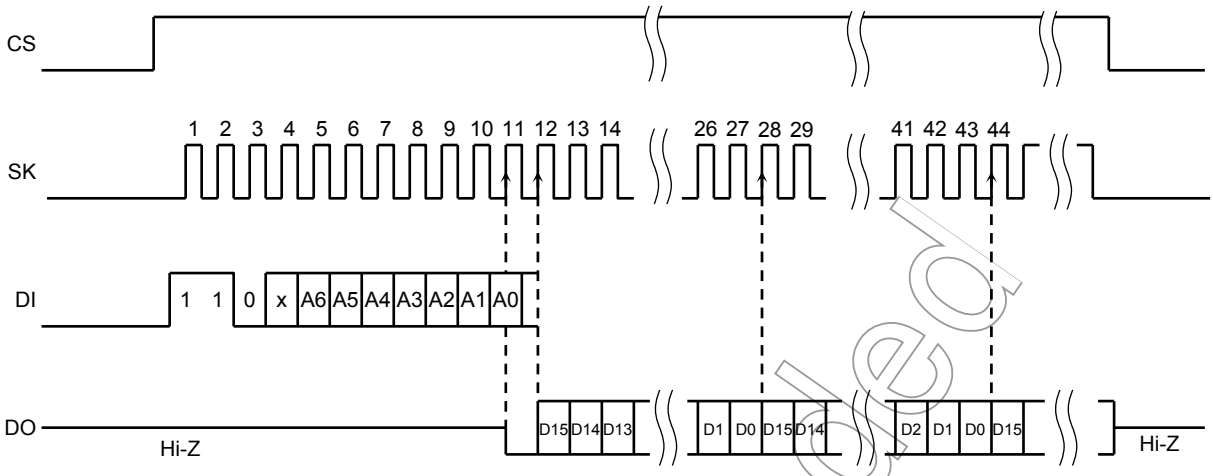

Figure 2. Read Timing Diagram (TC9WMC2)

(3) Write operation (WRITE, ERASE, WRAL, ERAL)

The write operation has four modes: Write (WRITE), Erase (ERASE), Write All (WRAL) and Erase All (ERAL). The write operation is triggered when the CS is driven Low after the SK pulse is applied. The SK and DI inputs are disabled during the write operation, so no attempt should be made to transfer instructions at this time.

If 16-bit or longer data is transferred to the device, the first 16 bits of data are valid and the remaining bits are ignored. The DO output must be held High or in the high-impedance state when a write instruction is received. A write operation is enabled in program enable mode.

(3.1) Verify operation

A write operation in all write modes is completed within 10 ms (write cycle tPW), but the typical write cycle is shorter (5 ms). If the completion of the write operation is known, the internal write cycle can be minimized. To accomplish this, a verify operation is performed.

(a) Operational description

When the CS is brought High following the initiation of a write operation (CS = Low), the write operation status can be seen by monitoring the DO pin. This is called a verify operation and the period during which the CS is held High following the initiation of a write operation is called a verify operation cycle.

- DO pin = Low: A write operation is in progress. (busy)
- DO pin = High: A write operation has been completed. (ready)

After the write operation is completed, and if a start bit is not identified, the DO pin goes to the high-impedance state if the CS is Low. If the CS is Low, the DO pin is driven High. When the write operation is in progress (busy), the SK and DI inputs are disabled. Once the write operation has been completed and a start bit is received, the verify operation is stopped.

(b) Two operation methods

There are two ways to perform a verify operation. One way is to monitor the DO output successively with the CS driven High until the DO output status changes. The other way is to monitor the DO output and, if no change is evident, the verify operation is stopped (CS = Low). The verify operation is then restarted by the CS being pulled High. In this way, when the DO output is not being monitored, the CPU is free for other operations, thus allowing more efficient design of electronic systems.

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(3.2) Write (WRITE)

The Write instruction contains the 16 bits of data to be written into the specified memory location. After the CS is driven High, a start bit is transferred followed by the WRITE instruction, address and 16 bits of data. After the least significant bit (D0) of data is received on the rising edge of SK, a write operation is triggered by the CS being pulled Low. It is not necessary to set every bit in the memory array to "1" before writing data.

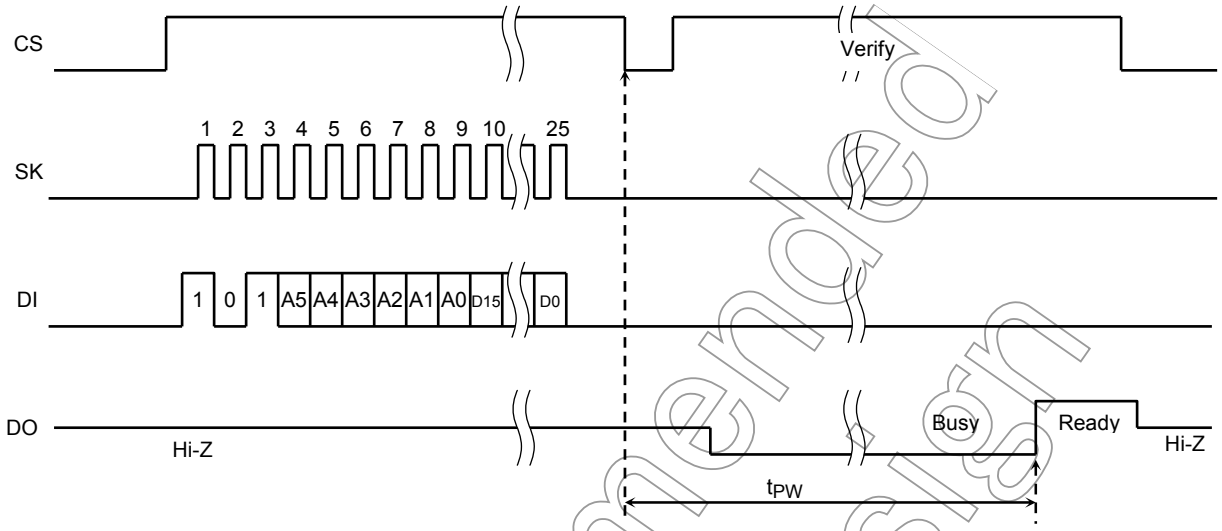

Figure 3. Write Timing Diagram (TC9WMC1)

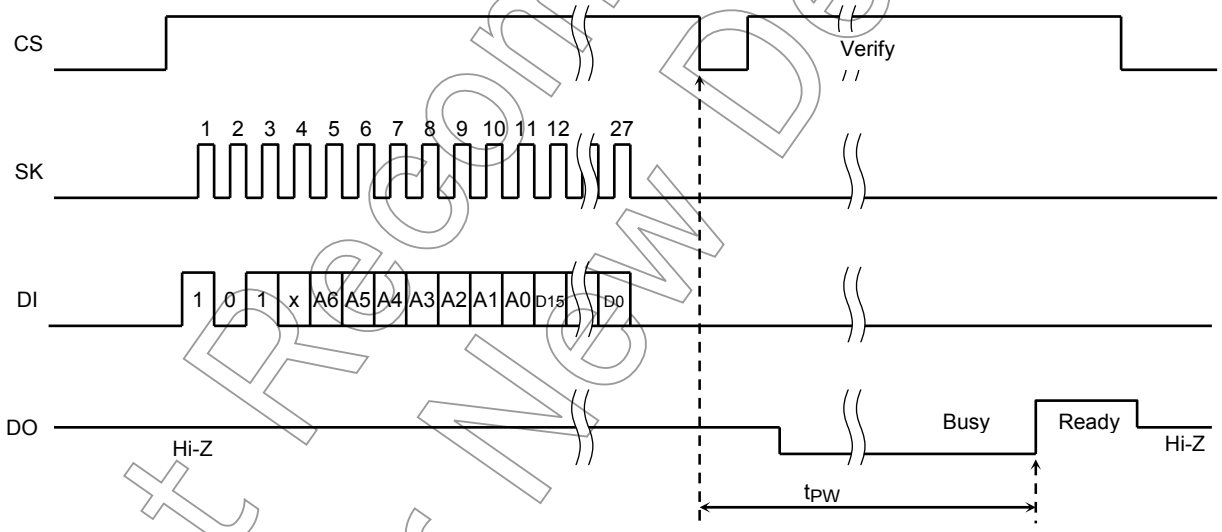

Figure 4. Write Timing Diagram (TC9WMC2)

Not Recommended for New Design

(3.3) Erase (ERASE)

The Erase instruction writes all bits in the specified memory location to 1. After the CS is driven High, a start bit is transferred followed by the ERASE instruction and address. In this mode, data does not need to be transferred. After the least significant bit (A0) of the address is received on the falling edge of SK, an erase operation is triggered by the CS being pulled Low.

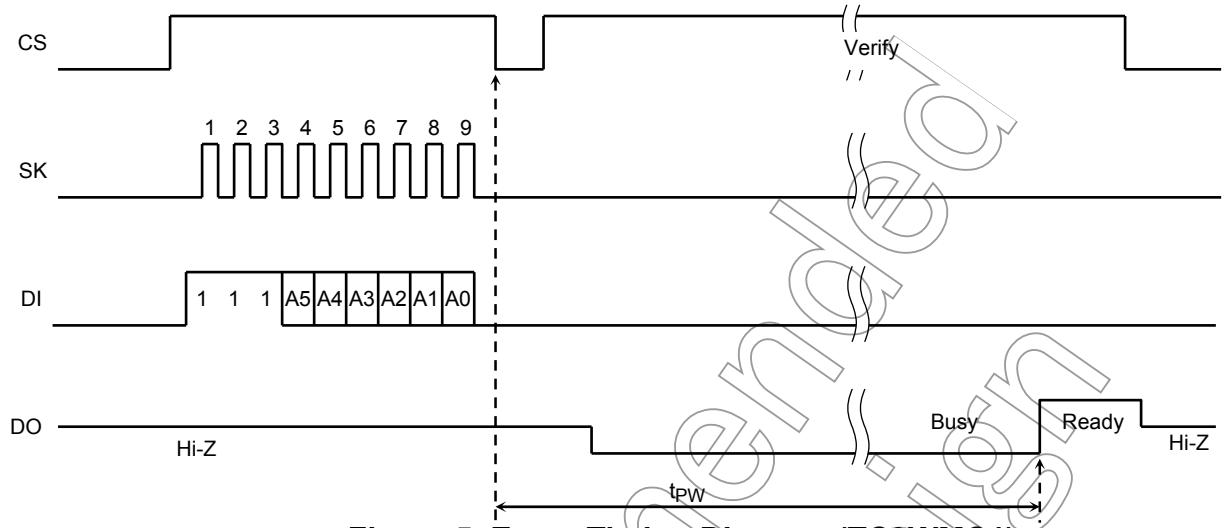

Figure 5. Erase Timing Diagram (TC9WMC1)

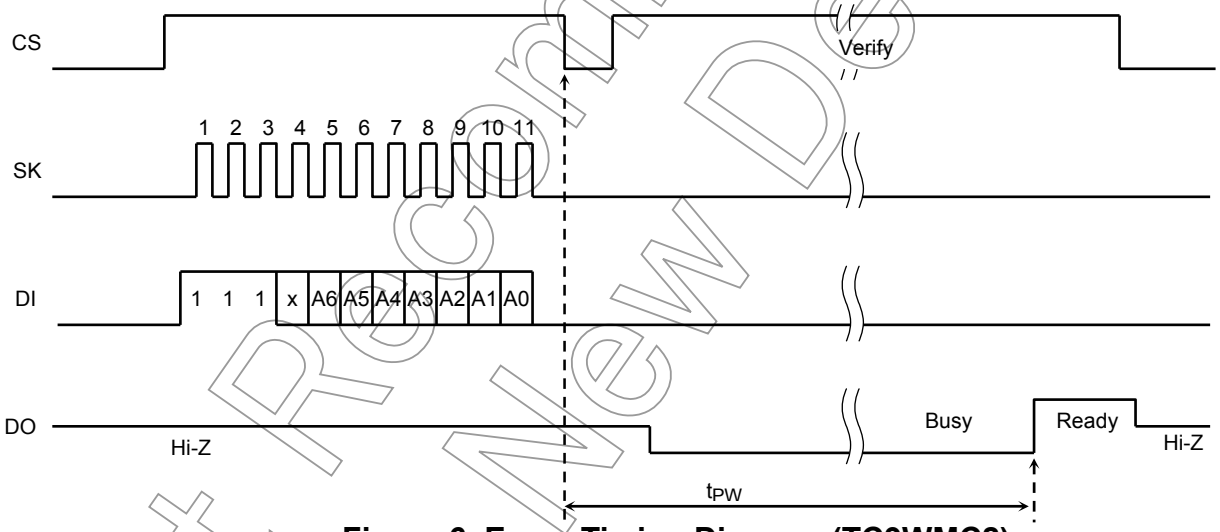

Figure 6. Erase Timing Diagram (TC9WMC2)

Not Recommended for New Design

(3.4) Write All (WRAL)

The Write All instruction writes all memory locations with data patterns specified in the instruction. The data is 16 bits long. After the CS is driven High, a start bit is transferred followed by the WRAL instruction, any addresses and 16 bits of data. After the least significant bit (D0) of data is received on the falling edge of SK, a write operation is triggered by the CS being pulled Low. It is not necessary to set every bit in the memory array to "1" before writing data.

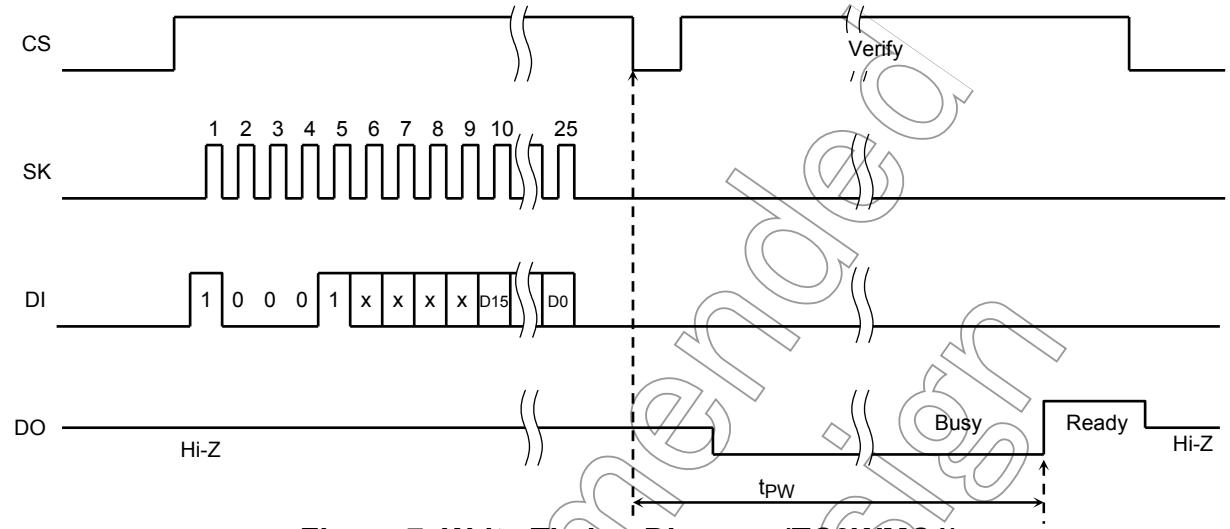

Figure 7. Write Timing Diagram (TC9WMC1)

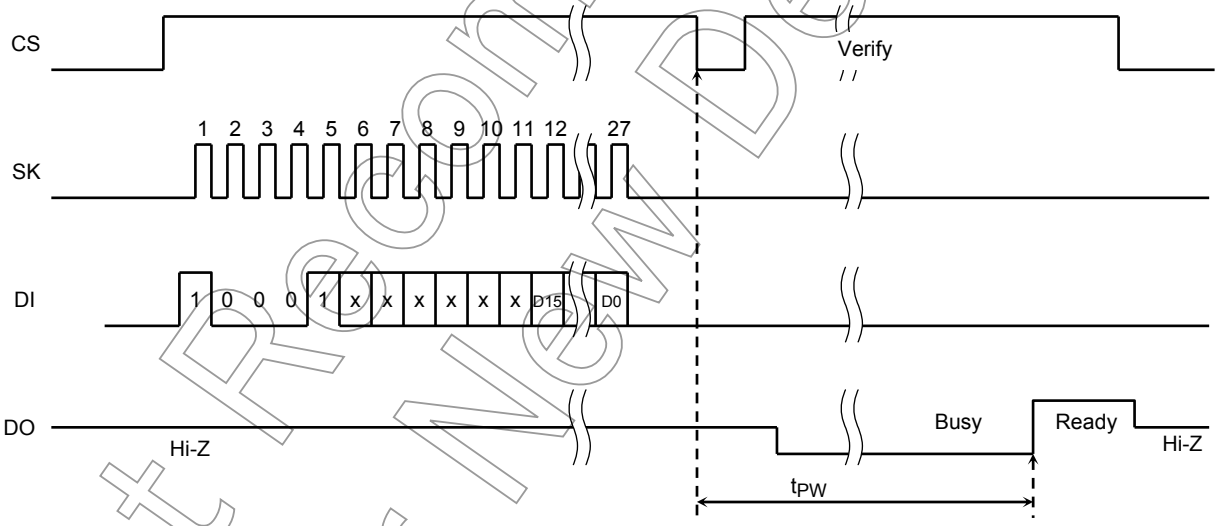

Figure 8. Write Timing Diagram (TC9WMC2)

Not Recommended for New Design

(3.5) Erase All (ERASE)

The Erase All instruction writes every bit in the memory array to 1. After the CS is driven High, a start bit is transferred followed by the ERAL instruction and any addresses. In this mode, data does not need to be transferred. After the least significant bit (A0) of the address is received on the falling edge of SK, an erase operation is triggered by the CS being pulled Low.

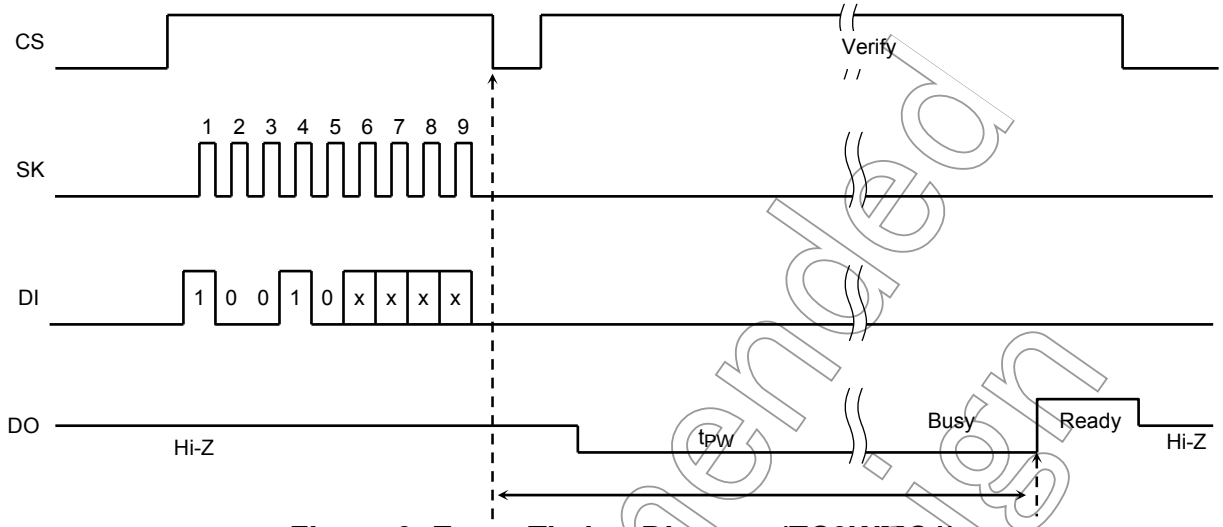

Figure 9. Erase Timing Diagram (TC9WMC1)

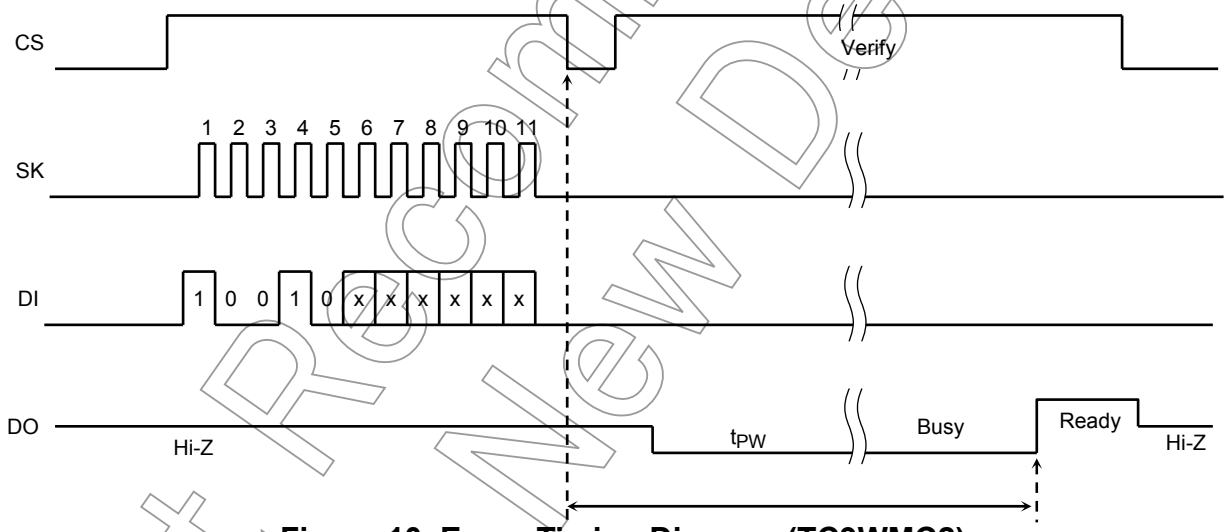

Figure 10. Erase Timing Diagram (TC9WMC2)

Not Recommended for New Design

(3.6) Write Enable (EWEN)/Write Disable (EWDS)

The EWEN instruction enables a write operation. In program enable mode, a writing operation is enabled.

The EWDS instruction disables a write operation. In program disable mode, a writing operation is disabled.

After power on, the device is in EWDS mode. The EWEN instruction must be executed before any write instructions can be carried out.

After the CS is driven High, a start bit is transferred followed by the EWEN/EWDS instruction and any addresses. The mode is enabled on the rising edge of SK after the least significant bit (A0) of the address is received.

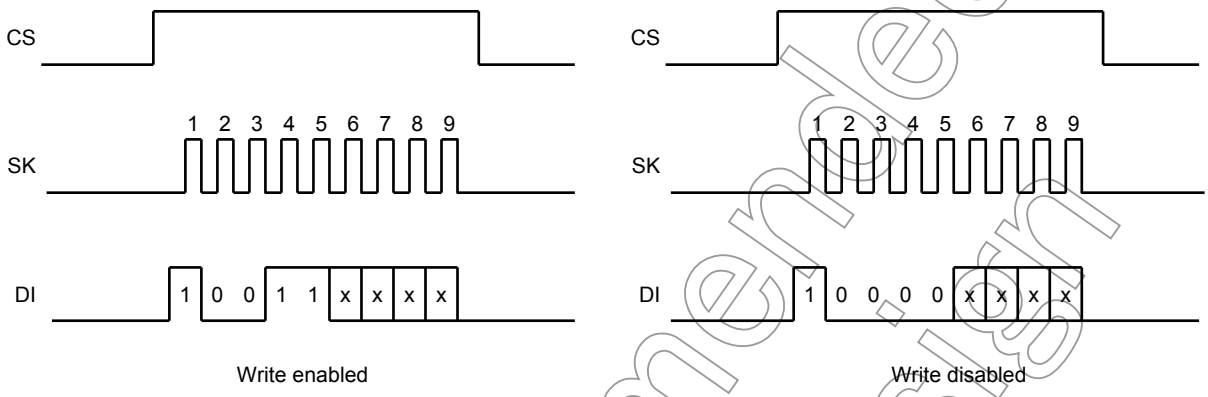

Figure 11. Write Enable/Disable Timing Diagram (TC9WMC1)

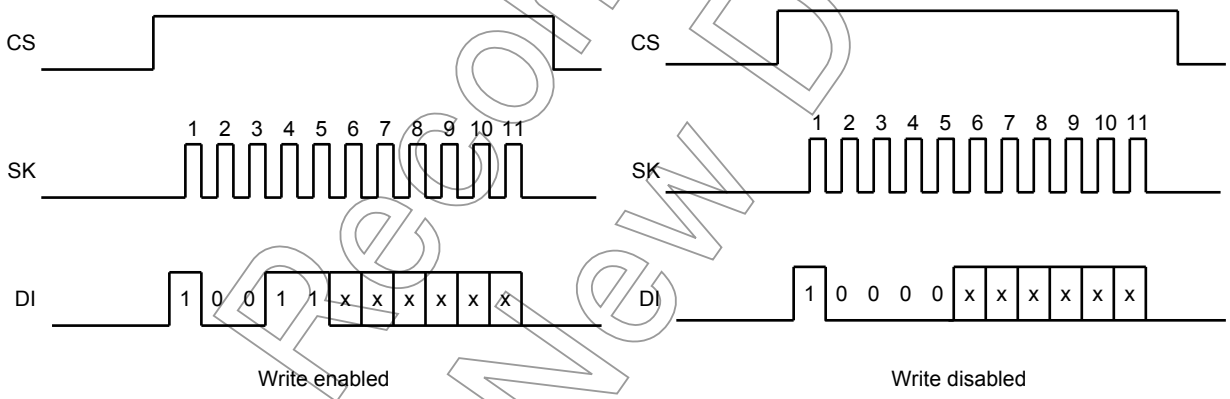

Figure 12. Write Enable/Disable Timing Diagram (TC9WMC2)

Not Recommended for New Design

3. Notes on Use

(1) Powering up the device

This device contains a power-on clear circuit, which initializes the internal circuit of the device when the power is turned on. If initialization fails, the chip may malfunction. When powering up the device, observe the following precautions to assure that the clear circuit will operate normally:

(a) Pull CS Low.
(b) The power rising time (t_R) must be 10 ms or less.
(c) After turning off the power, wait at least 100 ms (t_{OFF}) before attempting to power up the device again.
(d) The supply voltage must rise from a voltage lower than 0.1 V.
(e) After turning on the power, wait at least 20 ms before attempting to send an instruction to the device.

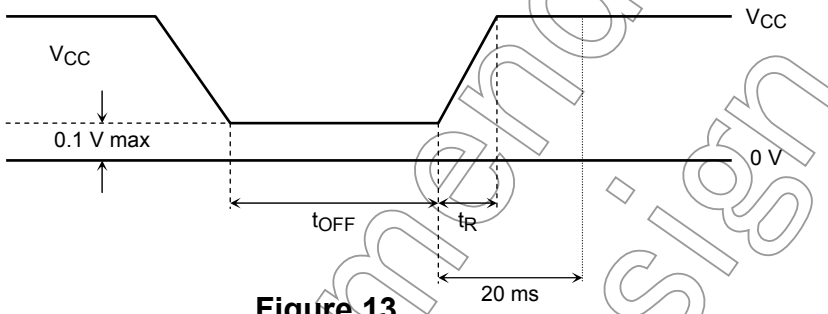

Figure 13

(2) Dummy cycle

When the DI input is driven Low, the SK clock cycles preceding a start bit are called “dummy cycles”. The device executes dummy cycles when an instruction from the CPU is longer than that for the device. For example, if the CPU’s instruction is 16 bits long, the TC9WMC1 executes seven dummy cycles and the TC9WMC2 executes five dummy cycles. Thus, the two instructions take the same number of clock cycles.

(3) Erroneous detection of a start bit

(a) If the DO output is High during the verify operation, a High on the DI input on the rising edge of SK causes the device to detect erroneously the start of serial reception. To prevent this, the DI input must be driven Low during the verify operation.
(b) When the DI and DO pins are configured as a 3-wire interface, data transfer from the CPU and that from the device can collide with each other during a certain period of time and the device cannot detect the start of serial reception correctly. To prevent this, a 10- to 100-KΩ resistor must be inserted between the DI and DO pins, so that the DI input from the CPU takes priority. (See Figure 14.)

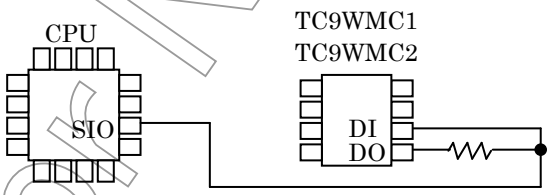

Figure 14

(4) Verify operation

(a) The DI input must be driven Low during the verify operation.
(b) When the DO output is driven High, a High on the DI input on the rising edge of SK causes the device to detect erroneously the start of serial reception and accepts an instruction. In this case, the DO pin immediately goes to the high-impedance state.

(5) Instruction cancellation

During an instruction execution, the instruction can be cancelled by pulling the CS pin Low. However, care must be taken for the timing of canceling a write operation as described below.

(a) The write operation can be cancelled when the CS is pulled Low on the rising edge of SK when the 15th bit of data is received.
(b) The write operation cannot be cancelled when the CS is pulled Low on the rising edge of SK after the 17th bit of data is received. In this case, the write instruction writes the 16 bits of data into the specified memory location.

Not Recommended for New Design

Absolute Maximum Ratings (Note) (GND = 0 V)

Characteristic	Symbol	Rating	Unit
Power supply voltage	V_{CC}	−0.3 to 7.0	V
Input voltage	V_{IN}	−0.3 to V_{CC} + 0.3	V
Output voltage	V_{OUT}	−0.3 to V_{CC} + 0.3	V
Power dissipation	P_D	300 (25°C,SM8)	mW
		200 (25°C,US8)	
Storage temperature	T_{stg}	−55 to 125	°C
Operating temperature	T_{opr}	−40 to 85	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (Note) (GND = 0 V, T_{opr} = −40 to 85°C)

Characteristic	Symbol	Test Condition	Min	Max	Unit
Supply voltage (for reading)	V_{CC}	—	1.8	3.6	V
Supply voltage (for writing)	V_{CC}	—	2.3	3.6	V
High-level input voltage	V_{IH}	2.7V ≤ V_{CC} ≤ 3.6 V	0.7 × V_{CC}	V_{CC}	V
		1.8 V ≤ V_{CC} < 2.7 V	0.8 × V_{CC}	V_{CC}	
Low-level input voltage	V_{IL}	2.7V ≤ V_{CC} ≤ 3.6 V	0	0.3 × V_{CC}	V
		1.8 V ≤ V_{CC} < 2.7 V	0	0.2 × V_{CC}	
Operating frequency	fsk	2.7V ≤ V_{CC} ≤ 3.6 V	0	2	MHz
		1.8 V ≤ V_{CC} < 2.7 V	0	0.5	

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either VCC or GND.

Electrical Characteristics

DC Characteristics (V_{CC} = 1.8 to 3.6 V, GND = 0 V, T_{opr} = −40 to 85°C)

Characteristic	Symbol	Test Condition	1.8 ≤ V_{CC} < 2.3 V		2.3 ≤ V_{CC} < 2.7 V		2.7 ≤ V_{CC} ≤ 3.6 V		Unit
			Min	Max	Min	Max	Min	Max	
Input current	I_{LI}		—	±1	—	±1	—	±1	μA
Output leakage current	I_{LO}		—	±1	—	±1	—	±1	μA
High-level output voltage	V_{OH}	I_{OH} = −400 μA	—	—	—	—	—	—	V
		I_{OH} = −100 μA	V_{CC} − 0.2	—	V_{CC} − 0.2	—	V_{CC} − 0.2	—	
Low-level output voltage	V_{OL}	I_{OL} = 2.1 mA	—	—	—	—	—	—	V
		I_{OL} = 100 μA	—	0.2	—	0.2	—	0.2	
Quiescent supply current	I_{CC1}		—	2	—	2	—	2	μA
Supply current during read	I_{CC2}	f_{SK} = 2 MHz (Note)	—	0.5	—	1.0	—	1.5	mA
Supply current during program	I_{CC3}	f_{SK} = 2 MHz	—	—	—	1.0	—	1.5	mA

Note: V_{CC} = 1.8 to 2.3 V @f_{SK} = 0.5 MHz

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AC Characteristics (V_{CC} = 1.8 to 3.6 V, GND = 0 V, T_{opr} = −40 to 85°C)

Characteristic	Symbol	1.8 ≤ V_{CC} < 2.3 V		2.3 ≤ V_{CC} < 2.7 V		2.7 ≤ V_{CC} ≤ 3.6 V		Unit
		Min	Max	Min	Max	Min	Max	
SK clock frequency	f_{SK}	0	0.5	0	1.5	0	2	MHz
SK clock pulse width	t_{SKH}	2.0	—	0.5	—	0.25	—	μs
	t_{SKL}	2.0	—	0.5	—	0.25	—	
CS Low period	t_{CS}	0.5	—	0.3	—	0.2	—	μs
CS setup time	t_{CSS}	1	—	0.4	—	0.2	—	μs
CS hold time	t_{CSH}	0	—	0	—	0	—	μs
DI setup time	t_{DS}	0.4	—	0.2	—	0.1	—	μs
DI hold time	t_{DH}	0.4	—	0.2	—	0.1	—	μs
Propagation delay time (Note)	t_{PD}	—	2.0	—	1.0	—	0.4	μs
Output disable time	t_{HZ}	0	1.0	0	0.5	0	0.5	μs
Output enable time	t_{SV}	0	1.0	0	0.5	0	0.5	μs

Note: C_L = 100 pF, R_L = 1 kΩ

E^2PROM Characteristics (GND = 0 V, 2.3 V ≤ V_{CC} ≤ 3.6 V, T_{opr} = −40 to 85°C)

Characteristic	Symbol	Test Condition	Min	Max	Unit
Program time	t_{PW}	3.0V ≤ V_{CC} ≤ 3.6 V	—	10	ms
		2.3V ≤ V_{CC} < 3.0 V	—	12	
Rewrite cycle	N_{EW}		1×10^5	—	Times
Data retention time	t_{RET}		10	—	Year

Capacitance Characteristics (Ta = 25°C)

Characteristic	Symbol	Test Condition		Typ.	Unit
			V_{CC} (V)		
Input capacitance	C_{IN}		3.3	4	pF
Output capacitance	C_O		3.3	4	pF

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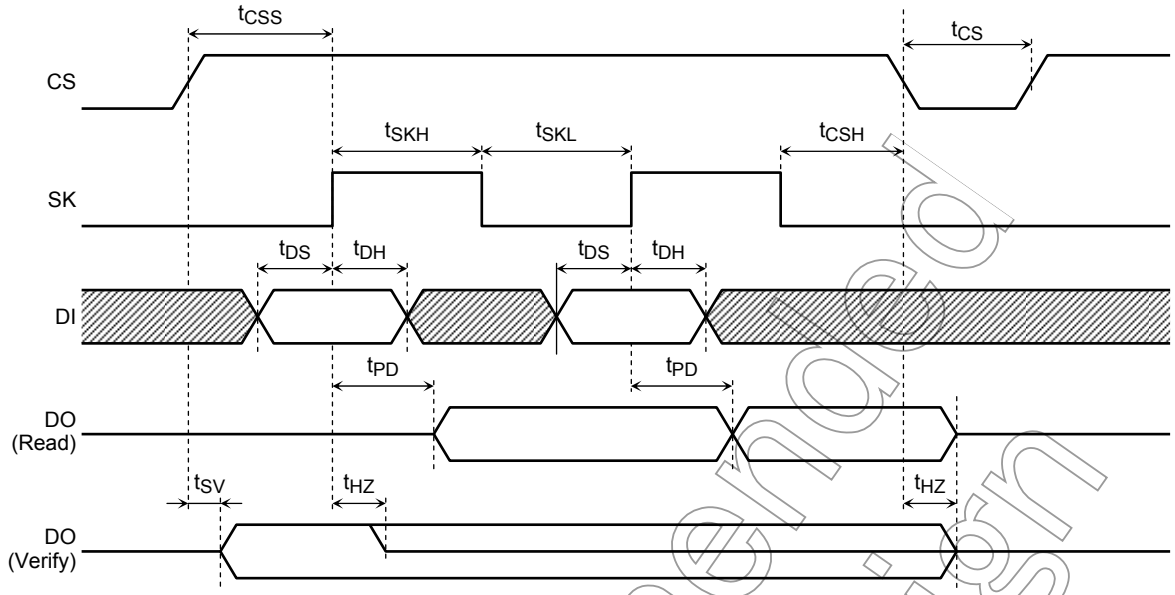
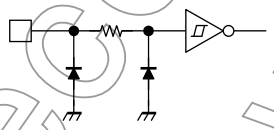
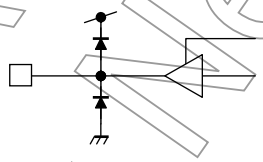
AC Characteristics Timing Chart



Input/Output Circuits of Pins

Pin	Type	Input/Output Circuit	Remarks
CS DI SK	Input		Hysteresis input
DO	Output		Initial High Z

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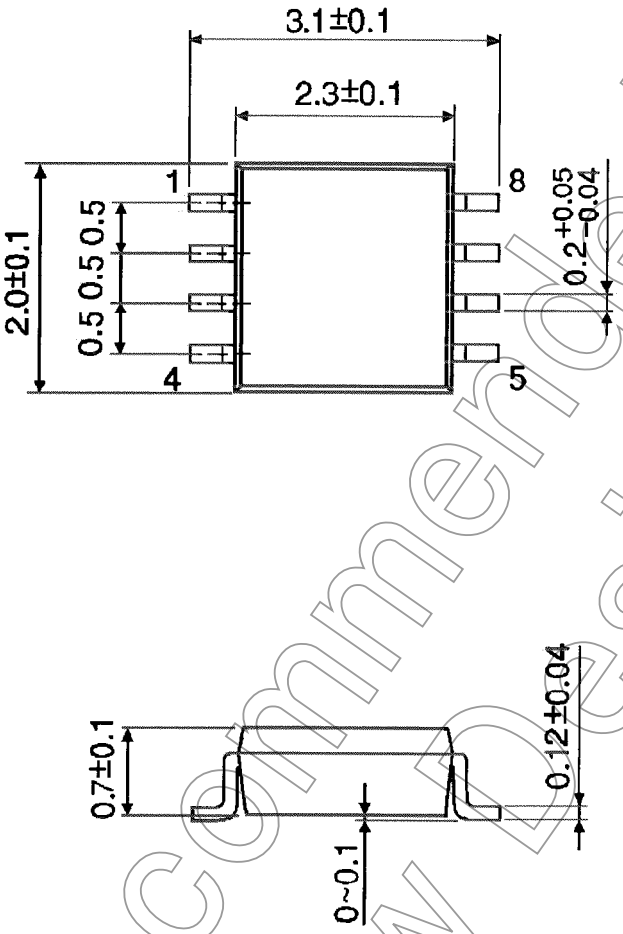
Package Dimensions

SSOP8-P-0.50A Unit : mm

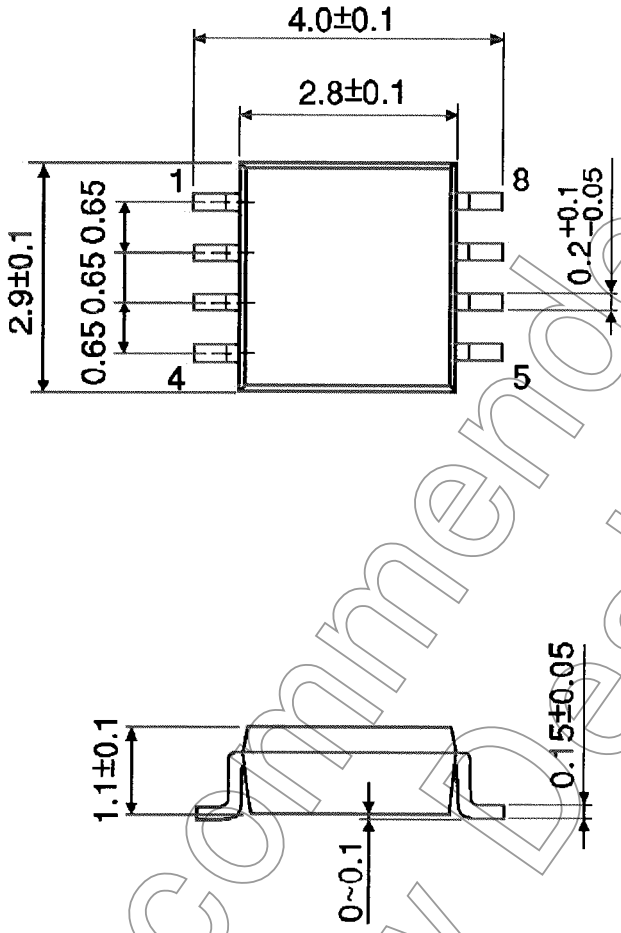


Weight: 0.01 g (typ.)

Not Recommended for New Design

Package Dimensions

SSOP8-P-0.65 Unit : mm



Weight: 0.02 g (typ.)

Not Recommended for New Design

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