

165-Bump BGA  
Commercial Temp  
Industrial Temp

## 144Mb SigmaQuad™-II Burst of 2 SRAM

300 MHz–250 MHz  
1.8 V  $V_{DD}$   
1.8 V and 1.5 V I/O

### Features

- Simultaneous Read and Write SigmaQuad™ Interface
- JEDEC-standard pinout and package
- Dual Double Data Rate interface
- Byte Write controls sampled at data-in time
- Burst of 2 Read and Write
- 1.8 V +100/-100 mV core power supply
- 1.5 V or 1.8 V HSTL Interface
- Pipelined read operation
- Fully coherent read and write pipelines
- ZQ pin for programmable output drive strength
- IEEE 1149.1 JTAG-compliant Boundary Scan
- Pin-compatible with present 144 Mb devices
- 165-bump, 15 mm x 17 mm, 1 mm bump pitch BGA package
- RoHS-compliant 165-bump BGA package available

### SigmaQuad™ Family Overview

The GS81302Q08/09E are built in compliance with the SigmaQuad-II SRAM pinout standard for Separate I/O synchronous SRAMs. They are 150,994,944-bit (144Mb) SRAMs. The GS81302Q08/09E SigmaQuad SRAMs are just one element in a family of low power, low voltage HSTL I/O SRAMs designed to operate at the speeds needed to implement economical high performance networking systems.

### Clocking and Addressing Schemes

The GS81302Q08/09E SigmaQuad-II SRAMs are synchronous devices. They employ two input register clock inputs, K and  $\bar{K}$ . K and  $\bar{K}$  are independent single-ended clock inputs, not differential inputs to a single differential clock input buffer. The device also allows the user to manipulate the output register clock inputs quasi independently with the C and  $\bar{C}$  clock inputs. C and  $\bar{C}$  are also independent single-ended clock inputs, not differential inputs. If the C clocks are tied high, the K clocks are routed internally to fire the output registers instead.

Each internal read and write operation in a SigmaQuad-II B2 RAM is two times wider than the device I/O bus. An input data bus de-multiplexer is used to accumulate incoming data before it is simultaneously written to the memory array. An output data multiplexer is used to capture the data produced from a single memory array read and then route it to the appropriate output drivers as needed. Therefore, the address field of a SigmaQuad-II B2 RAM is always one address pin less than the advertised index depth (e.g., the 16M x 8 has an 8M addressable index).

### Parameter Synopsis

	-300	-250
t <sub>KHKH</sub>	3.3 ns	4.0 ns
t <sub>KHQV</sub>	0.45 ns	0.45 ns

## 16M x 8 SigmaQuad-II SRAM—Top View

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{\text{CQ}}$	SA	SA	$\overline{\text{W}}$	$\overline{\text{NW1}}$	$\overline{\text{K}}$	SA	$\overline{\text{R}}$	SA	SA	CQ
B	NC	NC	NC	SA	NC/SA (288Mb)	K	$\overline{\text{NW0}}$	SA	NC	NC	Q3
C	NC	NC	NC	$V_{SS}$	SA	SA	SA	$V_{SS}$	NC	NC	D3
D	NC	D4	NC	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	NC	NC	NC
E	NC	NC	Q4	$V_{DDQ}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{DDQ}$	NC	D2	Q2
F	NC	NC	NC	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	NC	NC	NC
G	NC	D5	Q5	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	NC	NC	NC
H	$\overline{\text{Doff}}$	$V_{REF}$	$V_{DDQ}$	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	$V_{DDQ}$	$V_{REF}$	ZQ
J	NC	NC	NC	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	NC	Q1	D1
K	NC	NC	NC	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	NC	NC	NC
L	NC	Q6	D6	$V_{DDQ}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{DDQ}$	NC	NC	Q0
M	NC	NC	NC	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	NC	NC	D0
N	NC	D7	NC	$V_{SS}$	SA	SA	SA	$V_{SS}$	NC	NC	NC
P	NC	NC	Q7	SA	SA	C	SA	SA	NC	NC	NC
R	TDO	TCK	SA	SA	SA	$\overline{\text{C}}$	SA	SA	SA	TMS	TDI

 11 x 15 Bump BGA—15 x 17 mm<sup>2</sup> Body—1 mm Bump Pitch

**Notes:**

1.  $\overline{\text{NW0}}$  controls writes to D0:D3.  $\overline{\text{NW1}}$  controls writes to D4:D7.
2. B5 is the expansion address.

## 16M x 9 SigmaQuad-II SRAM — Top View

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{\text{CQ}}$	SA	SA	$\overline{\text{W}}$	NC	$\overline{\text{K}}$	SA	$\overline{\text{R}}$	SA	SA	CQ
B	NC	NC	NC	SA	NC/SA (288Mb)	K	$\overline{\text{BW0}}$	SA	NC	NC	Q4
C	NC	NC	NC	$V_{SS}$	SA	SA	SA	$V_{SS}$	NC	NC	D4
D	NC	D5	NC	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	NC	NC	NC
E	NC	NC	Q5	$V_{DDQ}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{DDQ}$	NC	D3	Q3
F	NC	NC	NC	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	NC	NC	NC
G	NC	D6	Q6	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	NC	NC	NC
H	$\overline{\text{Doff}}$	$V_{REF}$	$V_{DDQ}$	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	$V_{DDQ}$	$V_{REF}$	ZQ
J	NC	NC	NC	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	NC	Q2	D2
K	NC	NC	NC	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	NC	NC	NC
L	NC	Q7	D7	$V_{DDQ}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{DDQ}$	NC	NC	Q1
M	NC	NC	NC	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	NC	NC	D1
N	NC	D8	NC	$V_{SS}$	SA	SA	SA	$V_{SS}$	NC	NC	NC
P	NC	NC	Q8	SA	SA	C	SA	SA	NC	D0	Q0
R	TDO	TCK	SA	SA	SA	$\overline{\text{C}}$	SA	SA	SA	TMS	TDI

 11 x 15 Bump BGA—15 x 17 mm<sup>2</sup> Body—1 mm Bump Pitch

**Notes:**

1.  $\overline{\text{BW0}}$  controls writes to DQ:D8.
2. B5 is the expansion address.

**Pin Description Table**

Symbol	Description	Type	Comments
SA	Synchronous Address Inputs	Input	—
$\overline{R}$	Synchronous Read	Input	Active Low
$\overline{W}$	Synchronous Write	Input	Active Low
$\overline{BW0}$	Synchronous Byte Write	Input	Active Low x9 only
$\overline{NW0}\text{--}\overline{NW1}$	Nybble Write Control Pin	Input	Active Low x8 only
K	Input Clock	Input	Active High
$\overline{K}$	Input Clock	Input	Active Low
C	Output Clock	Input	Active High
$\overline{C}$	Output Clock	Input	Active Low
TMS	Test Mode Select	Input	—
TDI	Test Data Input	Input	—
TCK	Test Clock Input	Input	—
TDO	Test Data Output	Output	—
V <sub>REF</sub>	HSTL Input Reference Voltage	Input	—
ZQ	Output Impedance Matching Input	Input	—
Qn	Synchronous Data Outputs	Output	—
Dn	Synchronous Data Inputs	Input	—
$\overline{D}_{off}$	Disable DLL when low	Input	Active Low
CQ	Output Echo Clock	Output	—
$\overline{CQ}$	Output Echo Clock	Output	—
V <sub>DD</sub>	Power Supply	Supply	1.8 V Nominal
V <sub>DDQ</sub>	Isolated Output Buffer Supply	Supply	1.5 or 1.8 V Nominal
V <sub>SS</sub>	Power Supply: Ground	Supply	—
NC	No Connect	—	—

**Notes:**

1. NC = Not Connected to die or any other pin
2. When ZQ pin is directly connected to V<sub>DDQ</sub>, output impedance is set to minimum value and it cannot be connected to ground or left unconnected.
3. C,  $\overline{C}$ , K,  $\overline{K}$  cannot be set to V<sub>REF</sub> voltage.

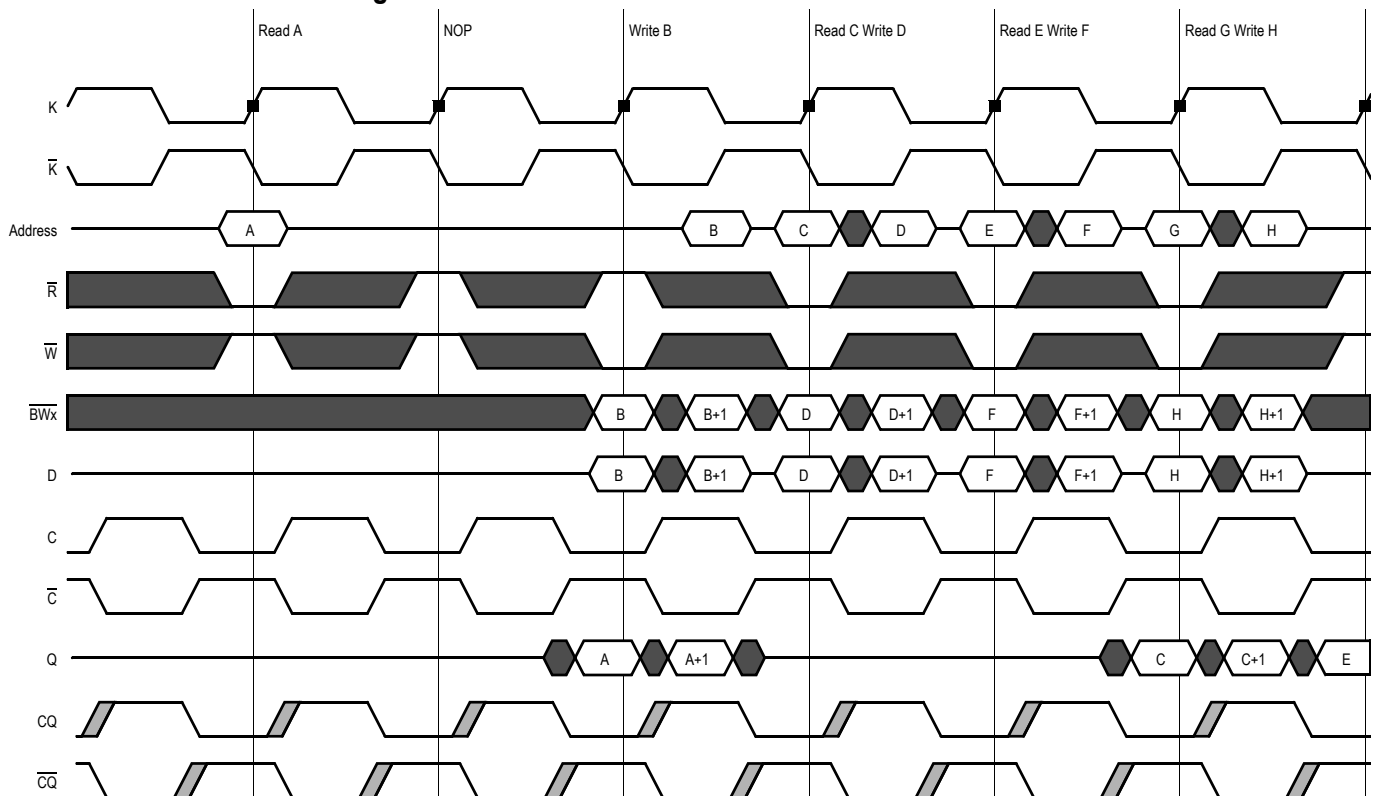
## Background

Separate I/O SRAMs, from a system architecture point of view, are attractive in applications where alternating reads and writes are needed. Therefore, the SigmaQuad-II SRAM interface and truth table are optimized for alternating reads and writes. Separate I/O SRAMs are unpopular in applications where multiple reads or multiple writes are needed because burst read or write transfers from Separate I/O SRAMs can cut the RAM's bandwidth in half.

### SigmaQuad-II B2 SRAM DDR Read

The read port samples the status of the Address Input and  $\overline{R}$  pins at each rising edge of K. A low on the Read Enable-bar pin,  $\overline{R}$ , begins a read cycle. Data can be clocked out after the next rising edge of K with a rising edge of  $\overline{C}$  (or by  $\overline{K}$  if C and  $\overline{C}$  are tied high), and after the following rising edge of  $\overline{K}$  with a rising edge of C (or by K if C and  $\overline{C}$  are tied high). Clocking in a high on the Read Enable-bar pin,  $\overline{R}$ , begins a read port deselect cycle.

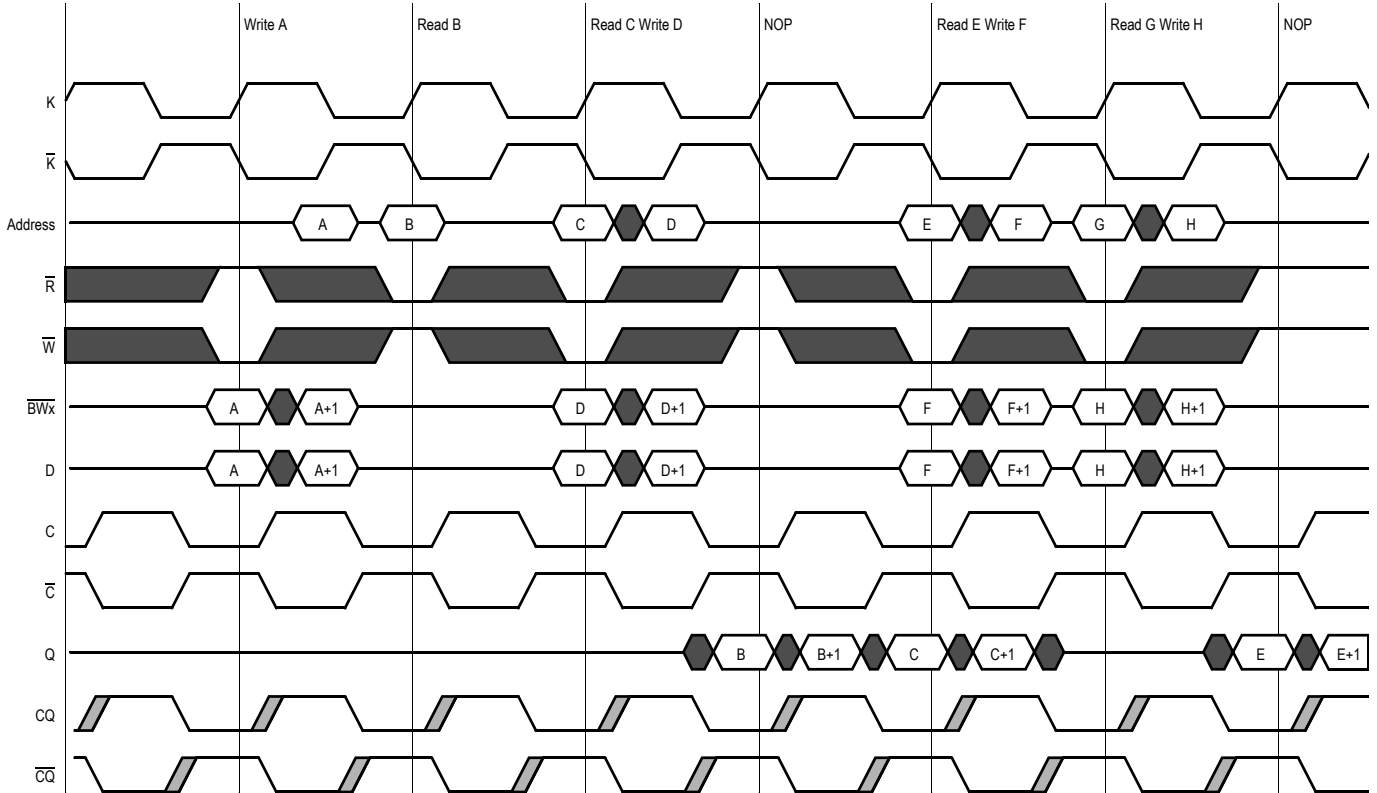
SigmaQuad-II B2 Double Data Rate SRAM Read First



**SigmaQuad-II B2 SRAM DDR Write**

The write port samples the status of the  $\overline{W}$  pin at each rising edge of  $K$  and the Address Input pins on the following rising edge of  $\overline{K}$ . A low on the Write Enable-bar pin,  $\overline{W}$ , begins a write cycle. The first of the data-in pairs associated with the write command is clocked in with the same rising edge of  $K$  used to capture the write command. The second of the two data in transfers is captured on the rising edge of  $\overline{K}$  along with the write address. Clocking in a high on  $\overline{W}$  causes a write port deselect cycle.

**SigmaQuad-II B2 Double Data Rate SRAM Write First**



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## Special Functions

### Byte Write and Nybble Write Control

Byte Write Enable pins are sampled at the same time that Data In is sampled. A high on the Byte Write Enable pin associated with a particular byte (e.g.,  $\overline{BW0}$  controls D0–D8 inputs) will inhibit the storage of that particular byte, leaving whatever data may be stored at the current address at that byte location undisturbed. Any or all of the Byte Write Enable pins may be driven high or low during the data in sample times in a write sequence.

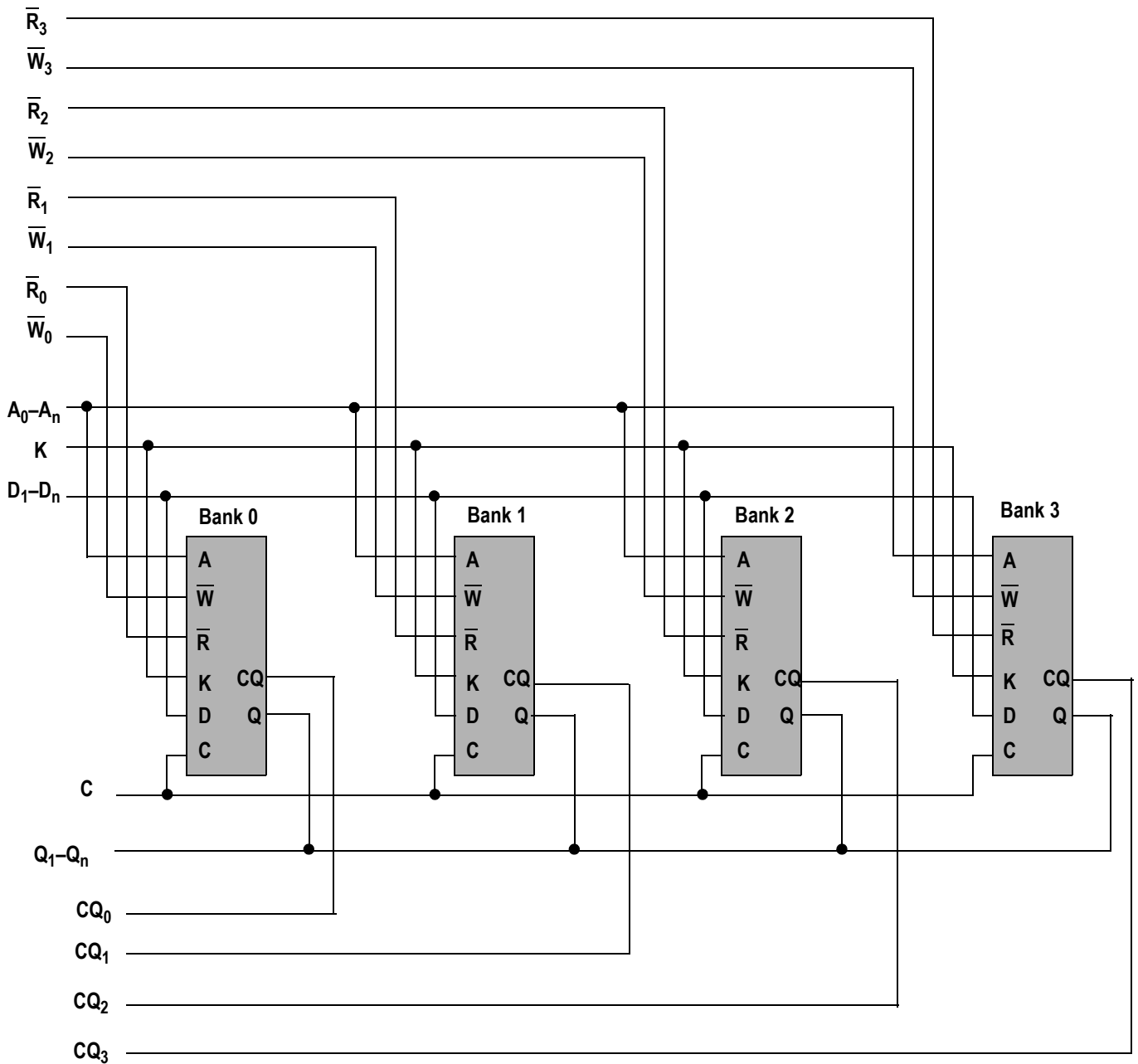
Each write enable command and write address loaded into the RAM provides the base address for a 2 beat data transfer. The x9 version of the RAM, for example, may write 36 bits in association with each address loaded. Either 9-bit byte may be masked in any write sequence.

Nybble Write (4-bit) control is implemented on the 8-bit-wide version of the device. For the x8 version of the device, “Nybble Write Enable” and “ $\overline{NBx}$ ” may be substituted in all the discussion above.

### Output Register Control

SigmaQuad-II SRAMs offer two mechanisms for controlling the output data registers. Typically, control is handled by the Output Register Clock inputs, C and  $\overline{C}$ . The Output Register Clock inputs can be used to make small phase adjustments in the firing of the output registers by allowing the user to delay driving data out as much as a few nanoseconds beyond the next rising edges of the K and  $\overline{K}$  clocks. If the C and  $\overline{C}$  clock inputs are tied high, the RAM reverts to K and  $\overline{K}$  control of the outputs, allowing the RAM to function as a conventional pipelined read SRAM.

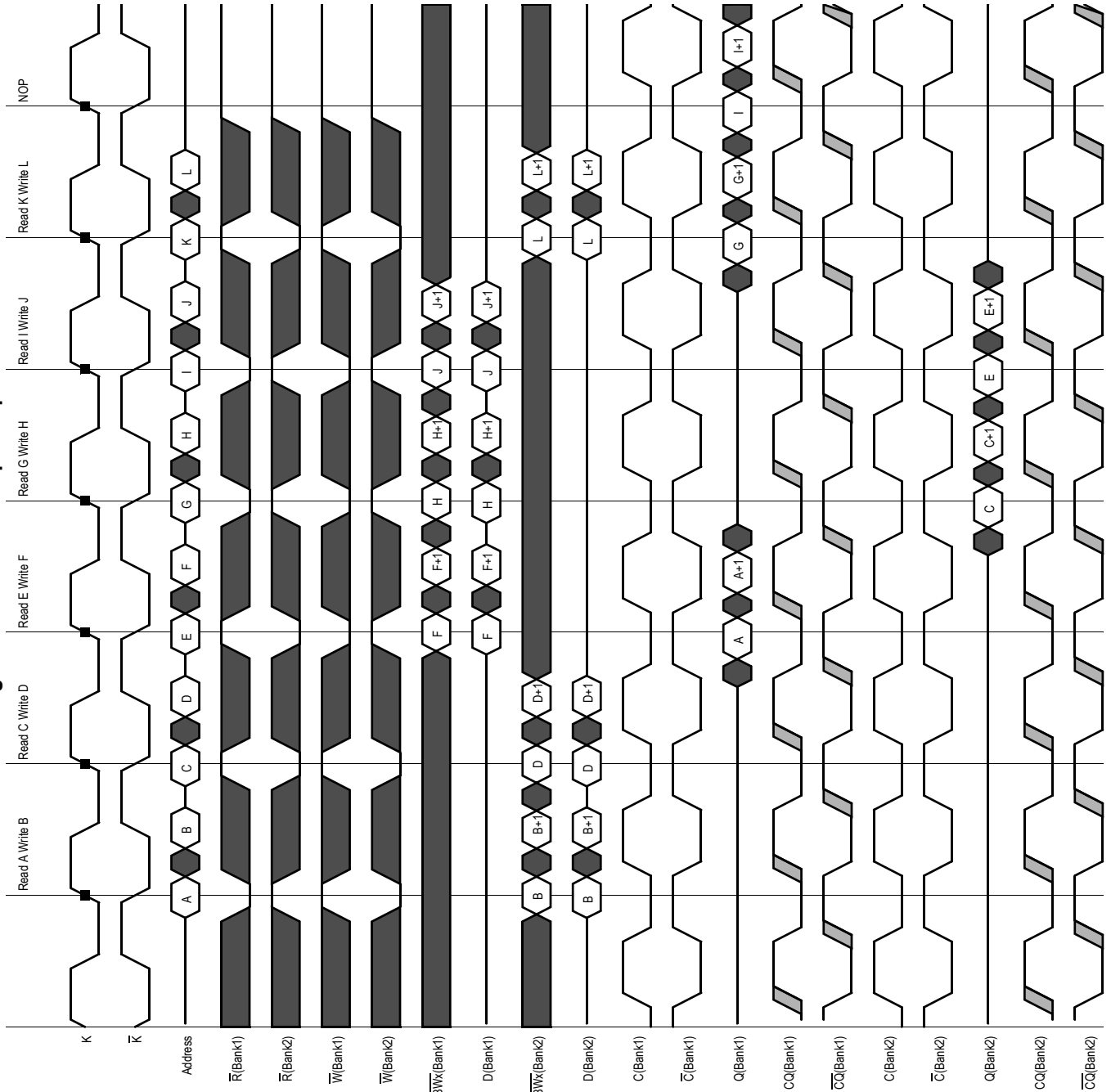
Example Four Bank Depth Expansion Schematic



**Note:**

For simplicity  $\overline{B}W_n, \overline{N}W_n, \overline{K}$ , and  $\overline{C}$  are not shown.

**Burst of 2 SigmaQuad-II SRAM Depth Expansion**



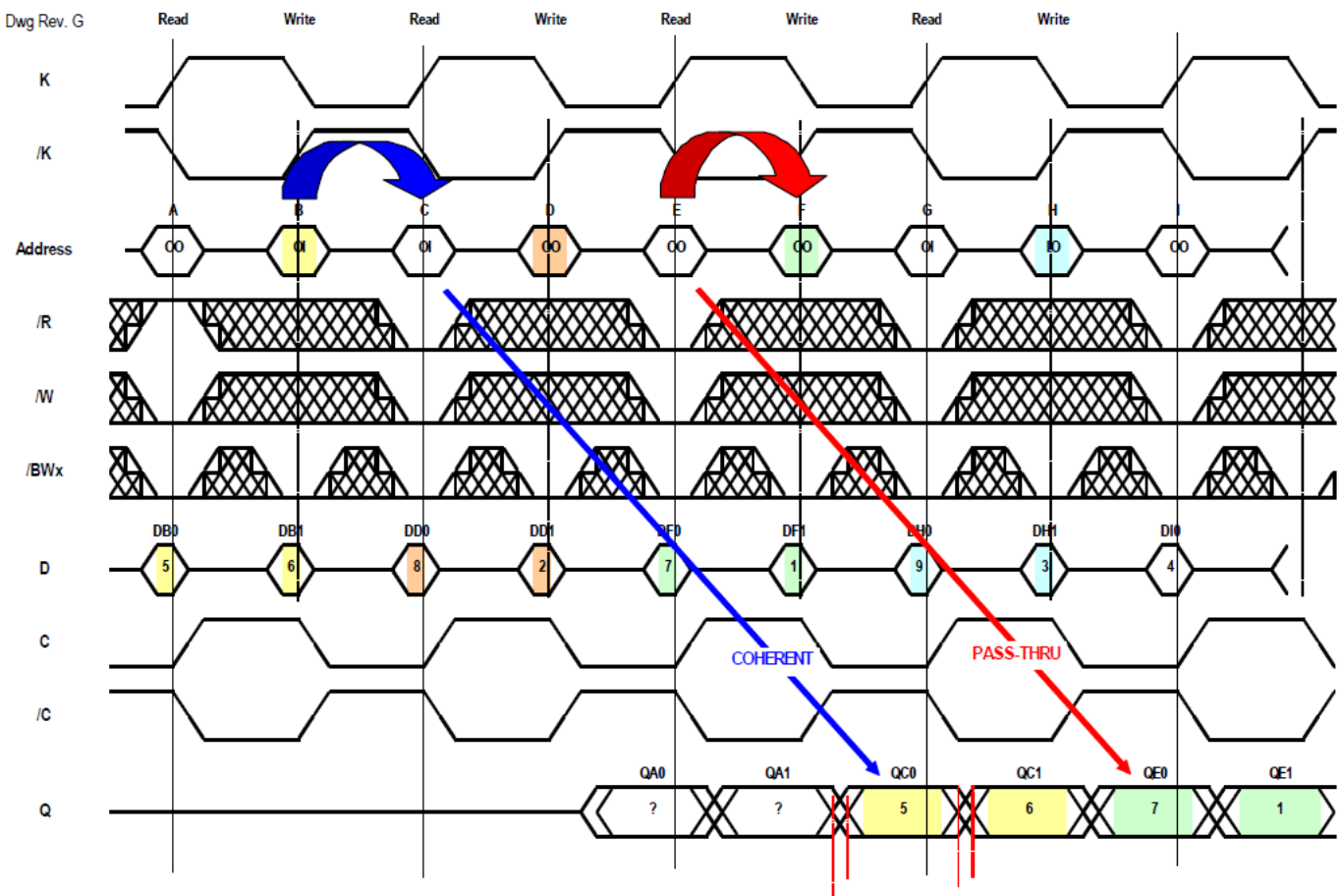
### FLXDrive-II Output Driver Impedance Control

HSTL I/O SigmaQuad-II SRAMs are supplied with programmable impedance output drivers. The ZQ pin must be connected to  $V_{SS}$  via an external resistor, RQ, to allow the SRAM to monitor and adjust its output driver impedance. The value of RQ must be 5X the value of the desired RAM output impedance. The allowable range of RQ to guarantee impedance matching continuously is between 175Ω and 350Ω. Periodic readjustment of the output driver impedance is necessary as the impedance is affected by drifts in supply voltage and temperature. The SRAM's output impedance circuitry compensates for drifts in supply voltage and temperature. A clock cycle counter periodically triggers an impedance evaluation, resets and counts again. Each impedance evaluation may move the output driver impedance level one step at a time towards the optimum level. The output driver is implemented with discrete binary weighted impedance steps.

### SigmaQuad-II B2 Coherency and Pass Through Functions

Because the SigmaQuad-II B2 read and write commands are loaded at the same time, there may be some confusion over what constitutes “coherent” operation. Normally, one would expect a RAM to produce the just-written data when it is read immediately after a write. This is true of the SigmaQuad-II B2 except in one case, as is illustrated in the following diagram. If the user holds the same address value in a given K clock cycle, loading the same address as a read address and then as a matching write address, the SigmaQuad-II B2 will read or “Pass-thru” the latest data input, rather than the data from the previously completed write operation.

**SigmaQuad-II B2 Coherency and Pass Through Functions**



**Separate I/O SigmaQuad-II B2 SigmaQuad-II SRAM Read Truth Table**

A	$\bar{R}$	Output Next State	Q	Q
$K \uparrow$ ( $t_n$ )	$K \uparrow$ ( $t_n$ )	$K \uparrow$ ( $t_n$ )	$\bar{K} \uparrow$ ( $t_{n+1/2}$ )	$K \uparrow$ ( $t_{n+2}$ )
X	1	Deselect	Hi-Z	Hi-Z
V	0	Read	Q0	Q1

**Notes:**

1. X = Don't Care, 1 = High, 0 = Low, V = Valid.
2. R is evaluated on the rising edge of K.
3. Q0 and Q1 are the first and second data output transfers in a read.

**Separate I/O SigmaQuad-II B2 SigmaQuad-II SRAM Write Truth Table**

A	$\bar{W}$	$\overline{BWn}$	$\overline{BWn}$	Input Next State	D	D
$\bar{K} \uparrow$ ( $t_{n+1/2}$ )	$K \uparrow$ ( $t_n$ )	$K \uparrow$ ( $t_n$ )	$\bar{K} \uparrow$ ( $t_{n+1/2}$ )	$K \uparrow, \bar{K} \uparrow$ ( $t_n, t_{n+1/2}$ )	$K \uparrow$ ( $t_n$ )	$\bar{K} \uparrow$ ( $t_{n+1/2}$ )
V	0	0	0	Write Byte Dx0, Write Byte Dx1	D0	D1
V	0	0	1	Write Byte Dx0, Write Abort Byte Dx1	D0	X
V	0	1	0	Write Abort Byte Dx0, Write Byte Dx1	X	D1
X	0	1	1	Write Abort Byte Dx0, Write Abort Byte Dx1	X	X
X	1	X	X	Deselect	X	X

**Notes:**

1. X = Don't Care, H = High, L = Low, V = Valid.
2. W is evaluated on the rising edge of K.
3. D0 and D1 are the first and second data input transfers in a write.
4.  $\overline{BWn}$  represents any of the Byte Write Enable inputs ( $\overline{BW0}$ ,  $\overline{BW1}$ , etc.).

**x8 Nybble Write Enable ( $\overline{NWn}$ ) Truth Table**

$\overline{NW0}$	$\overline{NW1}$	D0–D3	D4–D7
1	1	Don't Care	Don't Care
0	1	Data In	Don't Care
1	0	Don't Care	Data In
0	0	Data In	Data In

## Absolute Maximum Ratings

(All voltages reference to  $V_{SS}$ )

Symbol	Description	Value	Unit
$V_{DD}$	Voltage on $V_{DD}$ Pins	-0.5 to 2.9	V
$V_{DDQ}$	Voltage in $V_{DDQ}$ Pins	-0.5 to $V_{DD}$	V
$V_{REF}$	Voltage in $V_{REF}$ Pins	-0.5 to $V_{DDQ}$	V
$V_{I/O}$	Voltage on I/O Pins	-0.5 to $V_{DDQ} + 0.5$ ( $\leq 2.9$ V max.)	V
$V_{IN}$	Voltage on Other Input Pins	-0.5 to $V_{DDQ} + 0.5$ ( $\leq 2.9$ V max.)	V
$I_{IN}$	Input Current on Any Pin	+/-100	mA dc
$I_{OUT}$	Output Current on Any I/O Pin	+/-100	mA dc
$T_J$	Maximum Junction Temperature	125	$^{\circ}\text{C}$
$T_{STG}$	Storage Temperature	-55 to 125	$^{\circ}\text{C}$

### Note:

Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Recommended Operating Conditions, for an extended period of time, may affect reliability of this component.

## Recommended Operating Conditions

### Power Supplies

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	$V_{DD}$	1.7	1.8	1.9	V
I/O Supply Voltage	$V_{DDQ}$	1.4	—	$V_{DD}$	V
Reference Voltage	$V_{REF}$	0.68	—	0.95	V

### Note:

The power supplies need to be powered up simultaneously or in the following sequence:  $V_{DD}$ ,  $V_{DDQ}$ ,  $V_{REF}$ , followed by signal inputs. The power down sequence must be the reverse.  $V_{DDQ}$  must not exceed  $V_{DD}$ . For more information, read **AN1021 SigmaQuad and SigmaDDR Power-Up**.

### Operating Temperature

Parameter	Symbol	Min.	Typ.	Max.	Unit
Junction Temperature (Commercial Range Versions)	$T_J$	0	25	85	$^{\circ}\text{C}$
Junction Temperature (Industrial Range Versions)*	$T_J$	-40	25	100	$^{\circ}\text{C}$

### Note:

\* The part numbers of Industrial Temperature Range versions end with the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.

## Thermal Impedance

Package	Test PCB Substrate	$\theta_{JA}$ (C°/W) Airflow = 0 m/s	$\theta_{JA}$ (C°/W) Airflow = 1 m/s	$\theta_{JA}$ (C°/W) Airflow = 2 m/s	$\theta_{JB}$ (C°/W)	$\theta_{JC}$ (C°/W)
165 BGA	4-layer	16.4	13.4	12.4	8.6	1.2

### Notes:

1. Thermal Impedance data is based on a number of samples from multiple lots and should be viewed as a typical number.
2. Please refer to JEDEC standard JESD51-6.
3. The characteristics of the test fixture PCB influence reported thermal characteristics of the device. Be advised that a good thermal path to the PCB can result in cooling or heating of the RAM depending on PCB temperature.

## HSTL I/O DC Input Characteristics

Parameter	Symbol	Min	Max	Units	Notes
DC Input Logic High	$V_{IH}$ (dc)	$V_{REF} + 0.1$	$V_{DDQ} + 0.3$	V	1
DC Input Logic Low	$V_{IL}$ (dc)	-0.3	$V_{REF} - 0.1$	V	1

### Notes:

1. Compatible with both 1.8 V and 1.5 V I/O drivers.
2. These are DC test criteria. DC design criteria is  $V_{REF} \pm 50$  mV. The AC  $V_{IH}/V_{IL}$  levels are defined separately for measuring timing parameters.
3.  $V_{IL}$  (Min)DC = -0.3 V,  $V_{IL}$  (Min)AC = -1.5 V (pulse width  $\leq 3$  ns).
4.  $V_{IH}$  (Max)DC =  $V_{DDQ} + 0.3$  V,  $V_{IH}$  (Max)AC =  $V_{DDQ} + 0.85$  V (pulse width  $\leq 3$  ns).

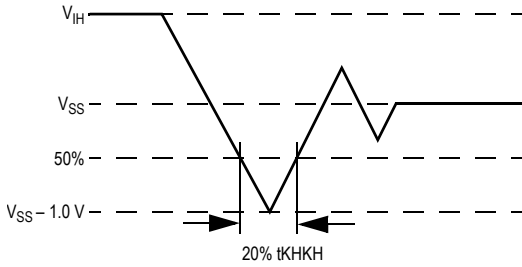
## HSTL I/O AC Input Characteristics

Parameter	Symbol	Min	Max	Units	Notes
AC Input Logic High	$V_{IH}$ (ac)	$V_{REF} + 200$	—	mV	2,3
AC Input Logic Low	$V_{IL}$ (ac)	—	$V_{REF} - 200$	mV	2,3
$V_{REF}$ Peak-to-Peak AC Voltage	$V_{REF}$ (ac)	—	5% $V_{REF}$ (DC)	mV	1

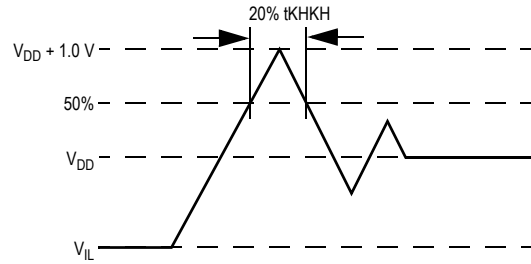
### Notes:

1. The peak-to-peak AC component superimposed on  $V_{REF}$  may not exceed 5% of the DC component of  $V_{REF}$ .
2. To guarantee AC characteristics,  $V_{IH}, V_{IL}, Trise,$  and  $Tfall$  of inputs and clocks must be within 10% of each other.
3. For devices supplied with HSTL I/O input buffers. Compatible with both 1.8 V and 1.5 V I/O drivers.

**Undershoot Measurement and Timing**



**Overshoot Measurement and Timing**



**Capacitance**

( $T_A = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$ ,  $V_{DD} = 1.8\text{ V}$ )

Parameter	Symbol	Test conditions	Typ.	Max.	Unit
Input Capacitance	$C_{IN}$	$V_{IN} = 0\text{ V}$	4	5	pF
Output Capacitance	$C_{OUT}$	$V_{OUT} = 0\text{ V}$	6	7	pF
Clock Capacitance	$C_{CLK}$	$V_{IN} = 0\text{ V}$	5	6	pF

**Note:**

This parameter is sample tested.

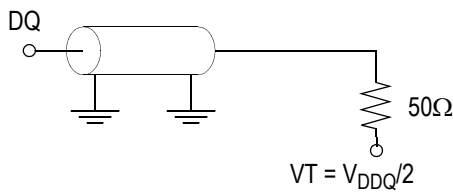
**AC Test Conditions**

Parameter	Conditions
Input high level	1.25 V
Input low level	0.25 V
Max. input slew rate	2 V/ns
Input reference level	0.75 V
Output reference level	$V_{DDQ}/2$

**Note:**

Test conditions as specified with output loading as shown unless otherwise noted.

**AC Test Load Diagram**



$R_Q = 250\ \Omega$  (HSTL I/O)  
 $V_{REF} = 0.75\text{ V}$

### Input and Output Leakage Characteristics

Parameter	Symbol	Test Conditions	Min.	Max
Input Leakage Current (except mode pins)	$I_{IL}$	$V_{IN} = 0$ to $V_{DD}$	-2 $\mu$ A	2 $\mu$ A
$\overline{\text{Doff}}$	$I_{IL\overline{\text{DOFF}}}$	$V_{IN} = 0$ to $V_{DD}$	-2 $\mu$ A	100 $\mu$ A
Output Leakage Current	$I_{OL}$	Output Disable, $V_{OUT} = 0$ to $V_{DDQ}$	-2 $\mu$ A	2 $\mu$ A

### Programmable Impedance HSTL Output Driver DC Electrical Characteristics

Parameter	Symbol	Min.	Max.	Units	Notes
Output High Voltage	$V_{OH1}$	$V_{DDQ}/2 - 0.12$	$V_{DDQ}/2 + 0.12$	V	1, 3
Output Low Voltage	$V_{OL1}$	$V_{DDQ}/2 - 0.12$	$V_{DDQ}/2 + 0.12$	V	2, 3
Output High Voltage	$V_{OH2}$	$V_{DDQ} - 0.2$	$V_{DDQ}$	V	4, 5
Output Low Voltage	$V_{OL2}$	$V_{SS}$	0.2	V	4, 6

#### Notes:

- $I_{OH} = (V_{DDQ}/2) / (RQ/5) \pm 15\%$  @  $V_{OH} = V_{DDQ}/2$  (for:  $175\Omega \leq RQ \leq 350\Omega$ ).
- $I_{OL} = (V_{DDQ}/2) / (RQ/5) \pm 15\%$  @  $V_{OL} = V_{DDQ}/2$  (for:  $175\Omega \leq RQ \leq 350\Omega$ ).
- Parameter tested with  $RQ = 250\Omega$  and  $V_{DDQ} = 1.5$  V or 1.8 V
- $0\Omega \leq RQ \leq \infty\Omega$
- $I_{OH} = -1.0$  mA
- $I_{OL} = 1.0$  mA

**Operating Currents**

Parameter	Symbol	Test Conditions	-300		-250		Notes
			0 to 70°C	-40 to 85°C	0 to 70°C	-40 to 85°C	
Operating Current (x9): DDR	$I_{DD}$	$V_{DD} = \text{Max}$ , $I_{OUT} = 0 \text{ mA}$ Cycle Time $\geq t_{KHKH} \text{ Min}$	1250 mA	1260 mA	1060 mA	1070 mA	2, 3
Operating Current (x8): DDR	$I_{DD}$	$V_{DD} = \text{Max}$ , $I_{OUT} = 0 \text{ mA}$ Cycle Time $\geq t_{KHKH} \text{ Min}$	1250 mA	1260 mA	1060 mA	1070 mA	2, 3
Standby Current (NOP): DDR	$I_{SB1}$	Device deselected, $I_{OUT} = 0 \text{ mA}$ , $f = \text{Max}$ , All Inputs $\leq 0.2 \text{ V}$ or $\geq V_{DD} - 0.2 \text{ V}$	295 mA	305 mA	275 mA	285 mA	2, 4

**Notes:**

1. Power measured with output pins floating.
2. Minimum cycle,  $I_{OUT} = 0 \text{ mA}$
3. Operating current is calculated with 50% read cycles and 50% write cycles.
4. Standby Current is only after all pending read and write burst operations are completed.

**AC Electrical Characteristics**

Parameter	Symbol	-300		-250		Units	Notes
		Min	Max	Min	Max		
<b>Clock</b>							
K, $\overline{K}$ Clock Cycle Time C, C Clock Cycle Time	$t_{KHKH}$ $t_{CHCH}$	3.3	8.4	4.0	8.4	ns	
t <sub>KC</sub> Variable	$t_{KCVar}$	—	0.2	—	0.2	ns	6
K, $\overline{K}$ Clock High Pulse Width C, C Clock High Pulse Width	$t_{KHKL}$ $t_{CHCL}$	1.32	—	1.6	—	ns	
K, $\overline{K}$ Clock Low Pulse Width C, C Clock Low Pulse Width	$t_{KLKH}$ $t_{CLCH}$	1.32	—	1.6	—	ns	
K to $\overline{K}$ High C to C High	$t_{KH\overline{H}}$ $t_{CH\overline{H}}$	1.49	—	1.8	—	ns	
$\overline{K}$ to K High C to C High	$t_{\overline{K}KH}$ $t_{\overline{C}CH}$	1.49	—	1.8	—	ns	
K, $\overline{K}$ Clock High to C, $\overline{C}$ Clock High	$t_{KHCH}$	0	1.49	0	1.8	ns	
DLL Lock Time	$t_{KCLock}$	1024	—	1024	—	cycle	7
K Static to DLL reset	$t_{KCRreset}$	30	—	30	—	ns	
<b>Output Times</b>							
K, $\overline{K}$ Clock High to Data Output Valid C, C Clock High to Data Output Valid	$t_{KHQV}$ $t_{CHQV}$	—	0.45	—	0.45	ns	4
K, $\overline{K}$ Clock High to Data Output Hold C, C Clock High to Data Output Hold	$t_{KHQX}$ $t_{CHQX}$	-0.45	—	-0.45	—	ns	4
K, $\overline{K}$ Clock High to Echo Clock Valid C, C Clock High to Echo Clock Valid	$t_{KHCQV}$ $t_{CHCQV}$	—	0.45	—	0.45	ns	
K, $\overline{K}$ Clock High to Echo Clock Hold C, C Clock High to Echo Clock Hold	$t_{KHCQX}$ $t_{CHCQX}$	-0.45	—	-0.45	—	ns	
CQ, $\overline{CQ}$ High Output Valid	$t_{CQHQV}$	—	0.27	—	0.30	ns	8
CQ, $\overline{CQ}$ High Output Hold	$t_{CQHQX}$	-0.27	—	-0.30	—	ns	8
CQ Phase Distortion	$t_{CQH\overline{CQH}}$ $t_{\overline{CQH}CQH}$	1.24	—	1.55	—	ns	
K Clock High to Data Output High-Z C Clock High to Data Output High-Z	$t_{KHQZ}$ $t_{CHQZ}$	—	0.45	—	0.45	ns	4
K Clock High to Data Output Low-Z C Clock High to Data Output Low-Z	$t_{KHQX1}$ $t_{CHQX1}$	-0.45	—	-0.45	—	ns	4
<b>Setup Times</b>							
Address Input Setup Time	$t_{AVKH}$	0.3	—	0.35	—	ns	1
Control Input Setup Time ( $\overline{R}$ , $\overline{W}$ )	$t_{IVKH}$	0.3	—	0.35	—	ns	2
Control Input Setup Time ( $\overline{BW\overline{X}}$ ) ( $BW\overline{X}$ )	$t_{IVKH}$	0.3	—	0.35	—	ns	3
Data Input Setup Time	$t_{DVKH}$	0.3	—	0.35	—	ns	

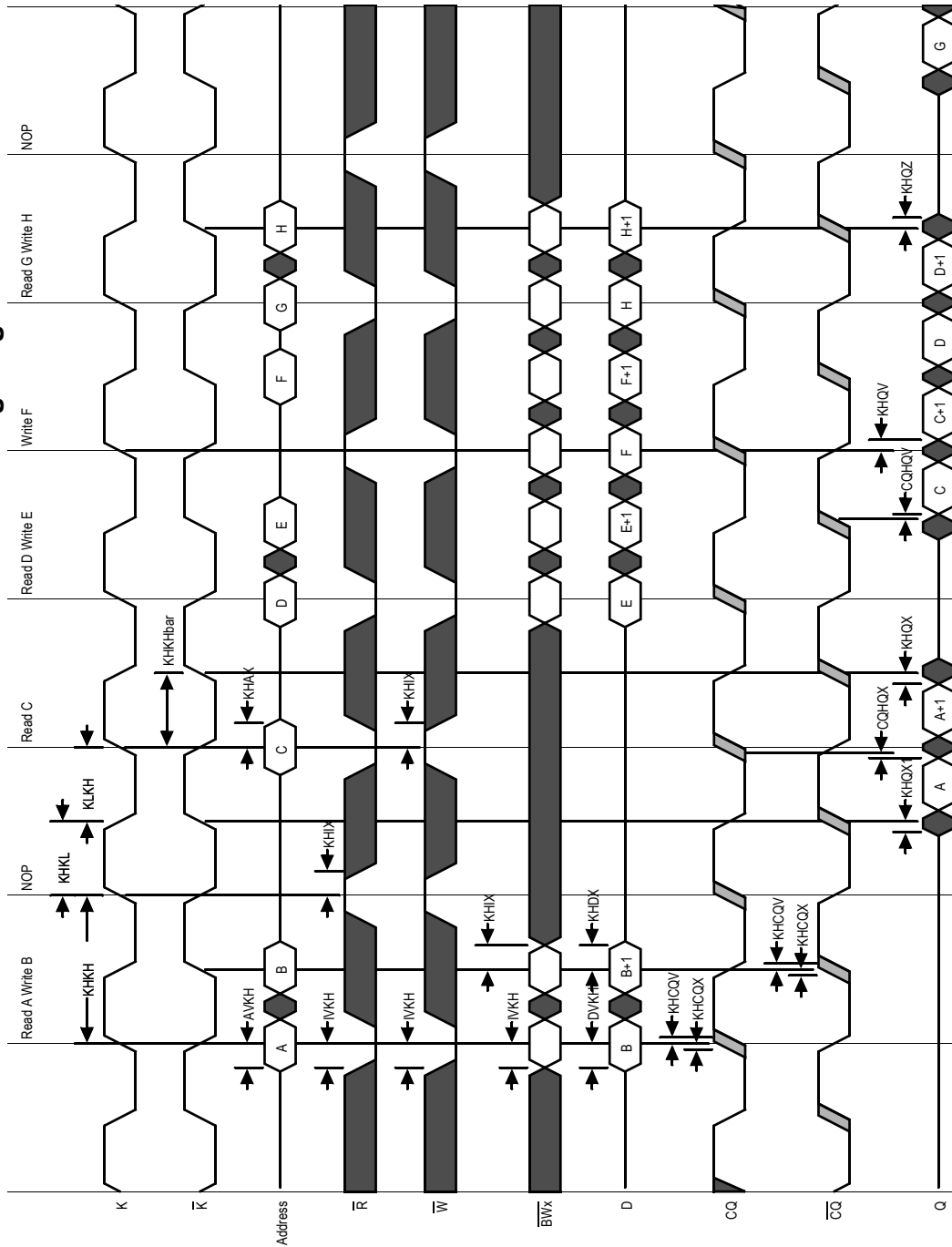
**AC Electrical Characteristics (Continued)**

Parameter	Symbol	-300		-250		Units	Notes
		Min	Max	Min	Max		
<b>Hold Times</b>							
Address Input Hold Time	$t_{KHAX}$	0.3	—	0.35	—	ns	1
Control Input Hold Time ( $\overline{R}$ , $\overline{W}$ )	$t_{KHIX}$	0.3	—	0.35	—	ns	2
Control Input Hold Time ( $\overline{BWX}$ ) ( $\overline{BWX}$ )	$t_{KHIX}$	0.3	—	0.35	—	ns	3
Data Input Hold Time	$t_{KHDX}$	0.3	—	0.35	—	ns	

**Notes:**

1. All Address inputs must meet the specified setup and hold times for all latching clock edges.
2. Control signals are  $\overline{R}$ ,  $\overline{W}$
3. Control signals are  $\overline{BW0}$  for x9, and  $\overline{NW0}$ ,  $\overline{NW1}$  for x8).
4. If  $\overline{C}$ ,  $\overline{C}$  are tied high,  $\overline{K}$ ,  $\overline{K}$  become the references for  $\overline{C}$ ,  $\overline{C}$  timing parameters
5. To avoid bus contention, at a given voltage and temperature  $t_{CHQX1}$  is bigger than  $t_{CHQZ}$ . The specs as shown do not imply bus contention because  $t_{CHQX1}$  is a MIN parameter that is worst case at totally different test conditions (0°C, 1.9 V) than  $t_{CHQZ}$ , which is a MAX parameter (worst case at 70°C, 1.7 V). It is not possible for two SRAMs on the same board to be at such different voltages and temperatures.
6. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge.
7.  $V_{DD}$  slew rate must be less than 0.1 V DC per 50 ns for DLL lock retention. DLL lock time begins once  $V_{DD}$  and input clock are stable.
8. Echo clock is very tightly controlled to data valid/data hold. By design, there is a  $\pm 0.1$  ns variation from echo clock to data. The datasheet parameters reflect tester guard bands and test setup variations.

**K and K Controlled Read-Write-Read Timing Diagram**





## JTAG Port Operation

### Overview

The JTAG Port on this RAM operates in a manner that is compliant with IEEE Standard 1149.1-1990, a serial boundary scan interface standard (commonly referred to as JTAG). The JTAG Port input interface levels scale with  $V_{DD}$ . The JTAG output drivers are powered by  $V_{DD}$ .

### Disabling the JTAG Port

It is possible to use this device without utilizing the JTAG port. The port is reset at power-up and will remain inactive unless clocked. TCK, TDI, and TMS are designed with internal pull-up circuits. To assure normal operation of the RAM with the JTAG Port unused, TCK, TDI, and TMS may be left floating or tied to either  $V_{DD}$  or  $V_{SS}$ . TDO should be left unconnected.

## JTAG Pin Descriptions

Pin	Pin Name	I/O	Description
TCK	Test Clock	In	Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.
TMS	Test Mode Select	In	The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will produce the same result as a logic one input level.
TDI	Test Data In	In	The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP Controller state machine and the instruction that is currently loaded in the TAP Instruction Register (refer to the TAP Controller State Diagram). An undriven TDI pin will produce the same result as a logic one input level.
TDO	Test Data Out	Out	Output that is active depending on the state of the TAP state machine. Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

### Note:

This device does not have a TRST (TAP Reset) pin. TRST is optional in IEEE 1149.1. The Test-Logic-Reset state is entered while TMS is held high for five rising edges of TCK. The TAP Controller is also reset automatically at power-up.

## JTAG Port Registers

### Overview

The various JTAG registers, referred to as Test Access Port or TAP Registers, are selected (one at a time) via the sequences of 1s and 0s applied to TMS as TCK is strobed. Each of the TAP Registers is a serial shift register that captures serial input data on the rising edge of TCK and pushes serial data out on the next falling edge of TCK. When a register is selected, it is placed between the TDI and TDO pins.

### Instruction Register

The Instruction Register holds the instructions that are executed by the TAP controller when it is moved into the Run, Test/Idle, or the various data register states. Instructions are 3 bits long. The Instruction Register can be loaded when it is placed between the TDI and TDO pins. The Instruction Register is automatically preloaded with the IDCODE instruction at power-up or whenever the controller is placed in Test-Logic-Reset state.

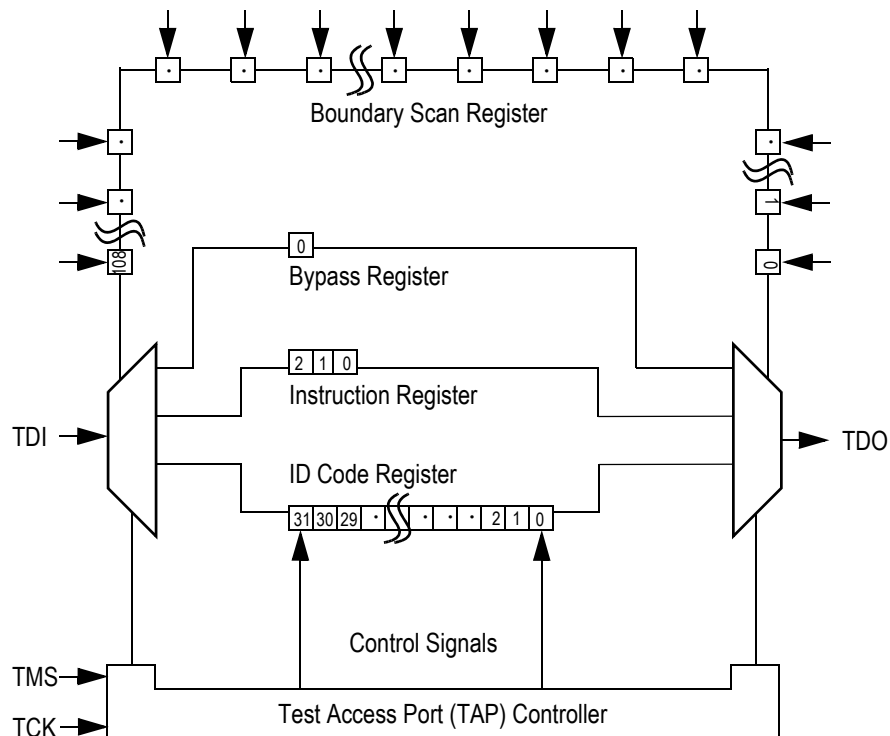
### Bypass Register

The Bypass Register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAM's JTAG Port to another device in the scan chain with as little delay as possible.

### Boundary Scan Register

The Boundary Scan Register is a collection of flip flops that can be preset by the logic level found on the RAM's input or I/O pins. The flip flops are then daisy chained together so the levels found can be shifted serially out of the JTAG Port's TDO pin. The Boundary Scan Register also includes a number of place holder flip flops (always set to a logic 1). The relationship between the device pins and the bits in the Boundary Scan Register is described in the Scan Order Table following. The Boundary Scan Register, under the control of the TAP Controller, is loaded with the contents of the RAMs I/O ring when the controller is in Capture-DR state and then is placed between the TDI and TDO pins when the controller is moved to Shift-DR state. SAMPLE-Z, SAMPLE/PRELOAD and EXTEST instructions can be used to activate the Boundary Scan Register.

### JTAG TAP Block Diagram



### Identification (ID) Register

The ID Register is a 32-bit register that is loaded with a device and vendor specific 32-bit code when the controller is put in Capture-DR state with the IDCODE command loaded in the Instruction Register. The code is loaded from a 32-bit on-chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into Shift-DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

**ID Register Contents**

See BSDL Model																		GSI Technology JEDEC Vendor ID Code								Presence Register						
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	0	1	1	0	1	1	0	0	1	1

**Tap Controller Instruction Set**

**Overview**

There are two classes of instructions defined in the Standard 1149.1-1990; the standard (Public) instructions, and device specific (Private) instructions. Some Public instructions are mandatory for 1149.1 compliance. Optional Public instructions must be implemented in prescribed ways. The TAP on this device may be used to monitor all input and I/O pads, and can be used to load address, data or control signals into the RAM or to preload the I/O buffers.

When the TAP controller is placed in Capture-IR state the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the Shift-IR state the Instruction Register is placed between TDI and TDO. In this state the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to Update-IR state. The TAP instruction set for this device is listed in the following table.



Typically, the Boundary Scan Register is loaded with the desired pattern of data with the SAMPLE/PRELOAD command. Then the EXTEST command is used to output the Boundary Scan Register's contents, in parallel, on the RAM's data output drivers on the falling edge of TCK when the controller is in the Update-IR state.

Alternately, the Boundary Scan Register may be loaded in parallel using the EXTEST command. When the EXTEST instruction is selected, the state of all the RAM's input and I/O pins, as well as the default values at Scan Register locations not associated with a pin, are transferred in parallel into the Boundary Scan Register on the rising edge of TCK in the Capture-DR state, the RAM's output pins drive out the value of the Boundary Scan Register location with which each output pin is associated.

#### **IDCODE**

The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in Capture-DR mode and places the ID register between the TDI and TDO pins in Shift-DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the Test-Logic-Reset state.

#### **SAMPLE-Z**

If the SAMPLE-Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (high-Z) and the Boundary Scan Register is connected between TDI and TDO when the TAP controller is moved to the Shift-DR state.

#### **JTAG TAP Instruction Set Summary**

<b>Instruction</b>	<b>Code</b>	<b>Description</b>	<b>Notes</b>
EXTEST	000	Places the Boundary Scan Register between TDI and TDO.	1
IDCODE	001	Preloads ID Register and places it between TDI and TDO.	1, 2
SAMPLE-Z	010	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO. Forces all RAM output drivers to High-Z.	1
GSI	011	GSI private instruction.	1
SAMPLE/PRELOAD	100	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO.	1
GSI	101	GSI private instruction.	1
GSI	110	GSI private instruction.	1
BYPASS	111	Places Bypass Register between TDI and TDO.	1

#### **Notes:**

1. Instruction codes expressed in binary, MSB on left, LSB on right.
2. Default instruction automatically loaded at power-up and in test-logic-reset state.

### JTAG Port Recommended Operating Conditions and DC Characteristics

Parameter	Symbol	Min.	Max.	Unit	Notes
Test Port Input Low Voltage	$V_{ILJ}$	-0.3	$0.3 * V_{DD}$	V	1
Test Port Input High Voltage	$V_{IHJ}$	$0.7 * V_{DD}$	$V_{DD} + 0.3$	V	1
TMS, TCK and TDI Input Leakage Current	$I_{INHJ}$	-300	1	uA	2
TMS, TCK and TDI Input Leakage Current	$I_{INLJ}$	-1	100	uA	3
TDO Output Leakage Current	$I_{OLJ}$	-1	1	uA	4
Test Port Output High Voltage	$V_{OHJ}$	$V_{DD} - 0.2$	—	V	5, 6
Test Port Output Low Voltage	$V_{OLJ}$	—	0.2	V	5, 7
Test Port Output CMOS High	$V_{OHJC}$	$V_{DD} - 0.1$	—	V	5, 8
Test Port Output CMOS Low	$V_{OLJC}$	—	0.1	V	5, 9

#### Notes:

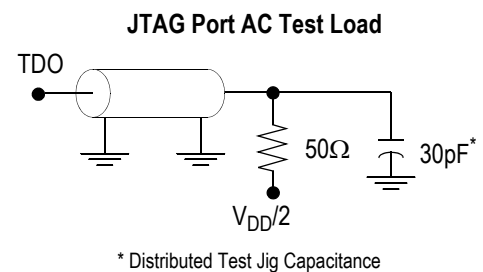
- Input Under/overshoot voltage must be  $-1 V < V_i < V_{DDn} + 1 V$  not to exceed 2.9 V maximum, with a pulse width not to exceed 20% tTKC.
- $V_{ILJ} \leq V_{IN} \leq V_{DDn}$
- $0 V \leq V_{IN} \leq V_{ILJn}$
- Output Disable,  $V_{OUT} = 0$  to  $V_{DDn}$
- The TDO output driver is served by the  $V_{DD}$  supply.
- $I_{OHJ} = -2$  mA
- $I_{OLJ} = +2$  mA
- $I_{OHJC} = -100$  uA
- $I_{OLJC} = +100$  uA

### JTAG Port AC Test Conditions

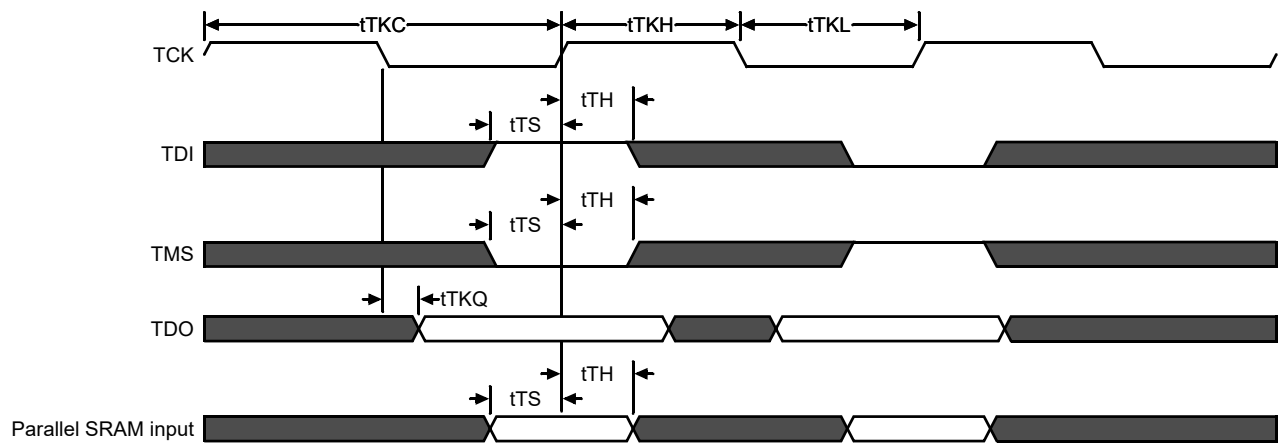
Parameter	Conditions
Input high level	$V_{DD} - 0.2 V$
Input low level	0.2 V
Input slew rate	1 V/ns
Input reference level	$V_{DD}/2$
Output reference level	$V_{DD}/2$

#### Notes:

- Include scope and jig capacitance.
- Test conditions as shown unless otherwise noted.



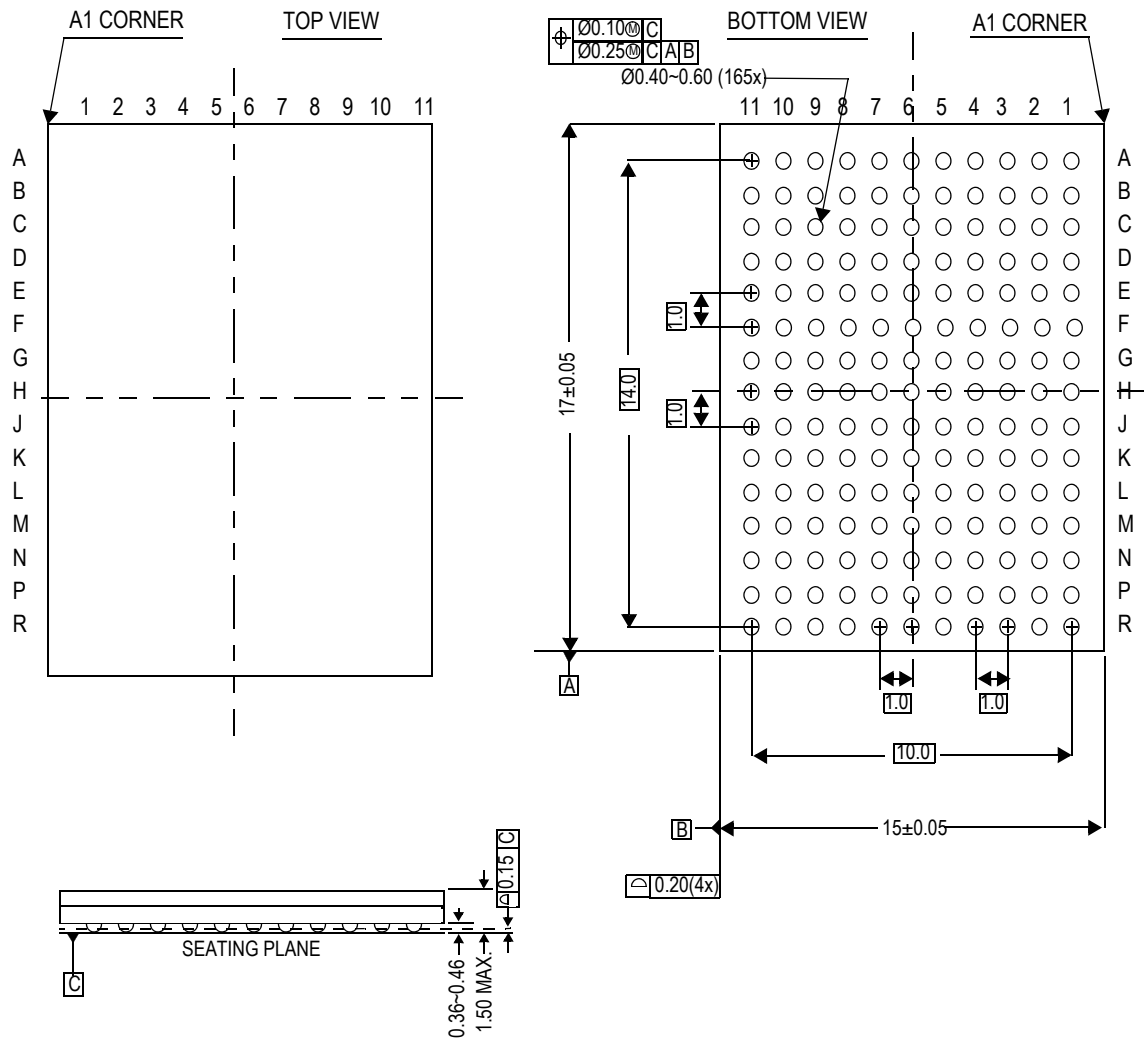
### JTAG Port Timing Diagram



### JTAG Port AC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
TCK Cycle Time	$t_{TKC}$	50	—	ns
TCK Low to TDO Valid	$t_{TKQ}$	—	20	ns
TCK High Pulse Width	$t_{TKH}$	20	—	ns
TCK Low Pulse Width	$t_{TKL}$	20	—	ns
TDI & TMS Set Up Time	$t_{TS}$	10	—	ns
TDI & TMS Hold Time	$t_{TH}$	10	—	ns

Package Dimensions—165-Bump FPBGA (Package E)



**Ordering Information—GSI SigmaQuad-II SRAM**

Org	Part Number <sup>1</sup>	Type	Package	Speed (MHz)	T <sub>J</sub> <sup>2</sup>
16M x 9	GS81302Q09E-300	SigmaQuad-II SRAM	165-bump BGA	300	C
16M x 9	GS81302Q09E-250	SigmaQuad-II SRAM	165-bump BGA	250	C
16M x 9	GS81302Q09E-300I	SigmaQuad-II SRAM	165-bump BGA	300	I
16M x 9	GS81302Q09E-250I	SigmaQuad-II SRAM	165-bump BGA	250	I
16M x 8	GS81302Q08E-300	SigmaQuad-II SRAM	165-bump BGA	300	C
16M x 8	GS81302Q08E-250	SigmaQuad-II SRAM	165-bump BGA	250	C
16M x 8	GS81302Q08E-300I	SigmaQuad-II SRAM	165-bump BGA	300	I
16M x 8	GS81302Q08E-250I	SigmaQuad-II SRAM	165-bump BGA	250	I
16M x 9	GS81302Q09GE-300	SigmaQuad-II SRAM	RoHS-compliant 165-bump BGA	300	C
16M x 9	GS81302Q09GE-250	SigmaQuad-II SRAM	RoHS-compliant 165-bump BGA	250	C
16M x 9	GS81302Q09GE-300I	SigmaQuad-II SRAM	RoHS-compliant 165-bump BGA	300	I
16M x 9	GS81302Q09GE-250I	SigmaQuad-II SRAM	RoHS-compliant 165-bump BGA	250	I
16M x 8	GS81302Q08GE-300	SigmaQuad-II SRAM	RoHS-compliant 165-bump BGA	300	C
16M x 8	GS81302Q08GE-250	SigmaQuad-II SRAM	RoHS-compliant 165-bump BGA	250	C
16M x 8	GS81302Q08GE-300I	SigmaQuad-II SRAM	RoHS-compliant 165-bump BGA	300	I
16M x 8	GS81302Q08GE-250I	SigmaQuad-II SRAM	RoHS-compliant 165-bump BGA	250	I

**Notes:**

1. Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. Example: GS81302Q36E-250T.
2. C = Commercial Temperature Range. I = Industrial Temperature Range.

**SigmaQuad-II Revision History**

File Name	Format/Content	Description of changes
81302Qxx_r1		Creation of datasheet
81302Qxx_r1.00a	Editorial	Corrected Ordering Information Table
81302Qxx_r1.01	Content	Updated AC Characteristics Table Updated 165 BGA Package Drawing Updated JTAG Port Operation Section
81302Qxx_r1.02	Content	Added 300 MHz speed bin to Q (Rev1.02a: removed CQ reference from SAMPLE-Z section in JTAG Tap Instruction Set Summary) (Rev1.02b: Updated DLL Lock time to 2048 cycles)
81302Qxx_r1.03	Content	Added 333 MHz speed bin to Q Removed 200 & 167 speed bins (Rev1.03a: fixed erroneous data in AC Char table)
81302Qxx_r1.04	Content	Added Op Currents Removed Preliminary banner due to MP status (Rev1.04a: Editorial updates) (Rev1.04b: Updated DLL lock time in AC Char table) (Rev1.04c: Removed 333 MHz from B2 datasheet) (Rev1.04c: Corrected erroneous information in Input and Output Leakage Characteristics table)
81302Qxx_r1.05	Content	Removed all references to x18/x36 due to NRND