TENTATIVE TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

2,097,152-WORD BY 8-BIT EDO (HYPER PAGE) DYNAMIC RAM

DESCRIPTION

The TC5117805CJS/CFTS/CSJS/CSTS is an EDO (hyper page) dynamic RAM organized as 2,097,152 words by 8 bits. The TC5117800CJS/CFTS/CSJS/CSTS utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC5117805BNJS/BNTS to be packaged in a 28-pin plastic SOJ or a 28-pin plastic TSOP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System-oriented features include a single power supply of 5 V ± 10% and direct interfacing capability with high-performance logic families such as Schottky TTL.

FEATURES

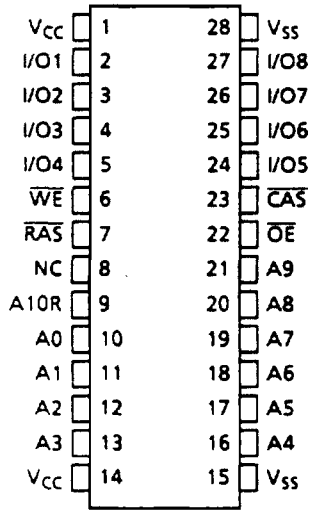
- 2,097,152-word by 8-bit organization
- Fast access and cycle times

		TC5117805CJS/CFTS /CSJS/CSTS
		-60
t_{RAC}	$\overline{RAS}$ Access Time	60ns
t_{AA}	Column Address Access Time	30ns
t_{CAC}	$\overline{CAS}$ Access Time	17ns
t_{RC}	Cycle Time	104ns
t_{HPC}	Hyper Page Mode Cycle Time	25ns

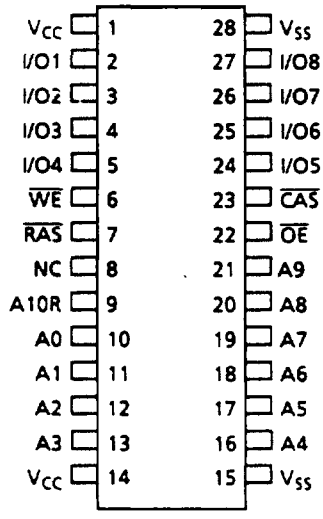
- Single power supply of 5 V ± 10% with built-in V_{BB} generator
- Low power dissipation (max)
  Operating: 770 mW (60 ns type)
  Standby: 1.65 mW (all devices)
- Unlatched outputs at cycle end allows two-dimensional chip selection
- Read-modify-write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, hidden refresh, self-refresh, Test mode and EDO (Hyper Page mode) capability
- All inputs and outputs are TTL-compatible
- 2048 refresh cycles per 64 ms
- Packages:
  CJS : SOJ28-P-400-1.27C, 1.13 grams
  CFTS : TSOPII 28-P-400-1.27, 0.47 grams
  CSJS : SOJ28-P-300-1.27B, 0.78 grams
  CSTS : TSOPII 28-P-300-1.27E, 0.32 grams

PIN ASSIGNMENT (TOP VIEW)

Plastic SOJ
TC5117805CJS/CSJS



Plastic TSOP
TC5117805CFTS/CSTS

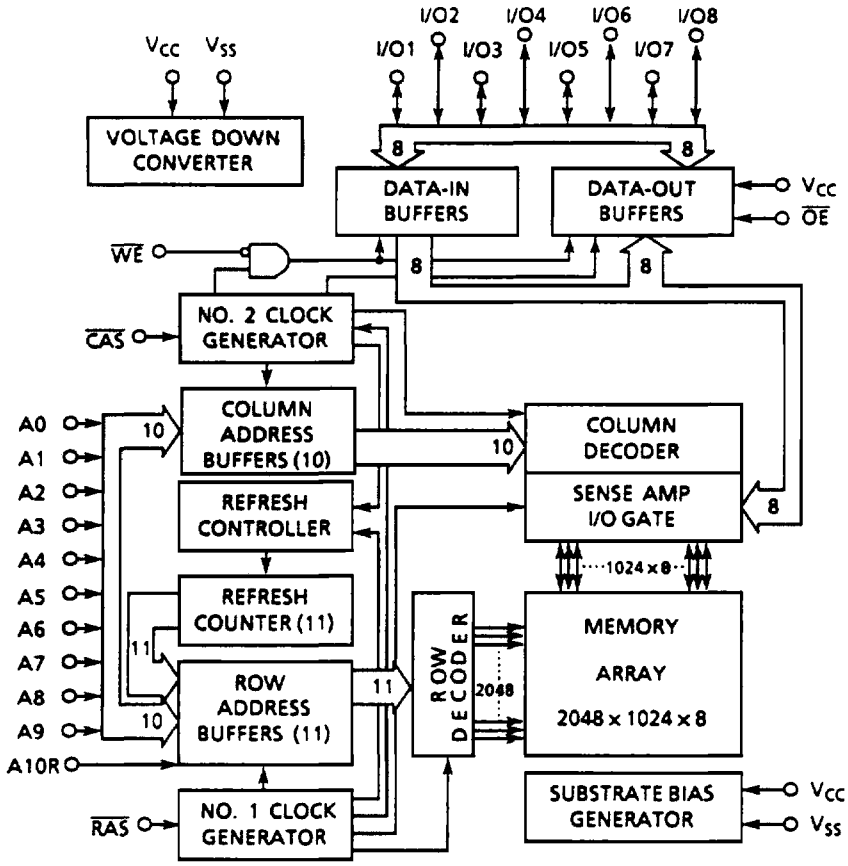


PIN NAMES

A0 to A10	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
I/O1 to I/O8	Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

961001EBA1

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT	NOTES
Input Voltage	V_{IN}	− 0.5 to Vcc + 0.5	V	1
Output Voltage	V_{OUT}	− 0.5 to Vcc + 0.5	V	1
Power Supply Voltage	V_{CC}	− 0.5 to 7.0	V	1
Operating Temperature	T_{OPR}	0 to 70	°C	1
Storage Temperature	T_{STG}	− 55 to 150	°C	1
Soldering Temperature (10 s)	T_{SOLDER}	260	°C	1
Power Dissipation	P_D	1.0	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0° to 70°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	V_{CC} + 0.5*	V	2
V_{IL}	Input Low Voltage	− 0.5**	−	0.8	V	2

* Vcc + 2.0V with pulse width ≤ 20ns (pulse width is measured at Vcc)

** − 2.0V with pulse width ≤ 20ns (pulse width is measured at Vss)

DC CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0° to 70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $t_{RC} = t_{RC}$ min)	–	140	mA	3, 4, 5
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{IH}$)	–	2	mA	
I_{CC3}	$\overline{RAS}$-ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$-only Mode ($\overline{RAS}$ Cycling, $\overline{CAS} = V_{IH}$: $t_{RC} = t_{RC}$ min)	–	140	mA	3, 5
I_{CC4}	HYPER PAGE MODE CURRENT Average Power Supply Current, Hyper Page Mode ($\overline{RAS} = V_{IL}$, $\overline{CAS}$, Address Cycling: $t_{HPC} = t_{HPC}$ min)	–	115	mA	3, 4, 5
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2V$)	–	300	μA	
I_{CC6}	$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$-before-$\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: $t_{RC} = t_{RC}$ min)	–	140	mA	3, 5
I_{CC7}	BATTERY BACK-UP CURRENT Average Power Supply Current, Battery Back-up Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = $\overline{CAS}$-before-$\overline{RAS}$ Cycling or 0.2V, $\overline{OE}$, $\overline{WE}$, A0 to A9, A10R = V_{CC} – 0.2V or 0.2V, I/O1 to I/O8 = V_{CC} – 0.2V, 0.2V or Hi-Z: $t_{RC} = 31.2\mu s$ $t_{RAS} = t_{RAS}$ min to 300ns)	–	700	μA	3
I_{CC8}	SELF REFRESH CURRENT Average Power Supply Current, Self Refresh Mode ($\overline{RAS} = \overline{CAS} = V_{IL}$, $\overline{OE}$, $\overline{WE}$, A0 to A9, A10R = V_{CC} – 0.2V or 0.2V, I/O1 to I/O8 = V_{CC} – 0.2V, 0.2V or Hi-Z)	–	600	μA	
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, Any Input (0V ≤ V_{IN} ≤ Vcc, All Other Pins Not under Test = 0V)	– 10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} Is Disabled, 0V ≤ V_{OUT} ≤ Vcc)	– 10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)	2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)	–	0.4	V	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0° to 70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_{I1}	Input Capacitance (A0 to A10)	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	–	7	pF
C_O	Input/Output Capacitance (I/O1 to I/O8)	–	7	pF

AC CHARACTERISTICS AND OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0° to 70°C) (Notes 6, 7, 8)

SYMBOL	PARAMETER	TC5117805CJS/CFTS/CSJS/CSTS -60		UNIT	NOTES
		MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	104	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	135	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	60	ns	9,14,15
t_{CAC}	Access Time from $\overline{CAS}$	–	17	ns	9,14
t_{AA}	Access Time from Column Address	–	30	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	35	ns	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	–	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	15	ns	10,16
t_T	Transition Time (Rise and Fall)	1	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	40	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Hyper Page Mode)	60	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	10	–	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge (Hyper Page Mode)	35	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	40	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	10	10,000	ns	
t_{RCD}	$\overline{RAS}$-to-$\overline{CAS}$ Delay Time	14	43	ns	14
t_{RAD}	$\overline{RAS}$-to-Column-Address Delay Time	12	30	ns	15
t_{CRP}	$\overline{CAS}$-to-$\overline{RAS}$ Precharge Time	5	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	–	ns	
t_{ASR}	Row Address Set-up Time	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	ns	
t_{ASC}	Column Address Set-up Time	0	–	ns	
t_{CAH}	Column Address Hold Time	10	–	ns	
t_{RAL}	Column-Address-to-$\overline{RAS}$ Lead Time	30	–	ns	
t_{RCS}	Read Command Set-up Time Referenced to $\overline{RAS}$	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	ns	11
t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0	–	ns	11
t_{WCH}	Write Command Hold Time	10	–	ns	

AC CHARACTERISTICS AND OPERATING CONDITIONS

(Continued)

SYMBOL	PARAMETER	TC5117805CJS/CFTS/CSJS/CSTS -60		UNIT	NOTES
		MIN	MAX		
t_{WP}	Write Command Pulse Width	10	-	ns	
t_{RWL}	Write-Command-to-$\overline{RAS}$ Lead Time	10	-	ns	
t_{CWL}	Write-Command-to-$\overline{CAS}$ Lead Time	10	-	ns	
t_{DS}	Data Set-up Time	0	-	ns	12
t_{DH}	Data Hold Time	10	-	ns	12
t_{REF}	Refresh Period	-	64	ms	
t_{WCS}	Write Command Set-up Time	0	-	ns	13
t_{CWD}	$\overline{CAS}$-to-$\overline{WE}$ Delay Time	36	-	ns	13
t_{RWD}	$\overline{RAS}$-to-$\overline{WE}$ Delay Time	79	-	ns	13
t_{AWD}	Column-Address-to-$\overline{WE}$ Delay Time	49	-	ns	13
t_{CPWD}	$\overline{CAS}$-Precharge-to-$\overline{WE}$ Delay Time	54	-	ns	13
t_{CSR}	$\overline{CAS}$ Set-up Time ($\overline{CAS}$-before-$\overline{RAS}$ Cycle)	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Cycle)	10	-	ns	
t_{RPC}	$\overline{RAS}$-to-$\overline{CAS}$ Precharge Time	5	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$-before-$\overline{RAS}$ Counter Test Cycle)	20	-	ns	
t_{ROH}	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	10	-	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	15	ns	9
t_{OED}	$\overline{OE}$-to-Data Delay	15	-	ns	
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	0	-	ns	
t_{OEZ}	Output Buffer Turn-off Delay Time from $\overline{OE}$	0	15	ns	10
t_{OEH}	$\overline{OE}$ Command Hold Time	10	-	ns	
t_{ODS}	Output Disable Set-up Time	0	-	ns	
t_{WTS}	Write Command Set-up Time (Test Mode)	10	-	ns	
t_{WTH}	Write Command Hold Time (Test Mode)	10	-	ns	
t_{WRP}	$\overline{WE}$-to-$\overline{RAS}$ Precharge Time ($\overline{CAS}$-before-$\overline{RAS}$ Cycle)	10	-	ns	
t_{WRH}	$\overline{WE}$-to-$\overline{RAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Cycle)	10	-	ns	
t_{RASS}	$\overline{RAS}$ Pulse Width ($\overline{CAS}$-before-$\overline{RAS}$ Self Refresh)	100	-	μs	
t_{RPS}	$\overline{RAS}$ Precharge Time ($\overline{CAS}$-before-$\overline{RAS}$ Self Refresh)	104	-	ns	
t_{CHS}	$\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Self Refresh)	-50	-	ns	

AC CHARACTERISTICS AND OPERATING CONDITIONS

(Continued)

SYMBOL	PARAMETER	TC5117805CJS/CFTS/CSJS/CSTS -60		UNIT	NOTES
		MIN	MAX		
t_{RNCD}	$\overline{RAS}$-to-Next-$\overline{CAS}$ Delay Time (Hyper Page Mode)	60	–	ns	
t_{HPC}	Hyper Page Mode Cycle Time	25	–	ns	
t_{HPRWC}	Hyper Page Mode Read-Modify-Write Cycle Time	68	–	ns	
t_{COH}	Output Data Hold Time	5	–	ns	
t_{REZ}	Output Buffer Turn-off Delay from $\overline{RAS}$	0	15	ns	10,16
t_{WEZ}	Output Buffer Turn-off Delay from $\overline{WE}$	0	15	ns	10
t_{WED}	$\overline{WE}$-to-Data Delay	15	–	ns	
t_{OE}	$\overline{OE}$ Pulse Width	15	–	ns	
t_{OEP}	$\overline{OE}$ Precharge Time	10	–	ns	
t_{CPO}	$\overline{CAS}$-to-$\overline{OE}$ Precharge Time	5	–	ns	
t_{OCH}	$\overline{CAS}$ Hold Time referenced to $\overline{OE}$	10	–	ns	

AC CHARACTERISTICS AND OPERATING CONDITIONS IN TEST MODE

SYMBOL	PARAMETER	TC5117805CJS/CFTS/CSJS/CSTS -60		UNIT	NOTES
		MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	109	–	ns	
t_{HPC}	Hyper Page Mode Cycle Time	30	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	65	ns	9,14,15
t_{CAC}	Access Time from $\overline{CAS}$	–	22	ns	9,14
t_{AA}	Access Time from Column Address	–	35	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	40	ns	9
t_{RAS}	$\overline{RAS}$ Pulse Width	65	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Hyper Page Mode)	65	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	15	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	45	–	ns	
t_{RHCP}	$\overline{CAS}$-Precharge-to-$\overline{RAS}$ Hold Time	40	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	10,000	ns	
t_{RAL}	Column-Address-to-$\overline{RAS}$ Lead Time	35	–	ns	

NOTES

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on the cycle rate.
4. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In case of I_{CC4}, it can be changed once or less during a Hyper Page mode cycle (t_{HPC}).
6. An initial pause of 200 μs is required after power-up followed by eight $\overline{RAS}$-only refresh cycles before proper device operation is achieved. When using the internal refresh counter, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of eight $\overline{RAS}$-only refresh cycles is required.
7. AC measurements assume t_T = 2 ns.
8. V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Also, transition times are measured between the V_{IH} and V_{IL} levels.
9. Measured with a load equivalent to two TTL loads and 100 pF.
10. Parameters t_{OFF} (max) and t_{OEZ} (max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WE}$ leading edge in read-modify-write cycles.
13. Parameters t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data-out pin will remain open circuit (high impedance) throughout the entire cycle. If $t_{RWD} \geqq t_{RWD}$ (min), $t_{CWD} \geqq t_{CWD}$ (min), $t_{AWD} \geqq t_{AWD}$ (min) and $t_{CPWD} \geqq t_{CPWD}$ (min) (Hyper Page mode), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the data output (at access time) is indeterminate.
14. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. Parameter t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. Parameter t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
16. If $\overline{RAS}$ goes high before $\overline{CAS}$ goes high, the output goes open circuit when $\overline{CAS}$ goes high (t_{OFF}). If $\overline{CAS}$ goes high before $\overline{RAS}$ goes high, the output goes open circuit when $\overline{RAS}$ goes high (t_{REZ}).

DATA-OUT HI-Z CONTROL LOGIC

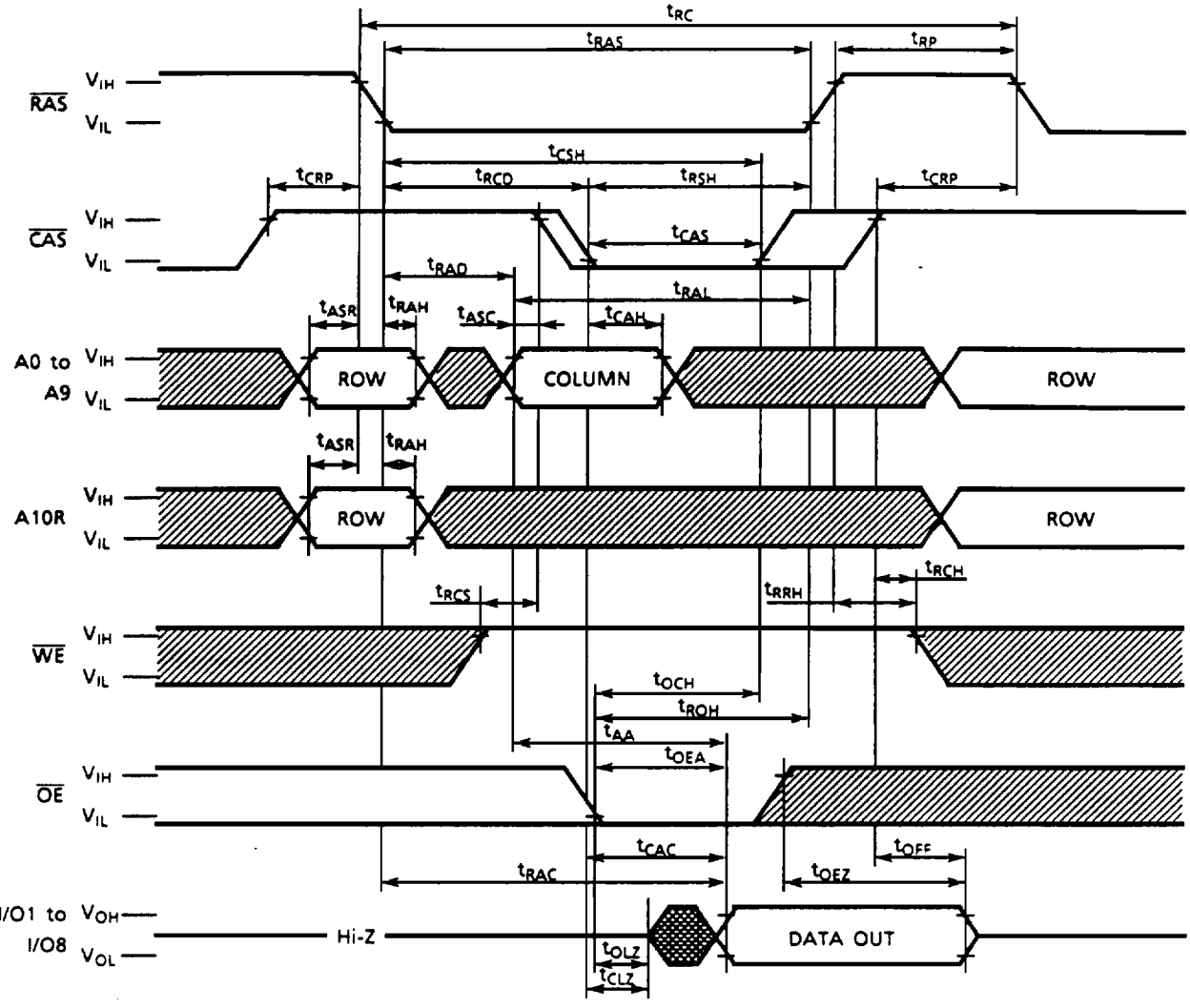
$\overline{RAS}$	$\overline{CAS}$	$\overline{OE}$	$\overline{WE}$	TIMING SPECIFICATION
"H"		"L"	"H"	t_{OFF}
	"H"	"L"	"H"	t_{REZ}
"L"	"L"		"H"	t_{OEZ}
"L"	"H"	"L"		t_{WEZ}

DATA-OUT LO-Z CONTROL LOGIC

$\overline{RAS}$	$\overline{CAS}$	$\overline{OE}$	$\overline{WE}$	TIMING SPECIFICATION
"L"		"L"	"H"	t_{CLZ}
"L"	"L"		"H"	t_{OLZ}
"L"	"L"		"H"	t_{OLZ}

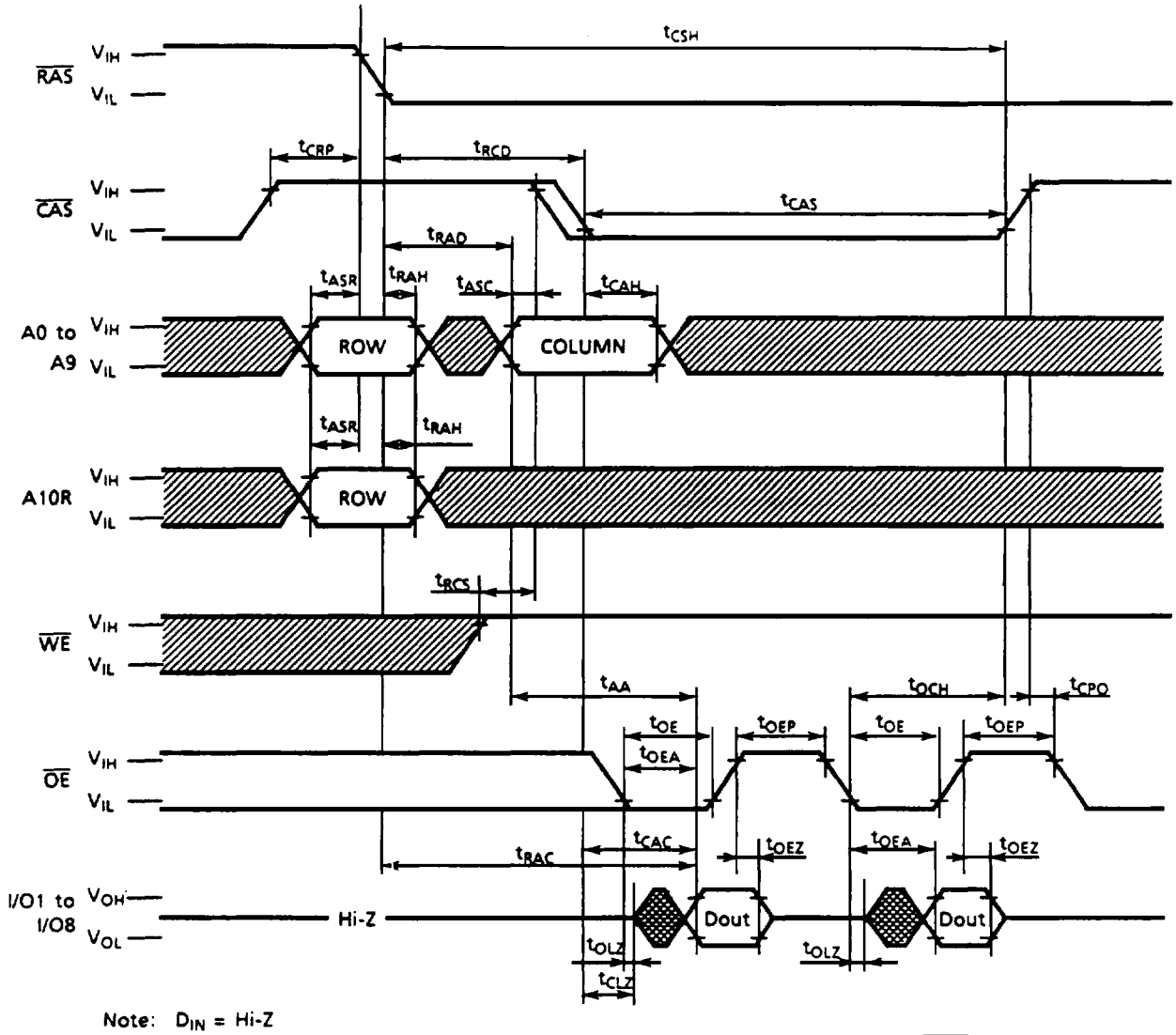
TIMING DIAGRAMS

READ CYCLE



Note: D_{IN} = Hi-Z

$\overline{OE}$ CONTROLLED READ CYCLE

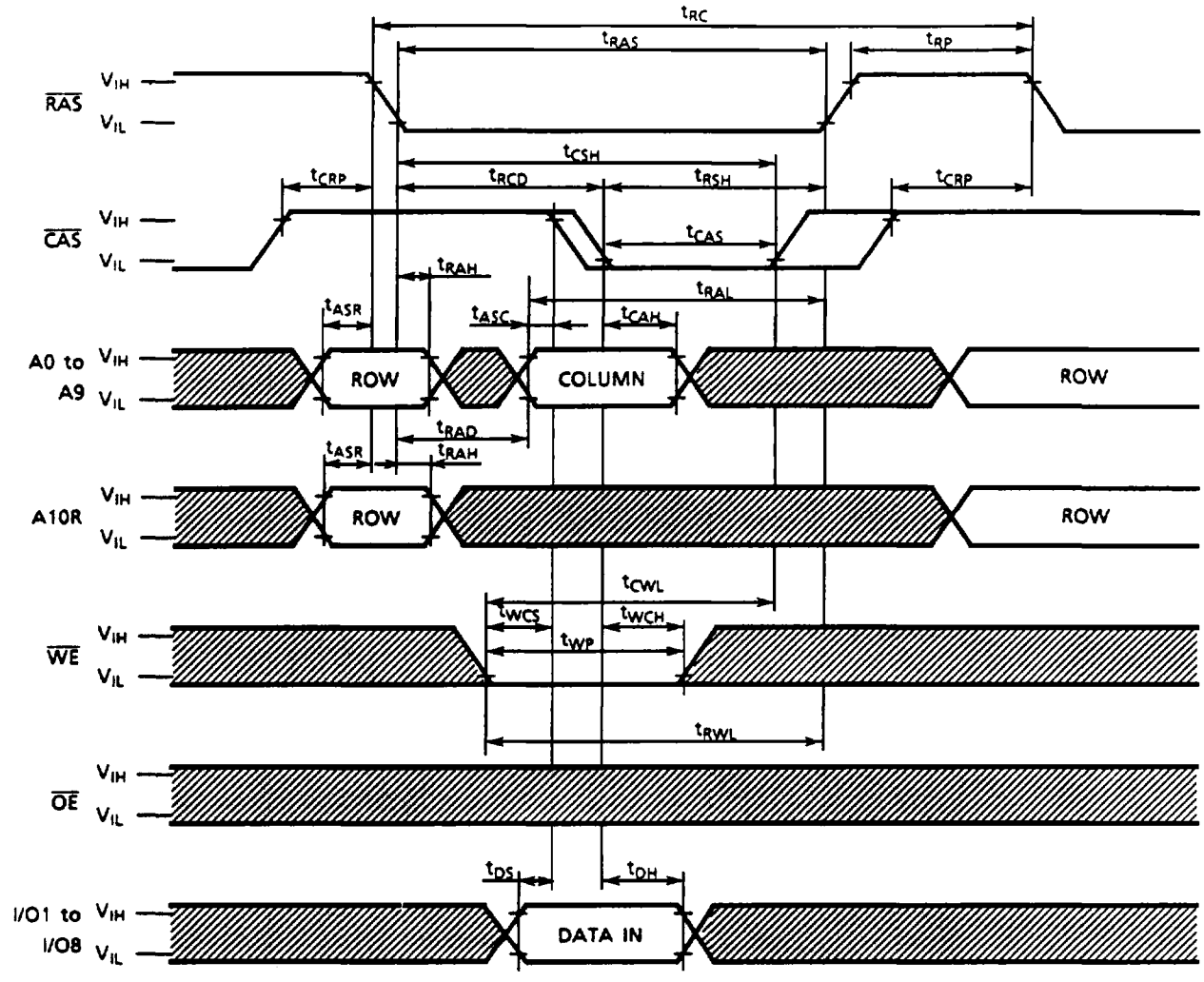


Note: D_{IN} = Hi-Z

: "H" or "L"

: Invalid Data

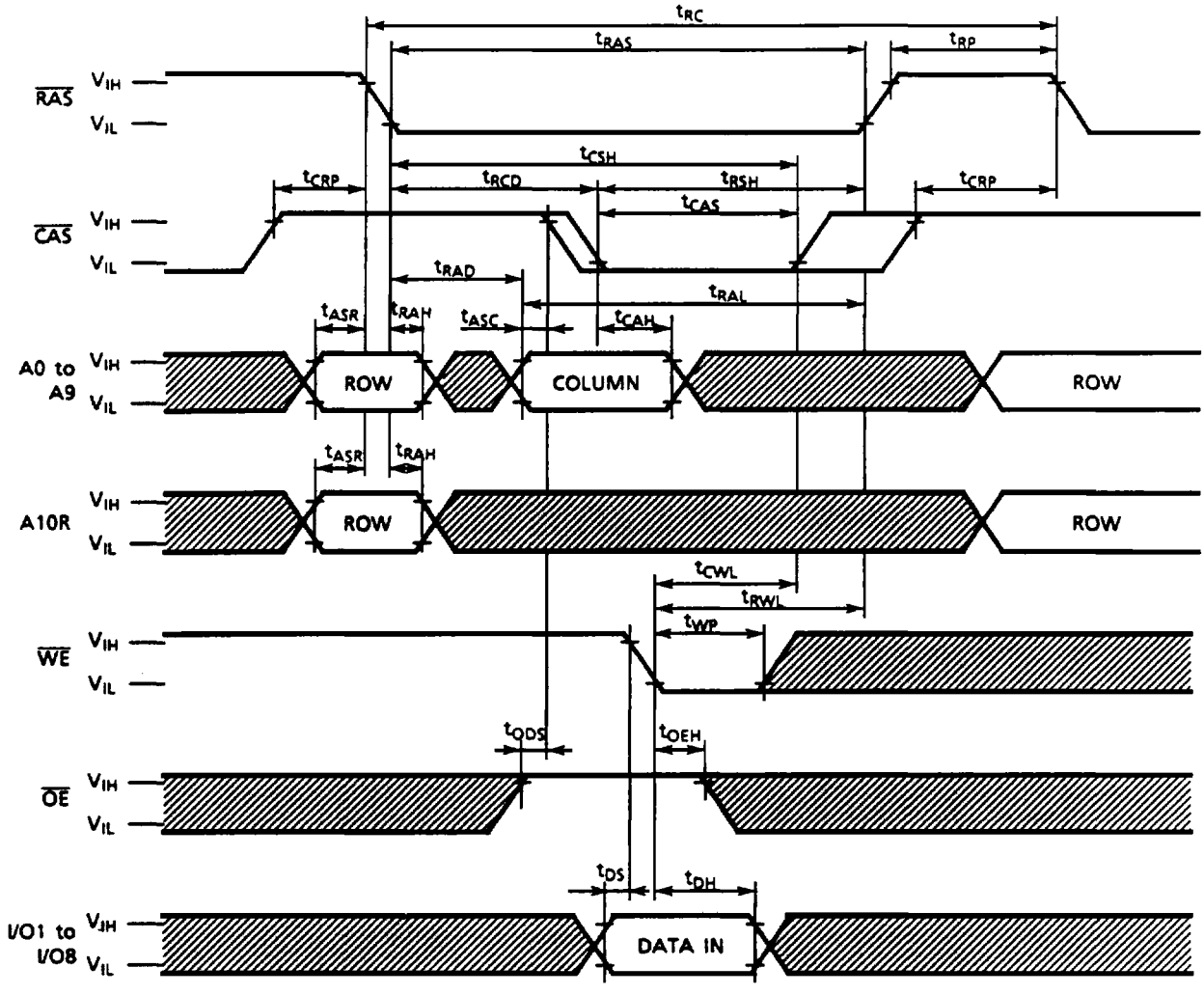
WRITE CYCLE (EARLY WRITE)



Note: D_{OUT} = Hi-Z

▨ : "H" or "L"

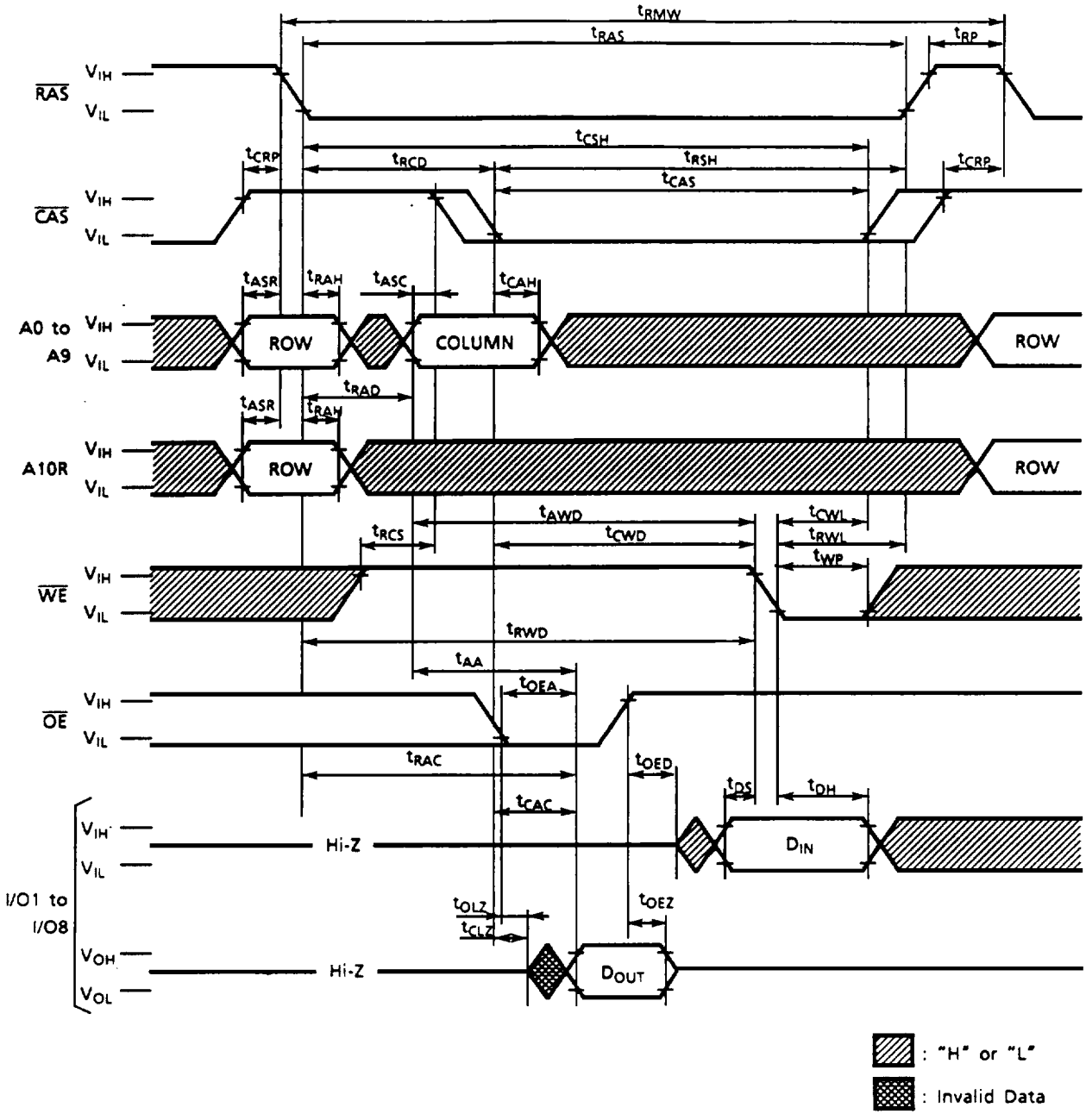
$\overline{OE}$ CONTROLLED WRITE CYCLE



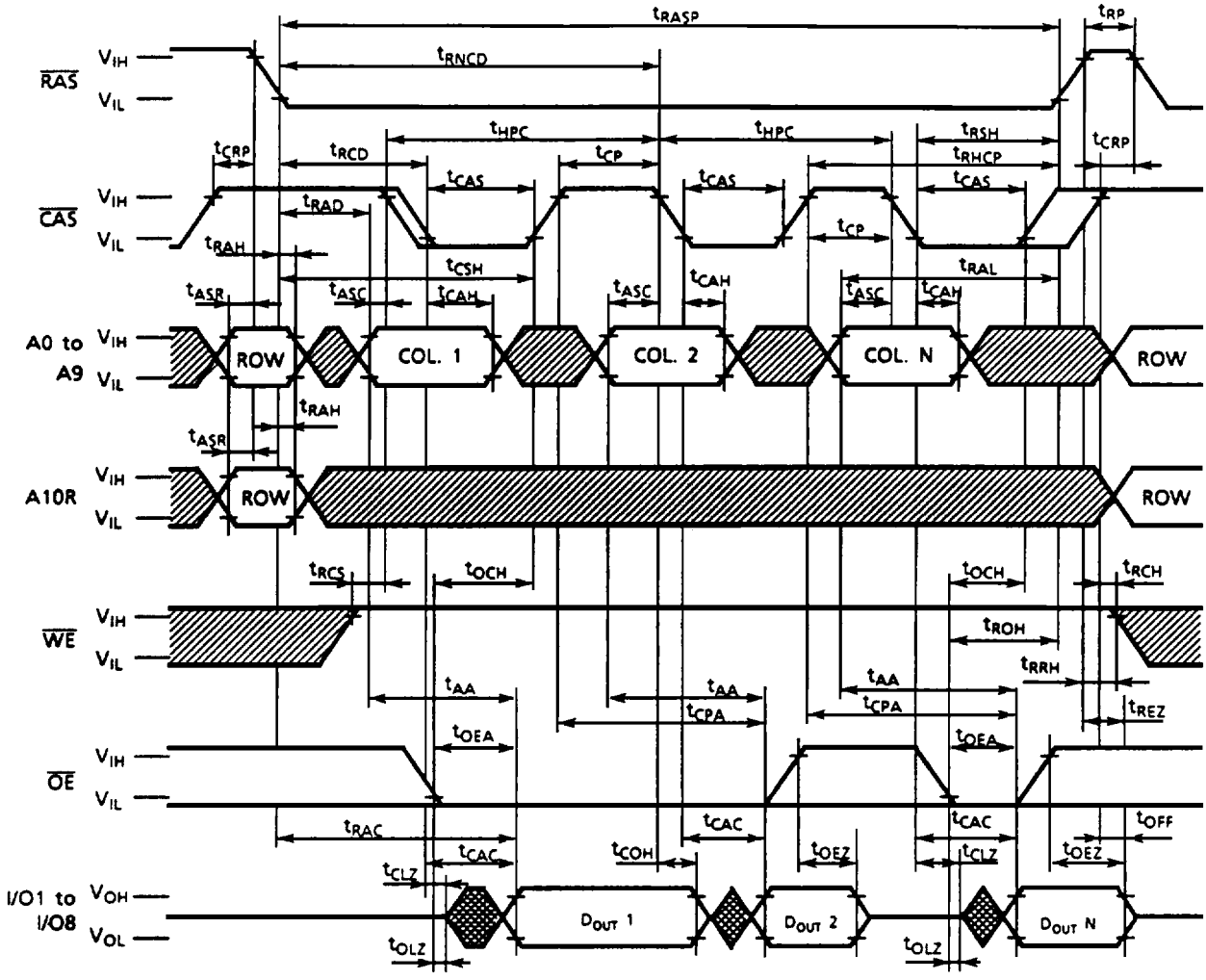
Note: D_{OUT} = Hi-Z

▨ : "H" or "L"

READ-MODIFY-WRITE CYCLE



HYPER PAGE MODE READ CYCLE

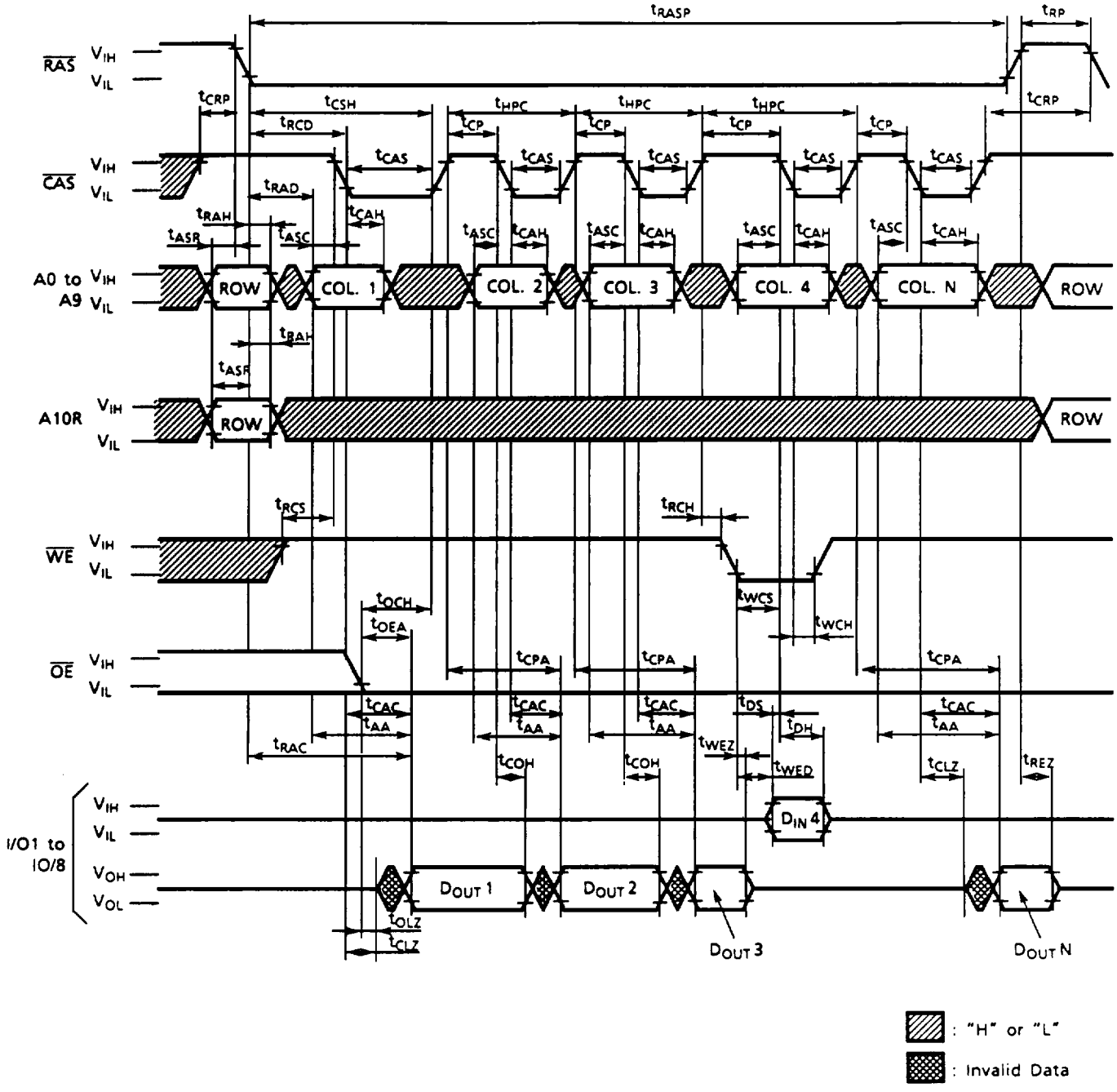


Note: D_{IN} = Hi-Z

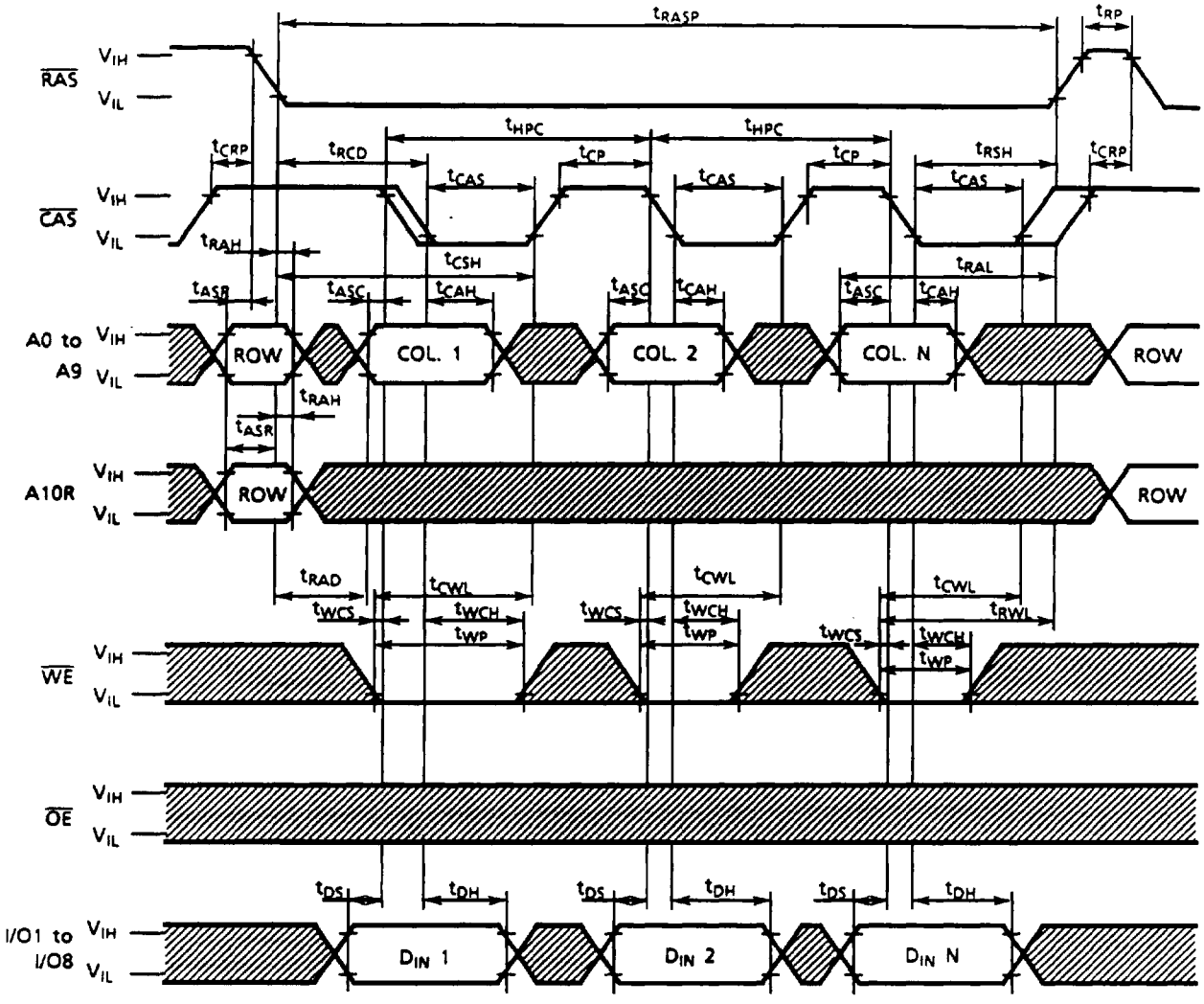
: "H" or "L"

: Invalid Data

HYPER PAGE MODE READ-WRITE MIXED CYCLE



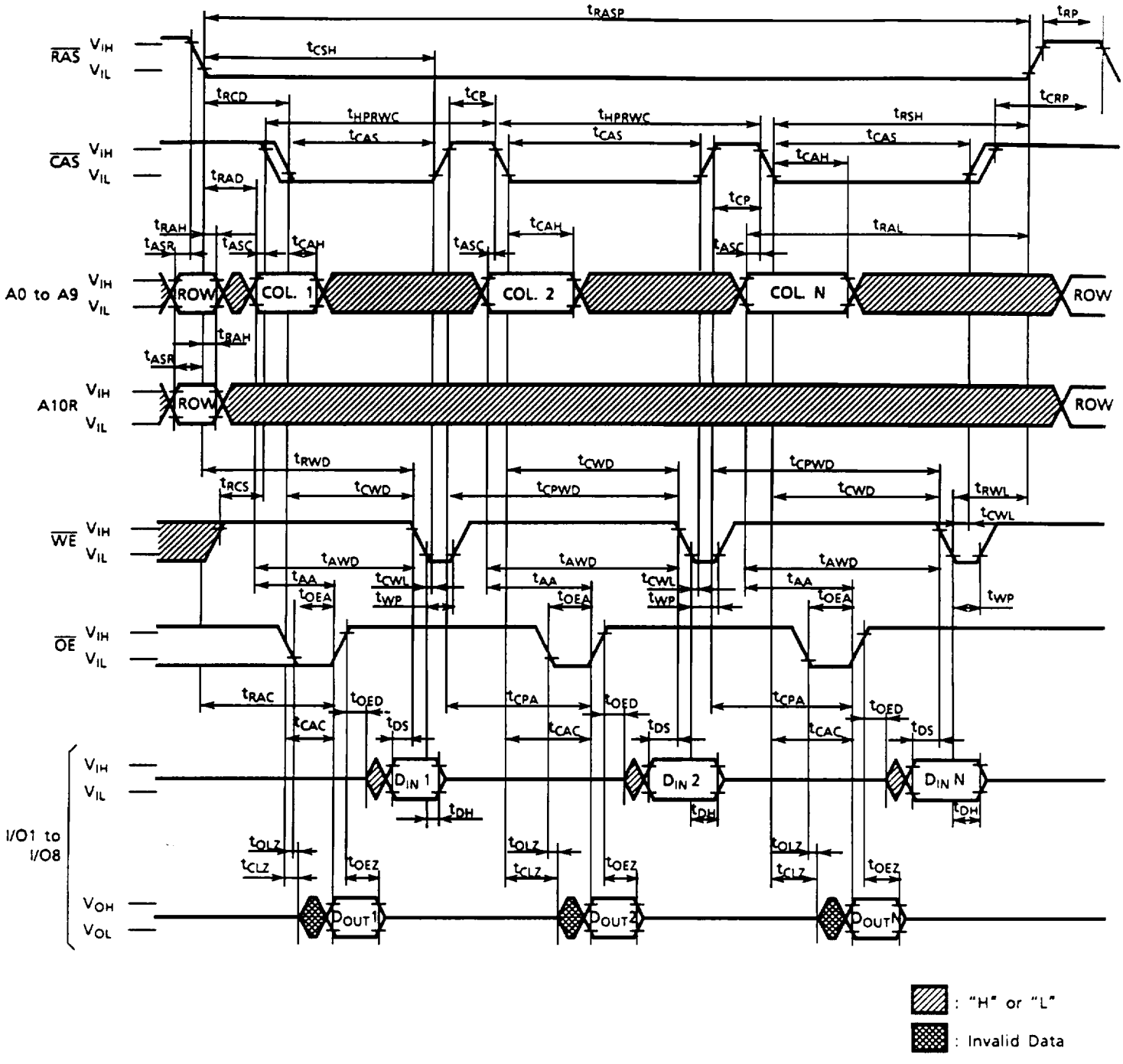
HYPER PAGE MODE WRITE CYCLE (EARLY WRITE)



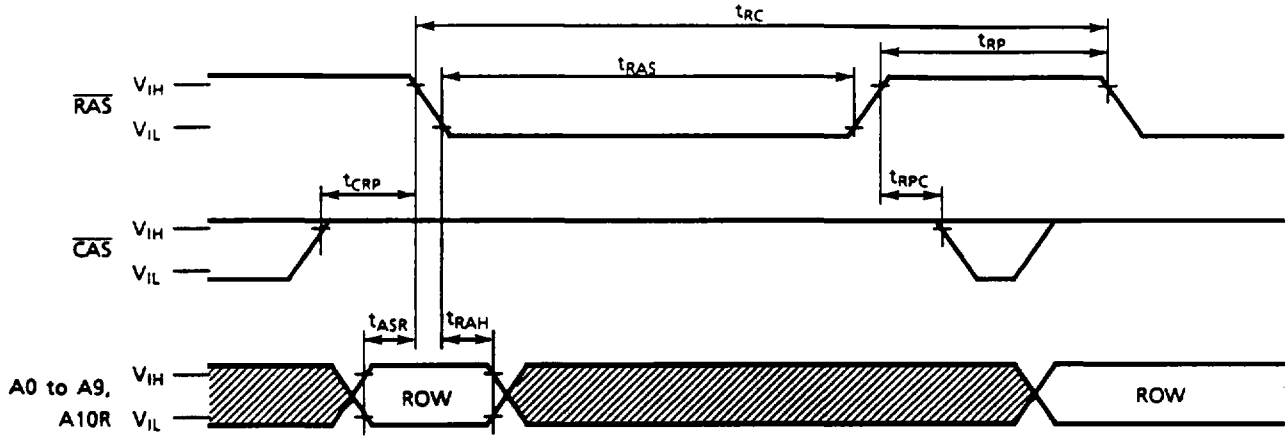
Note: D_{OUT} = Hi-Z

▨ : "H" or "L"

HYPER PAGE MODE READ-MODIFY-WRITE CYCLE



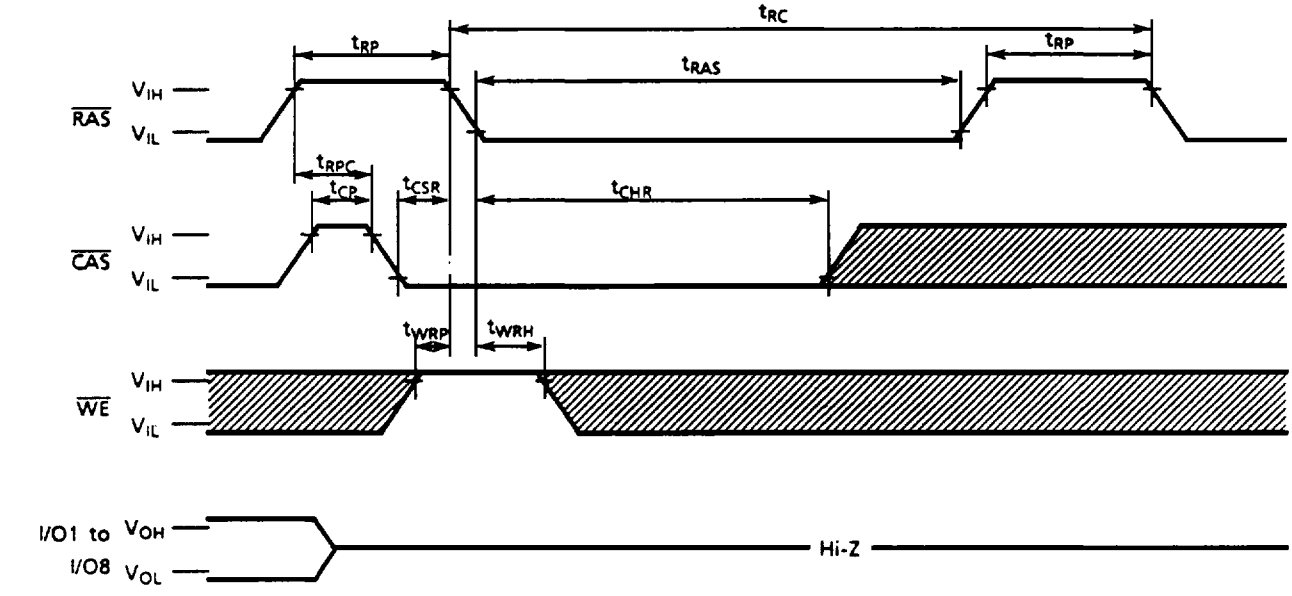
$\overline{RAS}$-ONLY REFRESH CYCLE



Note: $\overline{WE}$, $\overline{OE}$, D_{IN} = "H" or "L"
D_{OUT} = Hi-Z

▨ : "H" or "L"

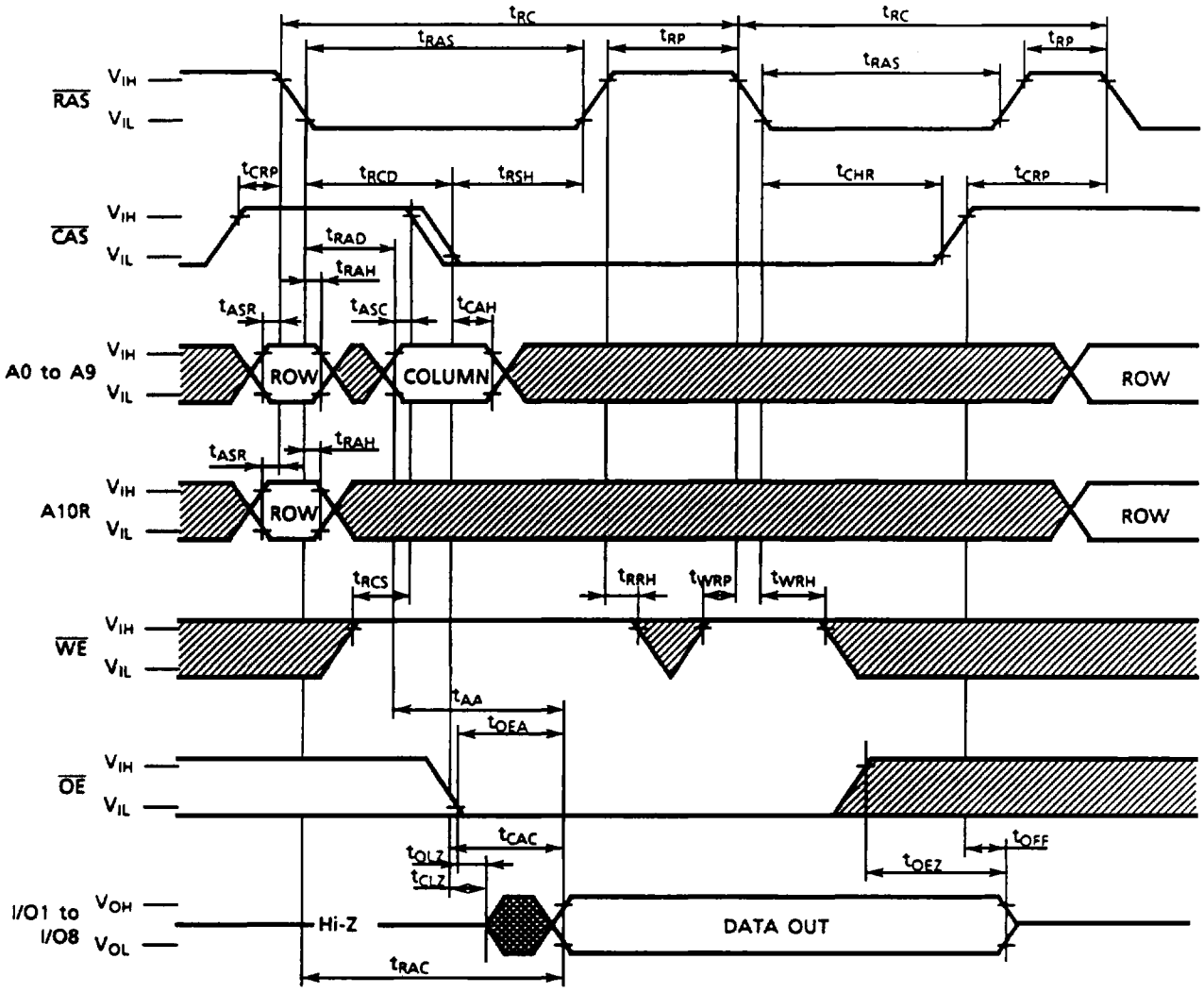
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



Note: D_{IN}, $\overline{OE}$, A0 to A9, A10R = "H" or "L"

▨ : "H" or "L"

HIDDEN REFRESH CYCLE (READ)

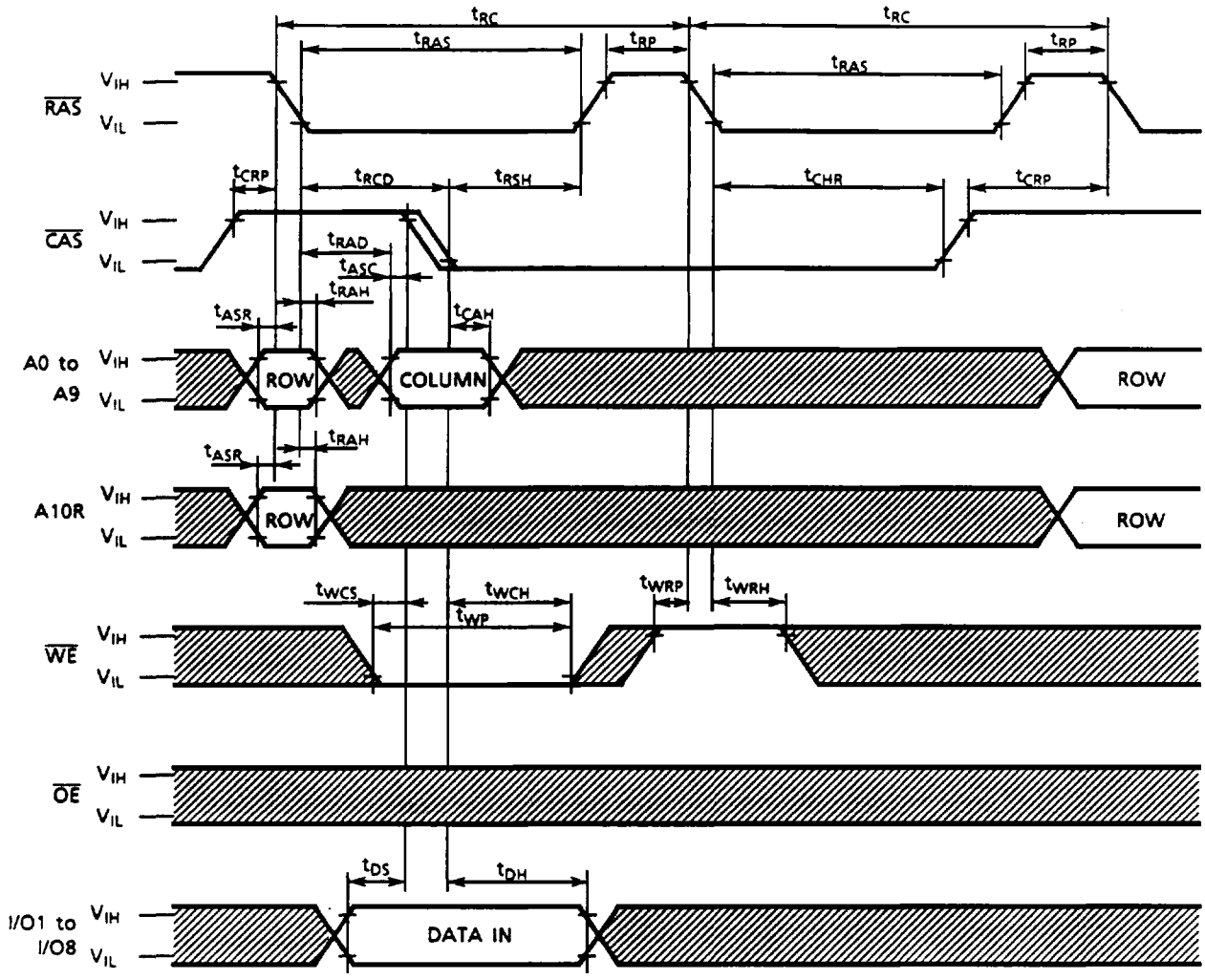


Note: D_{IN} = Hi-Z

: "H" or "L"

: Invalid Data

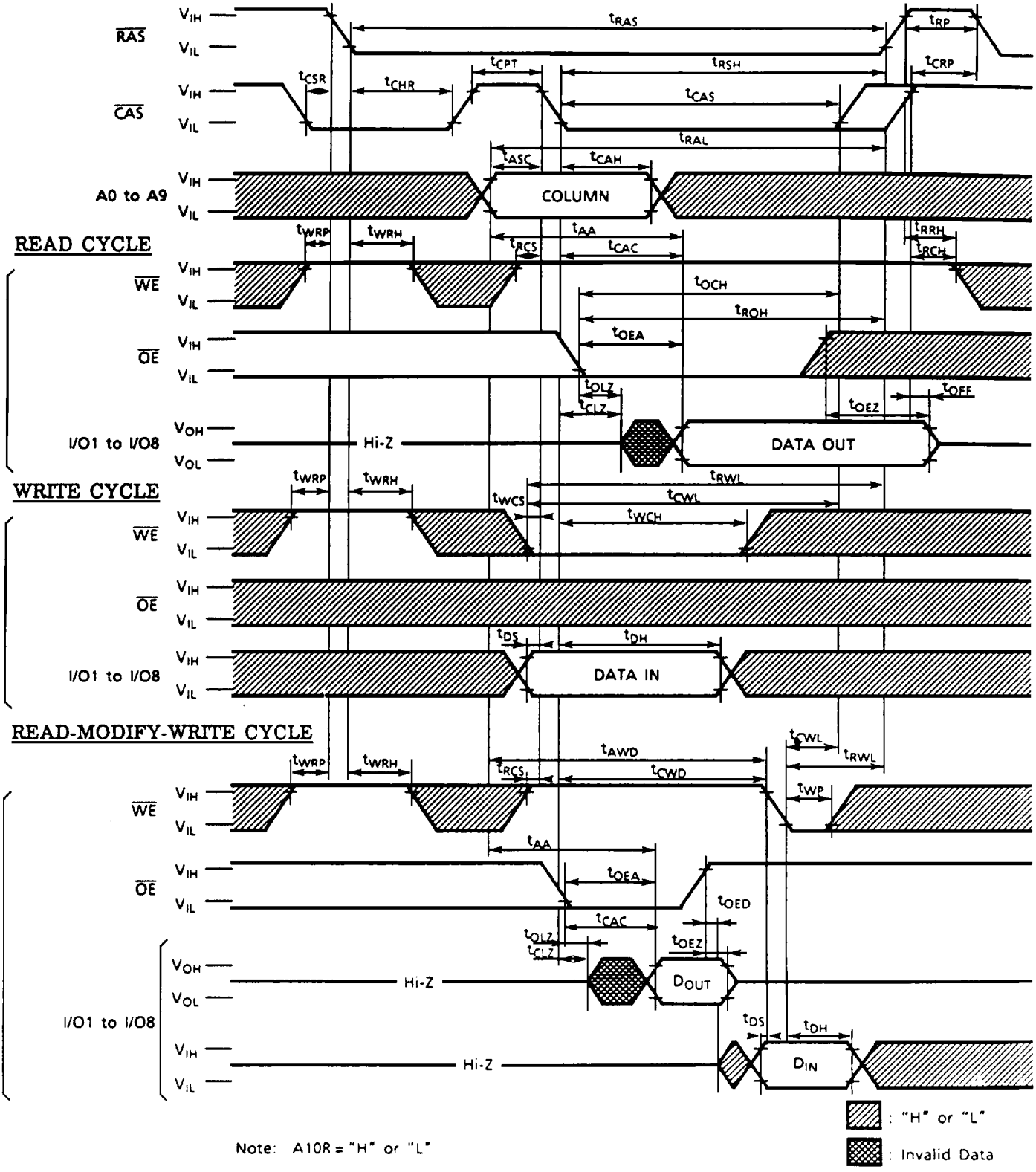
HIDDEN REFRESH CYCLE (WRITE)



Note: D_{OUT} = Hi-Z

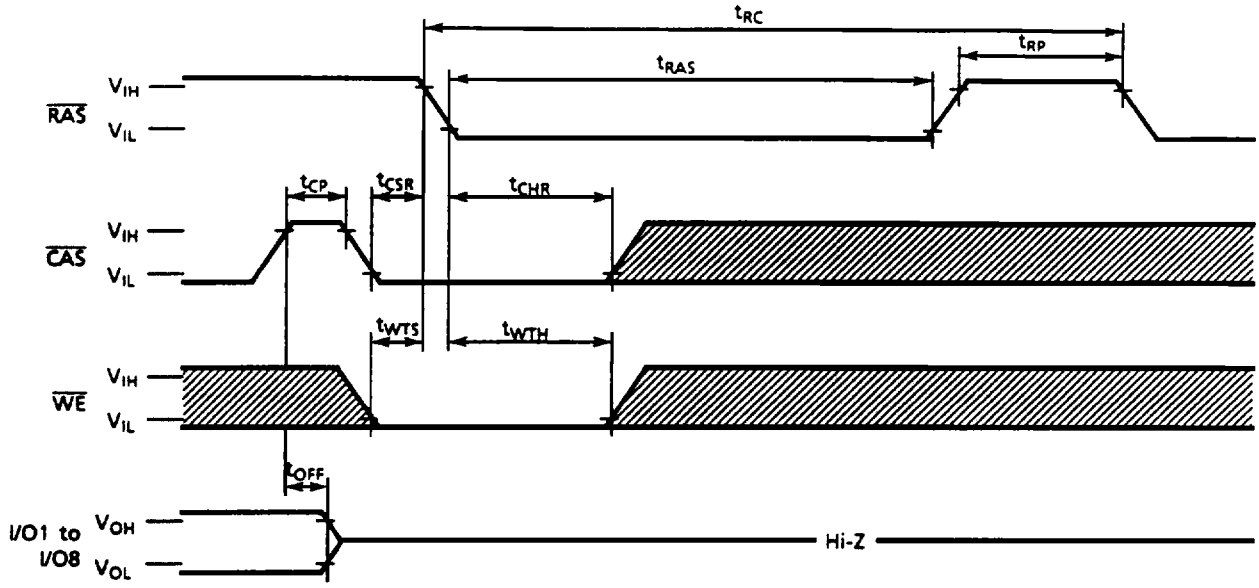
▨ : "H" or "L"

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



Note: A10R = "H" or "L"

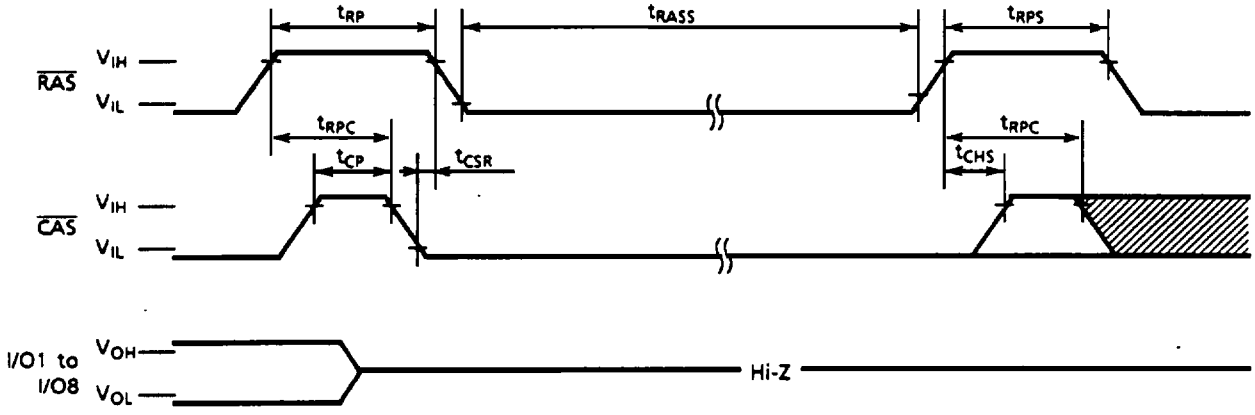
$\overline{WE}$, $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE (Test Mode)



Note: D_{IN}, $\overline{OE}$, A0 to A9, A10R = "H" or "L"

▨ : "H" or "L"

$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE



Note: $\overline{WE}$, $\overline{OE}$, A0 to A9, A10R = "H" or "L"
D_{IN} = "H" or "L"

▨ : "H" or "L"

TEST MODE

The TC5117805CJS/CFTS/CSJS/CSTS 2,097,152-word by 8-bit dynamic RAM is organized internally as 1,048,576 words by 16 bits. In test mode, data are written into 16 sectors in parallel through I/O1 only. (Address line A9 is not used.) If, when read, parallel bits are equal (either both ones or both zeroes) then a "1" is placed on the I/O8 pin. If any of the parallel bits differ, a "0" is placed on the I/O8 pin. The I/O1 through I/O7 pins always output a "1" during the test mode read cycle. This internal organization of the TC5117800CJS/CFTS/CSJS/CSTS is test mode, shown in the block diagram in Figure 1, allows the 2M x 8 bit DRAM to be tested as if it were a 1M x 16 bit DRAM.

A "$\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$" refresh cycle puts the device into test mode. A "$\overline{CAS}$ before $\overline{RAS}$" or "$\overline{RAS}$-only" refresh cycle puts it back into Normal mode. Refresh is performed in test mode using a "$\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$" refresh cycle, which uses the internal refresh address counter. Using test mode reduces test time (in the case of an N-test pattern) to one-half of that normally required.

TEST MODE BLOCK DIAGRAM

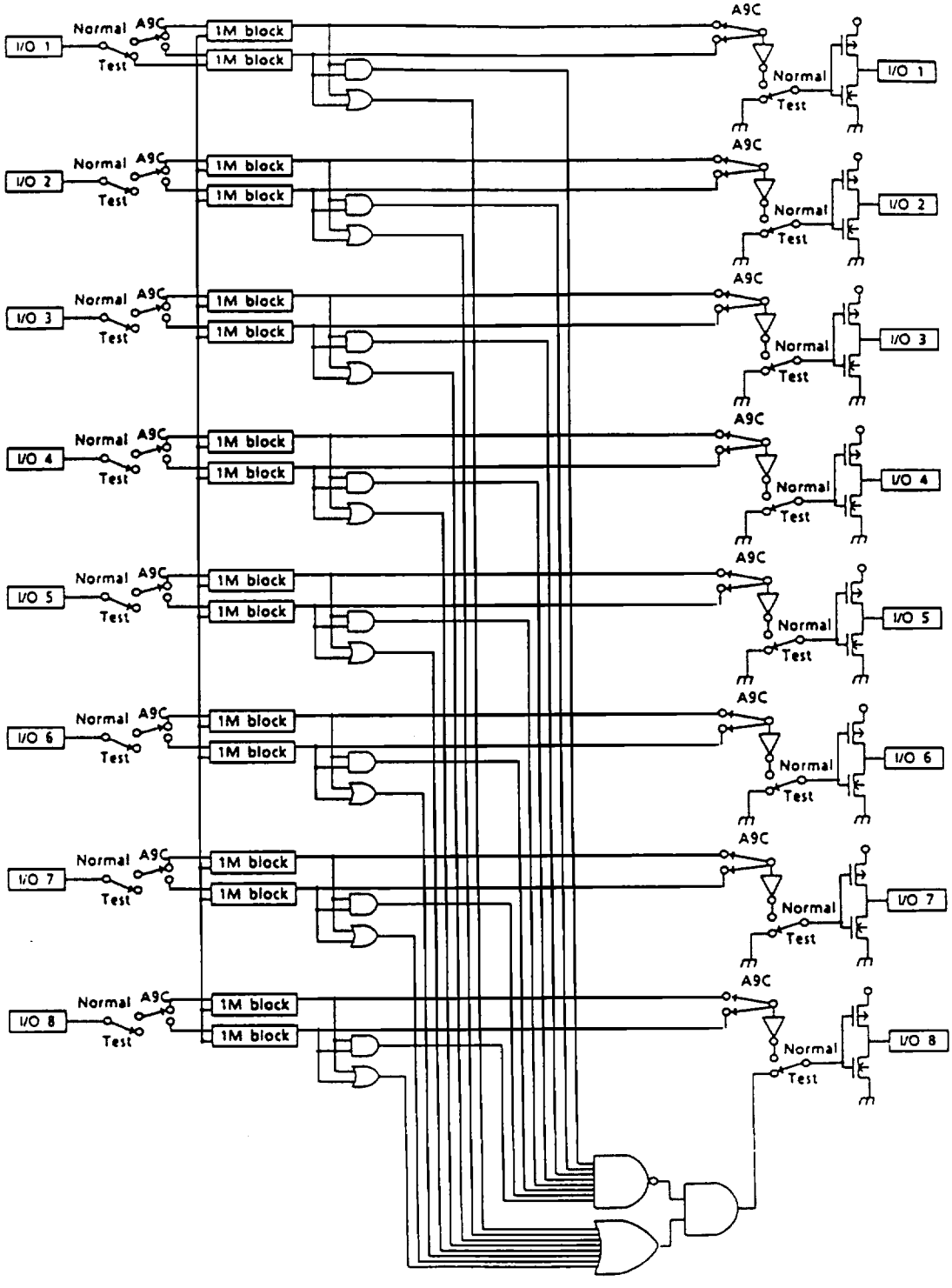
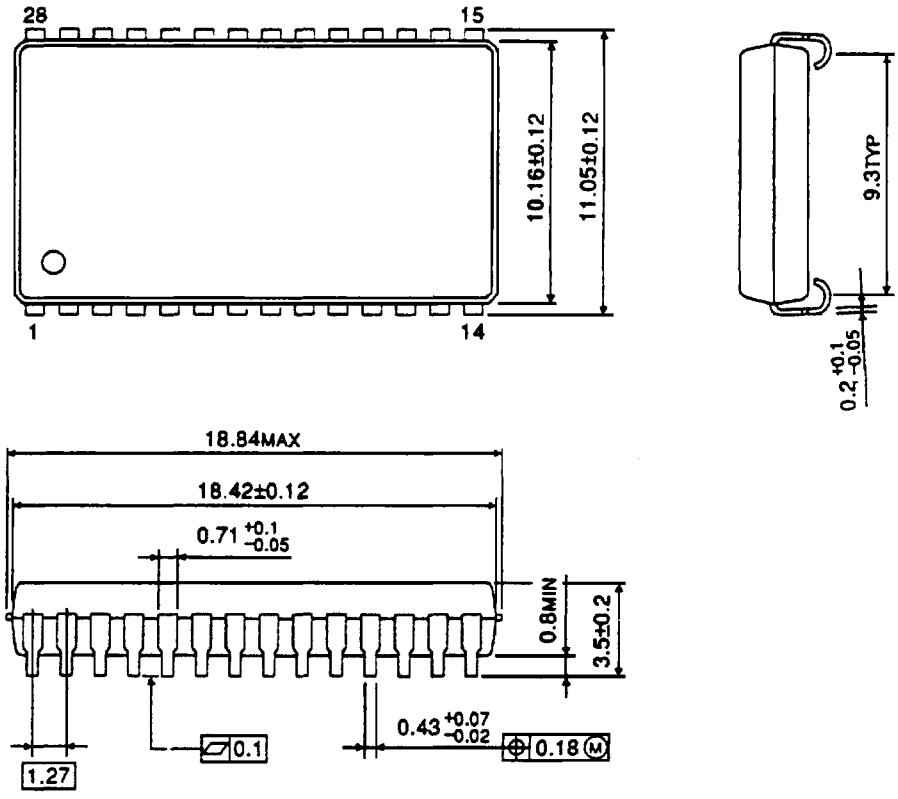


Fig. 1

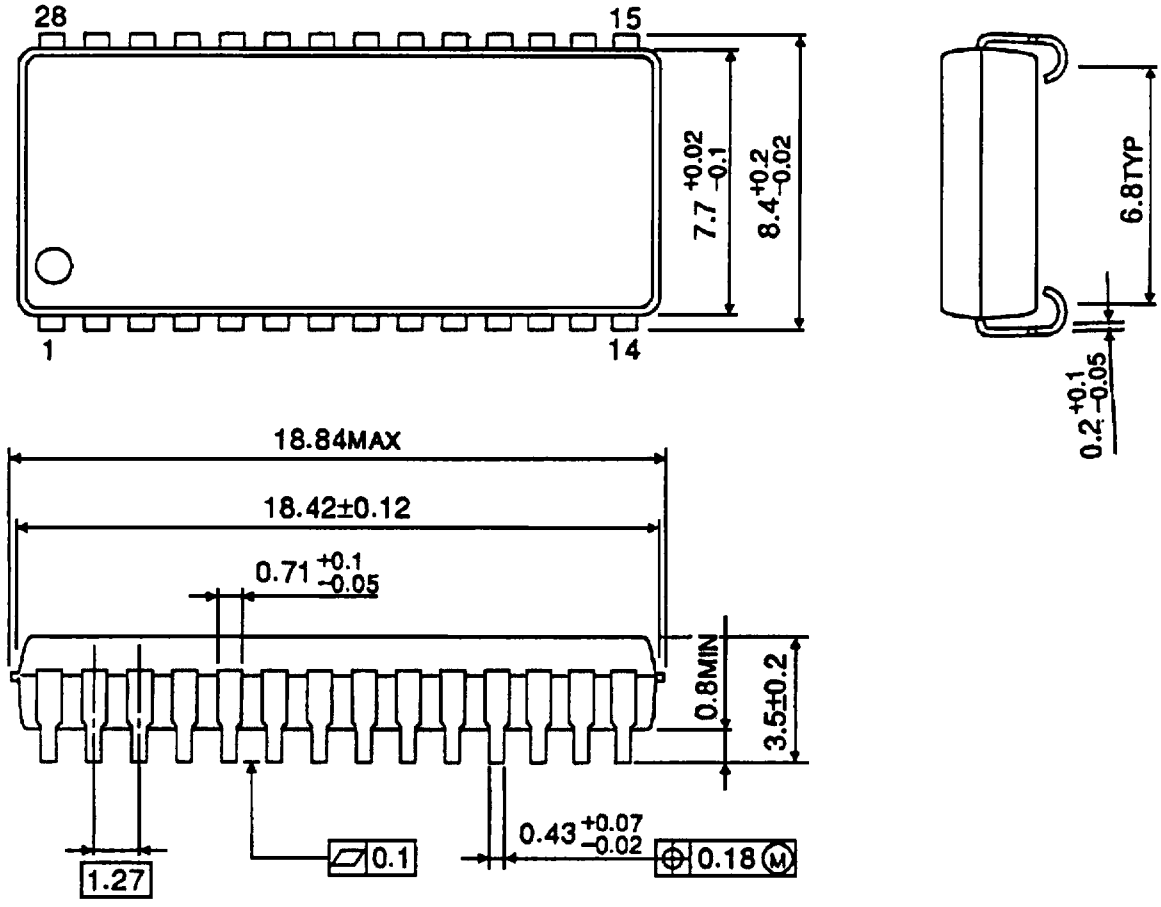
PACKAGE DIMENSIONS (SOJ28 – P – 400 – 1.27C)

Unit: mm



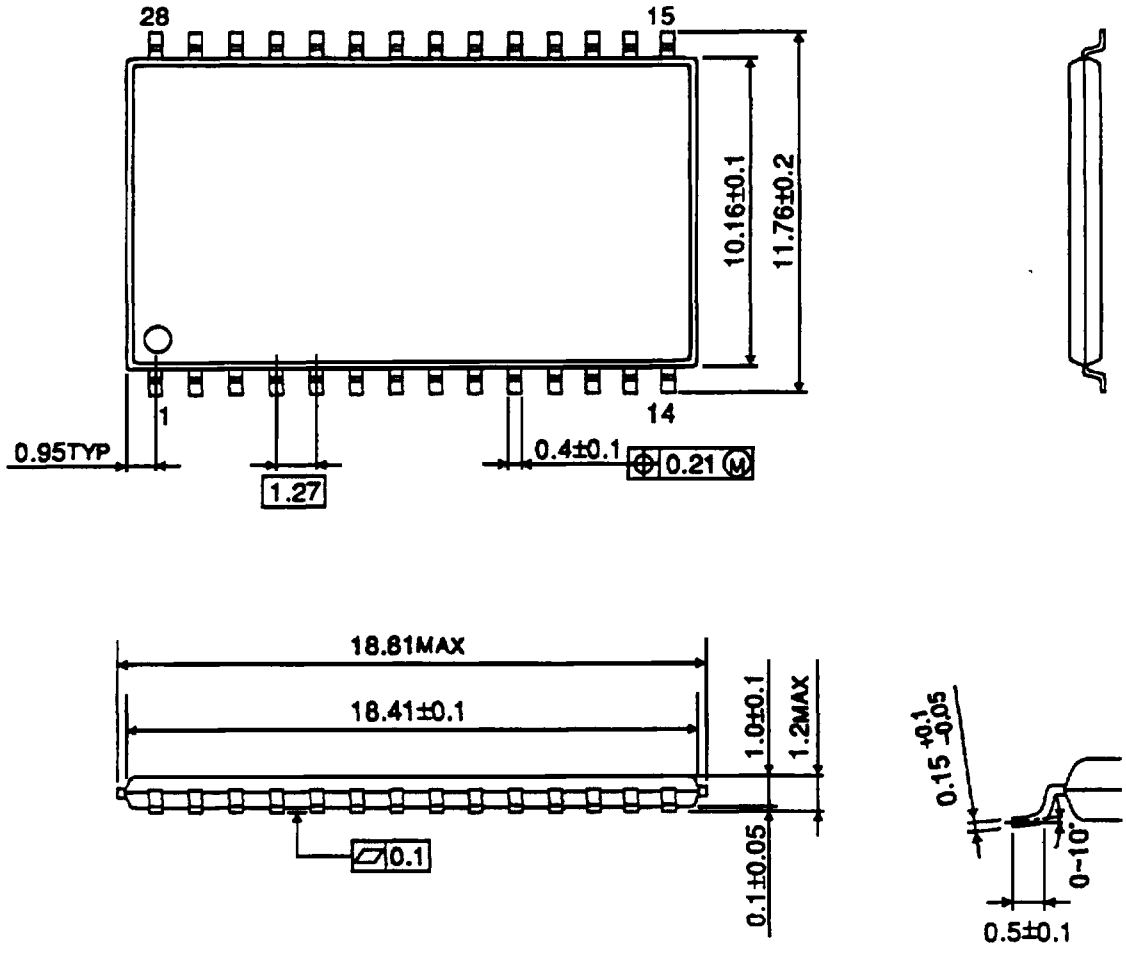
PACKAGE DIMENSIONS (SOJ28 – P – 300 – 1.27B)

Unit: mm



PACKAGE DIMENSIONS (TSOPII 28 – P – 400 – 1.27)

Unit: mm



PACKAGE DIMENSIONS (TSOPII 28 – P – 300 – 1.27E)

Unit: mm