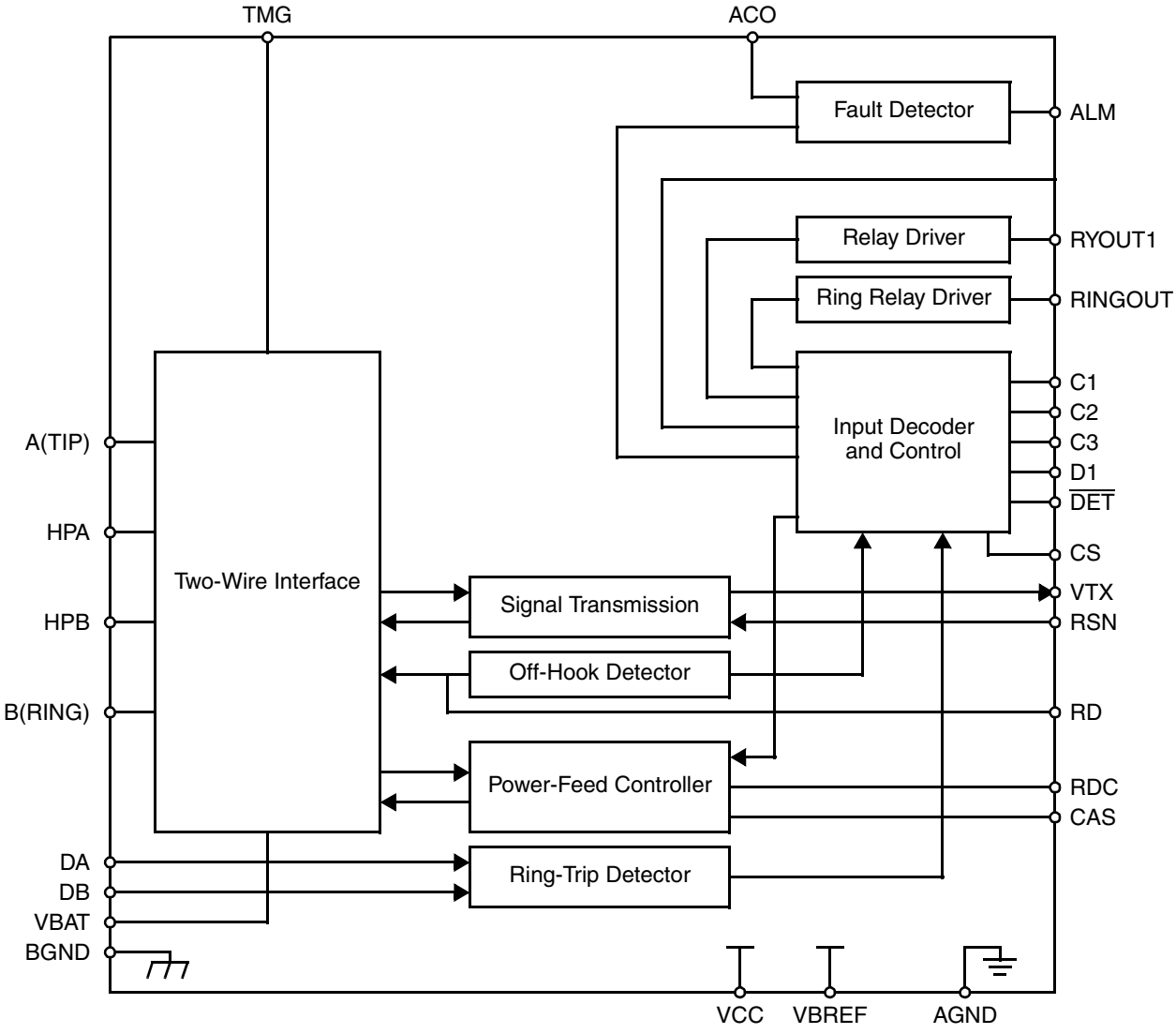
Le7925

Subscriber Line Interface Circuit

DISTINCTIVE CHARACTERISTICS

- **Control states: Active, Disconnect, and Ringing**
- **–20 V to –58 V battery operation**
- **On-hook transmission**
- **Two-wire impedance set by single external impedance**
- **No –5 V supply required**
- **Fault detectors**
- **Polarity reversal (active and on-hook)**
- **Programmable constant-current feed**
- **Programmable loop-detect threshold**
- **Programmable ring-trip detect threshold**
- **Current gain = 500**
- **On-chip Thermal Management (TMG) feature**
- **Two on-chip relay drivers and relay snubbers, one ringing and one general purpose**

BLOCK DIAGRAM

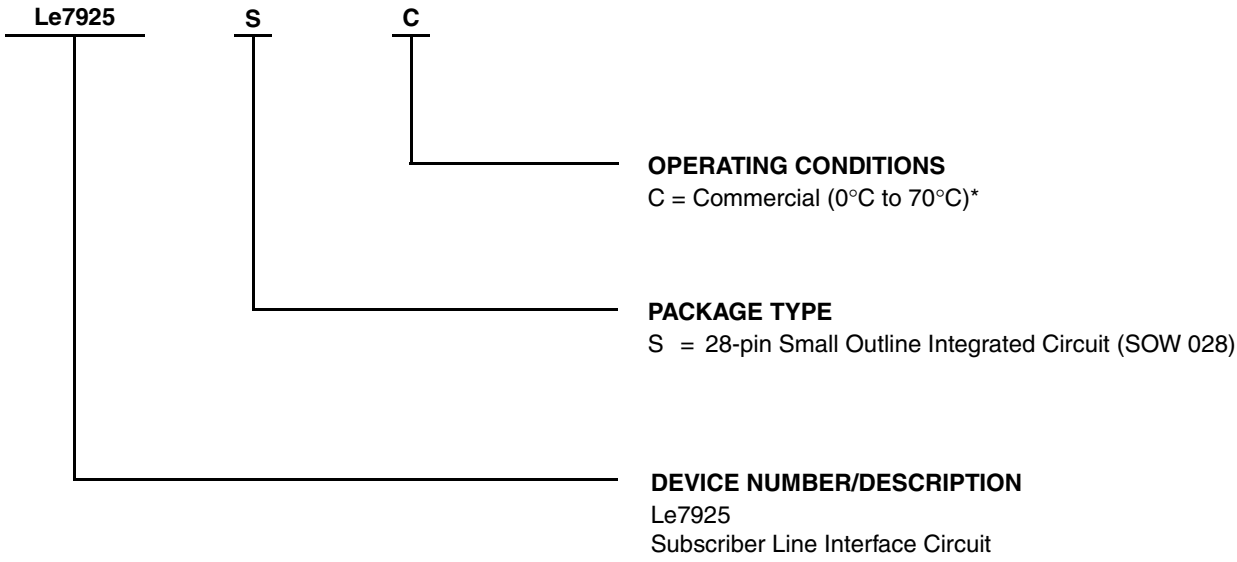


Document ID#	**080425**	Date:	**Jun 23, 2003**
Rev:	**B**	Version:	**1**
Distribution:	**Public Document**		

ORDERING INFORMATION

Standard Products

Legerity standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations	
Le7925**	SC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Legerity sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on Legerity's standard military

Note:

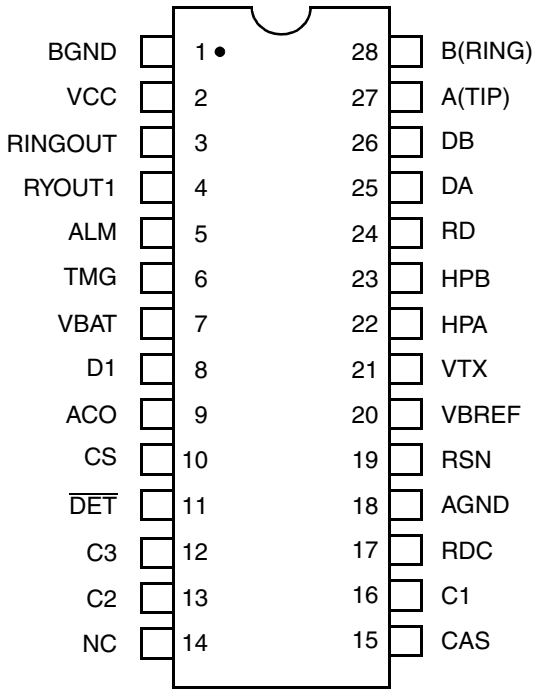
** Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from –40°C to +85°C is guaranteed by characterization and periodic sampling of production units.*

*** Legerity reserves the right to fulfill all orders for this device with parts marked with the "Am" part number prefix, until such time as all inventory bearing this mark has been depleted. It should be noted that parts marked with either the "Am" or the "Le" part number prefix are equivalent devices in terms of form, fit, and function. The only difference between the two is in the part number prefix appearing on the topside mark.*

CONNECTION DIAGRAMS

Top View

28-Pin SOIC



Notes:

1. *Pin 1 is marked for orientation.*
2. *NC = No connect*

PIN DESCRIPTIONS

Pin Names	Type	Description
ACO	Input	Overvoltage Alarm. Input from external resistor allows detection of positive overvoltages on the line. Detection forces ALM and $\overline{\text{DET}}$ Low.
AGND	Gnd	Analog ground
ALM	Output	Alarm. A logic Low indicates that a fault detector has been activated. Faults detected include thermal overload, ACO, and B to ground faults.
A(TIP)	Output	Output of A(TIP) power amplifier
BGND	Gnd	Battery (power) ground
B(RING)	Output	Output of B(RING) power amplifier
C1, C2, C3	Input	SLIC control pins. C3 is MSB and C1 is LSB. TTL compatible.
CAS	Capacitor	Anti-saturation pin for capacitor to filter reference voltage when operating in anti-saturation region.
CS	Input	Logic input to enable/disable the ALM and $\overline{\text{DET}}$ outputs. A logic Low enables the outputs. A logc High disables the outputs.
D1	Input	D1 controls the relay driver RYOUT1. A logic High on D1 activates the RYOUT1 relay driver. TTL compatible.
DA	Input	Ring-trip negative. Negative input to ring-trip comparator.
DB	Input	Ring-trip positive. Positive input to ring-trip comparator.
$\overline{\text{DET}}$	Output	Detector. Logic Low indicates that the selected detector is tripped. Logic inputs C2 and C3 select the detector. Open-collector with a built-in 15 kΩ pull-up resistor.
HPA	Capacitor	High-Pass Filter Capacitor. A(TIP) side of high-pass filter capacitor.
HPB	Capacitor	High-Pass Filter Capacitor. B(RING) side of high-pass filter capacitor.
NC	—	No connect. Pin not internally connected.
RD	Resistor	Detector resistor. Detector threshold set and filter pin.
RDC	Resistor	DC feed resistor. Connection point for the DC feed current programming network. The other end of the network connects to the receiver summing node (RSN).
RINGOUT	Output	Ring Signal Driver. Open-collector driver with emitter internally connected to BGND.
RSN	Input	The metallic current (AC and DC) between A(TIP) and B(RING) is equal to 500 x the current into this pin. The networks that program receive gain, two-wire impedance, and feed current all connect to this node.
RYOUT1	Output	Relay Driver. Open-collector driver with emitter internally connected to BGND.
TMG	—	Thermal Management. External resistor connects between this pin and VBAT to offload power from SLIC.
VBAT	Battery	Battery supply and connection to substrate
VBREF	—	This is an Legerity-reserved pin and must always be connected to the VBAT pin.
VCC	Power	+5 V power supply
VTX	Output	Transmit Audio. This output is a unity gain version of the A(TIP) and B(RING) metallic voltage. VTX also sources the two-wire input impedance programming network.

ABSOLUTE MAXIMUM RATINGS

Storage temperature . . . . . –55°C to +150°C

V_{CC} with respect to AGND/DGND . . .–0.4 V to +7.0 V

V_{BAT} with respect to AGND/DGND:
- Continuous . . . . . +0.4 V to –70 V
- 10 ms. . . . . +0.4 V to –75 V

BGND with respect to AGND/DGND . . . .+3 V to –3 V

A(TIP) or B(RING) to BGND:
- Continuous . . . . . V_{BAT} to +1 V
- 10 ms (f = 0.1 Hz) . . . . . –70 V to +5 V
- 1 µs (f = 0.1 Hz). . . . . –80 V to +8 V
- 250 ns (f = 0.1 Hz). . . . . –90 V to +12 V

Current from A(TIP) or B(RING). . . . . ±150 mA

RINGOUT and RYOUT1 outputs:
- RINGOUT current . . . . . 75 mA
- RYOUT1 current . . . . . 120 mA
- Voltage. . . . . BGND to +7 V
- Transient . . . . . BGND to +10 V

DA and DB inputs:
- Voltage on ring-trip inputs . . . . . V_{BAT} to 0 V
- Current into ring-trip inputs . . . . . ±10 mA

C3–C1, D1, and CS:
- Input voltage . . . . . –0.4 V to (V_{CC} + 0.4 V)

Maximum power dissipation, continuous,*
T_A = 70°C, No heat sink (See note):
- In 28-pin SOIC package . . . . . 1.35 W

Thermal Data: . . . . . θ_{JA}
- In 28-pin SOIC package . . . . . .60°C/W typ

ESD immunity/pin (HBM) . . . . . 1500 V

***Note:** Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 165°C. The device should never be exposed to this temperature. Operation above 145°C junction temperature may degrade device reliability. See the SLIC Packaging Considerations for more information.*

Stresses above those listed under Absolute Maximum Ratings can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient temperature . . . . . 0°C to +70°C*

V_{CC} . . . . . 4.75 V to 5.25 V

V_{BAT} . . . . . –20 V to –58 V

AGND/DGND . . . . . 0 V

BGND with respect to
- AGND/DGND . . . . . –100 mV to +100 mV

Load resistance on VTX to ground . . . . . 20 kΩ min

Operating Ranges define those limits between which device functionality is guaranteed.

** Legerity guarantees the performance of this device over commercial (0 to 70° C) and industrial (-40 to 85 ° C) temperature ranges by conducting electrical characterization over each range and by conducting a production test with single insertion coupled to periodic sampling. These characterization and test procedures comply with section 4.6.2 of Bellcore TR-TSY-000357 Component Reliability Assurance Requirements for Telecommunications Equipment.*

ELECTRICAL CHARACTERISTICS

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Transmission Performance						
2-wire return loss	200 Hz to 3.4 kHz	26			dB	1, 4
Analog output (V_{TX}) impedance			3	20	Ω	4
Analog (V_{TX}) output offset voltage		–50		+50	mV	
Overload level, 2-wire and 4-wire	Active state	2.5			Vpk	2a
Overload level	On hook, R_{LAC} = 600 Ω	0.77			Vrms	2b
THD, Total Harmonic Distortion	0 dBm +4.7 dBm		–64 –55	–50 –40	dB	5
THD, on hook	0 dBm, R_{LAC} = 600 Ω			–36		
Longitudinal Capability (See Test Circuit D)						
Longitudinal to metallic, L-T, L-4 balance	200 Hz to 1 kHz 1 kHz to 3.4 kHz	53 53			dB	
Longitudinal signal generation 4-L	200 Hz to 3.4 kHz	40				
Longitudinal current per pin (A or B)	Active state On hook	8.5 8.5	18 18		mArms	8
Longitudinal impedance (A or B)	0 to 100 Hz		25	35	Ω/pin	
Idle Channel Noise						
C-message weighted noise	R_L = 600 Ω		+7	+12	dBrnC	4
Psophometric weighted noise	R_L = 600 Ω R_{LAC} = 600, OHT mode		–83	–78 –70	dBmp	
Insertion Loss and Balance Return Signal (See Test Circuits A and B)						
Gain accuracy 4- to 2-wire	0 dBm, 1 kHz 0°C to 70°C –40°C to 85°C	–0.15 –0.20	0 0	+0.15 +0.20	dB	— 4
Gain accuracy 2- to 4-wire, 4- to 4-wire	0 dBm, 1 kHz 0°C to 70°C –40°C to 85°C	–6.22 –6.22	–6.02 –6.02	–5.82 –5.82		— 4
Gain accuracy, 4- to 2-wire	On hook	–0.35	0	+0.35		4
Gain accuracy, 2- to 4-wire, 4- to 4-wire	On hook	–6.37	–6.02	–5.67		4
Gain accuracy over frequency	300 Hz to 3400 Hz relative to 1 kHz	–0.15		+0.15		5
Gain tracking	+3 dBm to –55 dBm relative to 0 dBm	–0.15		+0.15		
Gain tracking On hook	0 dBm to –37 dBm +3 dBm to 0 dBm	–0.15 –0.35		+0.15 +0.35		
Group delay	0 dBm, 1 kHz		4		µs	4, 7

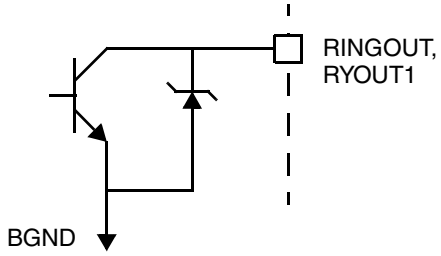
ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Line Characteristics						
I_L, Short loops, Active or Standby	R_{LDC} = 600 Ω	40.5	45	49.5	mA	
I_L, Long loops, Active	BAT = –47.2 V, R_{LDC} = 2000 Ω	18	20			
I_LLIM	Active, A and B to ground		95	130		
V_{AB}, Open circuit voltage	V_{BAT} = –48 V, Active state	V_{BAT} + 3.0	V_{BAT} + 1.5		V	
	OHT = 0	V_{BAT} + 7.5	V_{BAT} + 6.0			
Power Supply Rejection Ratio (V_{RIPPLE} = 100 mVrms), Active Normal State						
V_{CC}	50 Hz to 3.4 kHz	30	40		dB	5
V_{BAT}	50 Hz to 3.4 kHz	28	50			
Effective internal resistance	CAS pin to V_{BAT}	85	170	255	kΩ	4
Power Dissipation						
On hook, Active state	R_{TMG} = 1 kΩ		120	180	mW	
Off hook, Active state	R_L = 300 Ω, R_{TMG} = 1 kΩ		1150	1350		
Supply Currents, Battery = –48 V						
I_{CC}, on-hook V_{CC} supply current	Active state, V_{BAT} = –48 V		4.5	8.5	mA	
I_{BAT}, on-hook V_{BAT} supply current	Active state, V_{BAT} = –48 V		2.0	3.4		
RFI Rejection						
RFI rejection	100 kHz to 30 MHz (see Figure E)			1.0	mVrms	4
Receive Summing Node (RSN)						
RSN DC voltage	I_{RSN} = 0 mA		0		V	4
RSN impedance	200 Hz to 3.4 kHz		10	20	Ω	
Logic Inputs (C3–C1, D1, CS)						
V_{IH}, Input High voltage	All except C3	2.0			V	
V_{IH}, Input High voltage	C3	2.5				
V_{IL}, Input Low voltage				0.8		
I_{IH}, Input High current		–75		40	µA	
I_{IL}, Input Low current		–400				
Logic Output ($\overline{DET}$, ALM)						
V_{OL}, Output Low voltage	I_{OUT} = 0.3 mA			0.40	V	
V_{OH}, Output High voltage	I_{OUT} = –0.1 mA	2.4				
$\overline{DET}$ pull-up resistor to V_{CC}		9.5	15		kΩ	
ALM pull-up resistor to V_{CC}		13	20			
Ring-Trip Detector Input (DA, DB)						
Bias current		–500	–50		nA	
Offset voltage	Source resistance = 2 MΩ	–50	0	+50	mV	6

ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Loop Detector						
R_{LTH}, Loop-detect threshold tolerance	R_D = 35.4 kΩ	3.08	3.65	3.92	kΩ	
I_{ACO}, ACO fault input detect		220	320	420	µA	
Relay Driver Output (RINGOUT and RYOUT1)						
On voltage	I_{OL} = 50 mA, RINGOUT		+0.5	+0.75	V	
On voltage	I_{OL} = 90 mA, RYOUT1		0.7	1.0		
Off leakage	V_{OH} = +5 V			100	µA	
Zener breakover	I_Z = 100 µA	6	7.2		V	
Zener On voltage	I_Z = 30 mA		8			

RELAY DRIVER SCHEMATIC

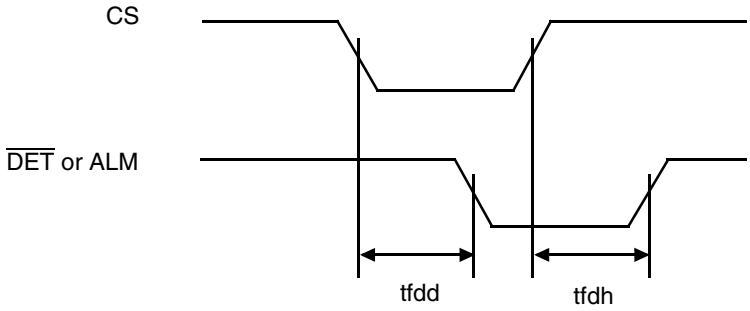


SWITCHING CHARACTERISTICS

Symbol	Parameter	Temperature Ranges	Min	Typ	Max	Unit	Note
t_{fdd}	CS Low to $\overline{DET}$ or ALM Active	0°C to 70°C –40°C to 85°C			1.1 1.6	µs	4
t_{fdh}	CS High to $\overline{DET}$ or ALM Disable	0°C to 70°C –40°C to 85°C			3.8 4.0		

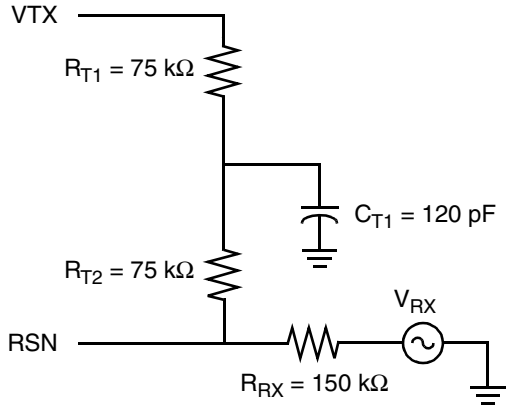
SWITCHING WAVEFORMS

CS to $\overline{DET}$ and ALM



Notes:

1. *Unless otherwise noted, test conditions are BAT = –48 V, V_{CC} = +5 V, R_L = 600 Ω, R_{DC1} = R_{DC2} = 6.95 kΩ, R_{TMG} = 1 kΩ, R_D = 35.4 kΩ, no fuse resistors, C_{HP} = 0.22 µF, C_{DC} = 430 nF, C_{CAS} = 0.33 µF, D_1 = 1N400x, two-wire AC input impedance is a 600 Ω resistance synthesized by the programming network shown below.*



2. *a. Overload level is defined when THD = 1%.*
   b. Overload level is defined when THD = 1.5%.
3. *Balance return signal is the signal generated at V_{TX} by V_{RX}. This specification assumes the two-wire AC load impedance matches the programmed impedance.*
4. *Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.*
5. *This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.*
6. *Tested with 0 Ω source impedance. 2 MΩ is specified for system design only.*
7. *Group delay can be greatly reduced by using a Z_T network such as that shown in Note 1 above. The network reduces the group delay to less than 2 µs and increases 2WRL. The effect of group delay on linecard performance also may be compensated for by synthesizing complex impedance with the QLSLAC™ device.*
8. *Minimum current level guaranteed not to cause a false loop detect.*

Table 1. SLIC Decoding

State	C3	C2	C1	Two-Wire Status	$\overline{\text{DET}}$	ALM
0	0	0	0	Disconnect	Disable	Disable
*1	0	0	1	(Disconnect)	(Disable)	(Disable)
2	0	1	0	On-hook TX (OHT) Polarity Reversal	Off-hook/Fault	Fault
3	0	1	1	Polarity Reversal	Off-hook/Fault	Fault
4	1	0	0	Ringing	Ring trip	Disable
*5	1	0	1	(Ringing)	(Ring trip)	(Disable)
6	1	1	0	OHT Forward	Off-hook/Fault	Fault
7	1	1	1	Active Forward	Off-hook/Fault	Fault

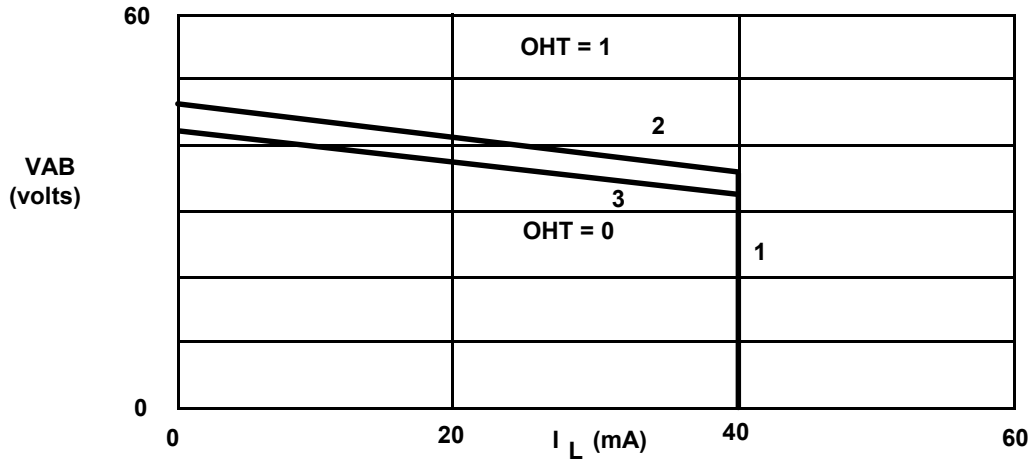
Note:
** Not valid states.*

		Note
D1	0	RYOUT1 Off
	1	RYOUT1 On
CS	0	$\overline{\text{DET}}$ and ALM enabled pin control table
	1	$\overline{\text{DET}}$ and ALM disabled

Table 2. User-Programmable Components

$Z_T = 250(Z_{2WIN} - 2R_F)$	Z_T is connected between the VTX and RSN pins. The fuse resistors are R_F, and Z_{2WIN} is the desired 2-wire AC input impedance. When computing Z_T, the internal current amplifier pole and any external stray capacitance between VTX and RSN must be taken into account.
$Z_{RX} = \frac{Z_L}{G_{42L}} \bullet \frac{500Z_T}{Z_T + 250(Z_L + 2R_F)}$	Z_{RX} is connected from V_{RX} to R_{SN}, Z_T is defined above, and G_{42L} is the desired receive gain.
$R_{DC1} + R_{DC2} = \frac{625}{I_{LOOP}}$ $C_{DC} = 1.5\ ms \bullet \frac{R_{DC1} + R_{DC2}}{R_{DC1}R_{DC2}}$	R_{DC1}, R_{DC2}, and C_{DC} form the network connected to the RDC pin. R_{DC1} and R_{DC2} are approximately equal. I_{LOOP} is the desired loop current in the constant-current region.
$R_{LTH} = \frac{R_D}{10}$	R_D is the resistor connected from R_D to ground, and R_{LTH} is the loop-resistance threshold between on-hook and off-hook detection.
$C_{CAS} = \frac{1}{3.4 \bullet 10^5 \pi f_c}$	C_{CAS} is the regulator filter capacitor and f_c is the desired filter cut-off frequency.
Thermal Management Equations (Normal Active and Tip Open States)	
$R_{TMG} \geq \frac{V_{BAT} - 7.8\ V}{I_{LOOP}}$	R_{TMG} is connected from T_{MG} to V_{BAT} and is used to limit power dissipation within the SLIC in Active and Disconnect states only.
$P_{RTMG} = \frac{(V_{BAT} - 7.8\ V - (I_L \bullet R_L))^2}{(R_{TMG} + 70\ \Omega)^2} \bullet R_{TMG}$	Power dissipated in the thermal management resistor, R_{TMG}, during Active and Disconnect states.
$P_{SLIC} = V_{BAT}(I_L) - P_{RTMG} - R_L(I_L)^2 + 0.12\ W$	Power dissipated in the SLIC while in Active and Disconnect states.

DC FEED CHARACTERISTICS



$R_{DC} = R_{DC1} + R_{DC2} = 6.95\ k\Omega$
BAT = –48 V

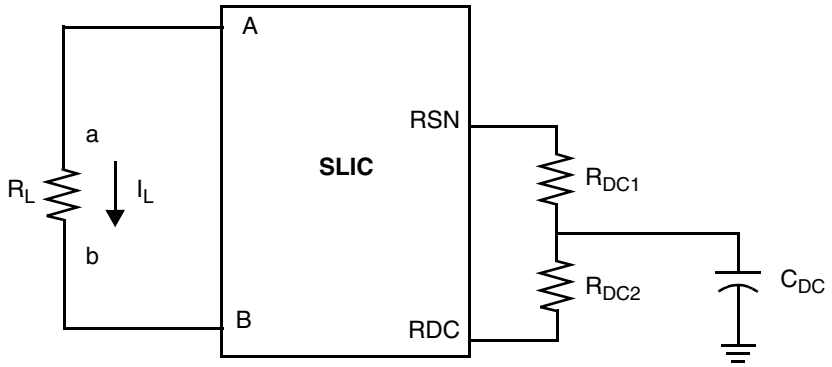
Notes:
Curve is for illustration only.

1. $V_{AB} = I_L R_L' = \frac{\text{[illegible]}}{R_{DC}}$ where $R_L' = R_L + 2R_F$

2. $V_{AB} = |V_{BAT}| - 1.5 - I_L\left(\frac{R_{DC}}{56.5}\right)$

3. $V_{AB} = |V_{BAT}| - 6.0 - I_L\left(\frac{R_{DC}}{56.5}\right)$

a. Load Line (Typical)

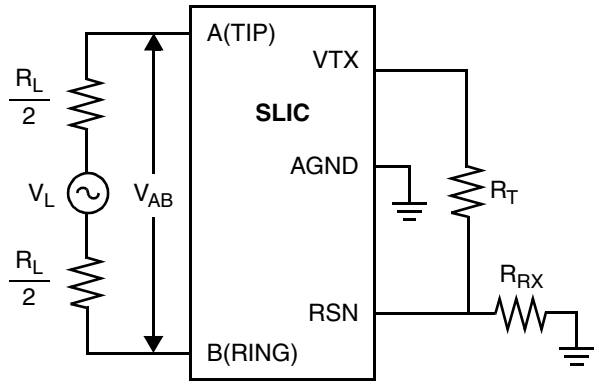


Feed current programmed by R_{DC1} and R_{DC2}

b. Feed Programming

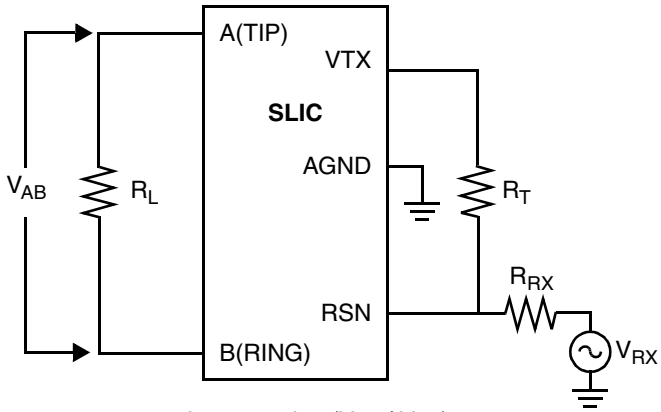
Figure 1. DC Feed Characteristics

TEST CIRCUITS



$I_{L2-4} = 20 \log (V_{TX} / V_{AB})$

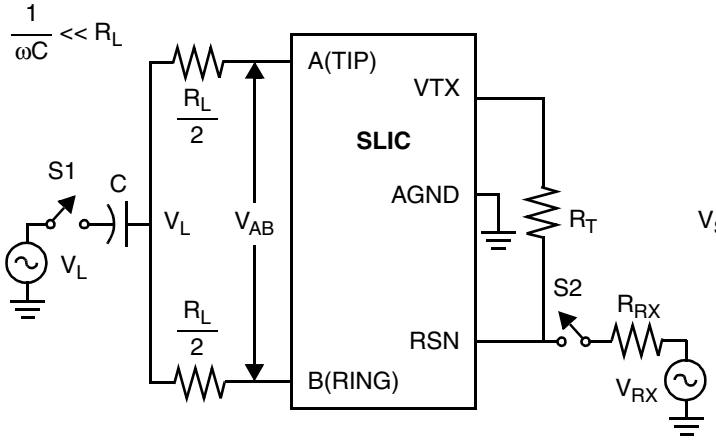
A. Two- to Four-Wire Insertion Loss



$I_{L4-2} = 20 \log (V_{AB} / V_{RX})$

$BRS = 20 \log (V_{TX} / V_{RX})$

B. Four- to Two-Wire Insertion Loss and Balance Return Signal



S2 Open, S1 Closed

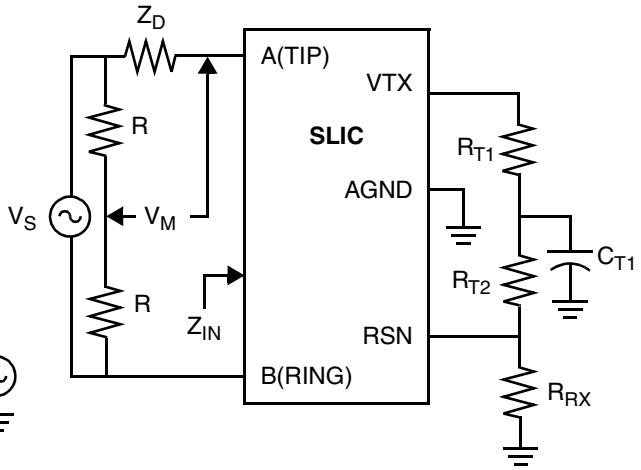
$L\text{-}T\ Long.\ Bal. = 20 \log (V_{AB} / V_L)$

$L\text{-}4\ Long.\ Bal. = 20 \log (V_{TX} / V_L)$

S2 Closed, S1 Open

$4\text{-}L\ Long.\ Sig.\ Gen. = 20 \log (V_L / V_{RX})$

C. Longitudinal Balance

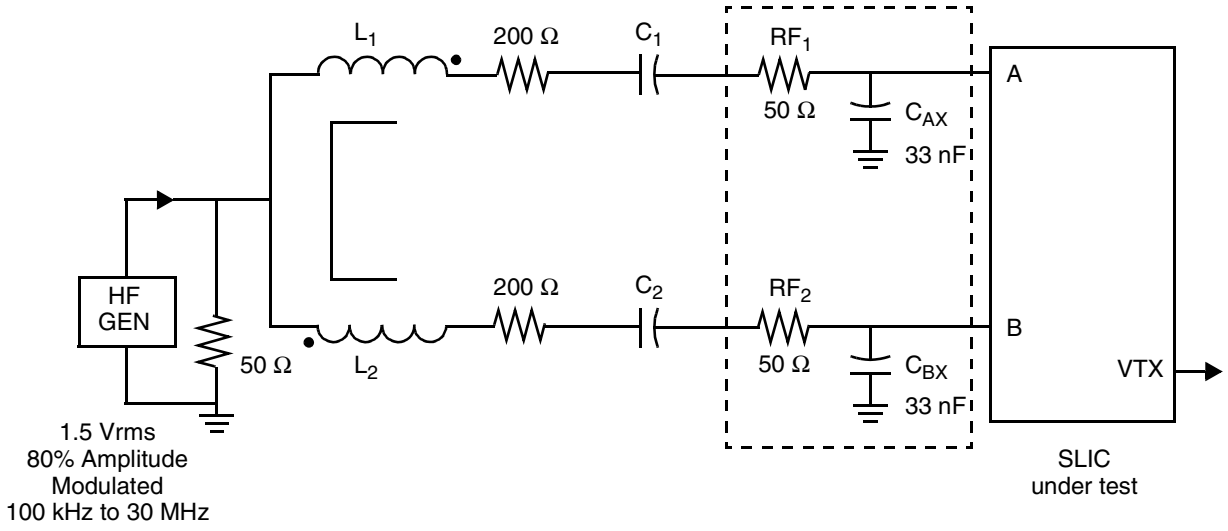


Note:
Z_D is the desired impedance (e.g., the characteristic impedance of the line).

$Return\ Loss = -20 \log (2\ V_M / V_S)$

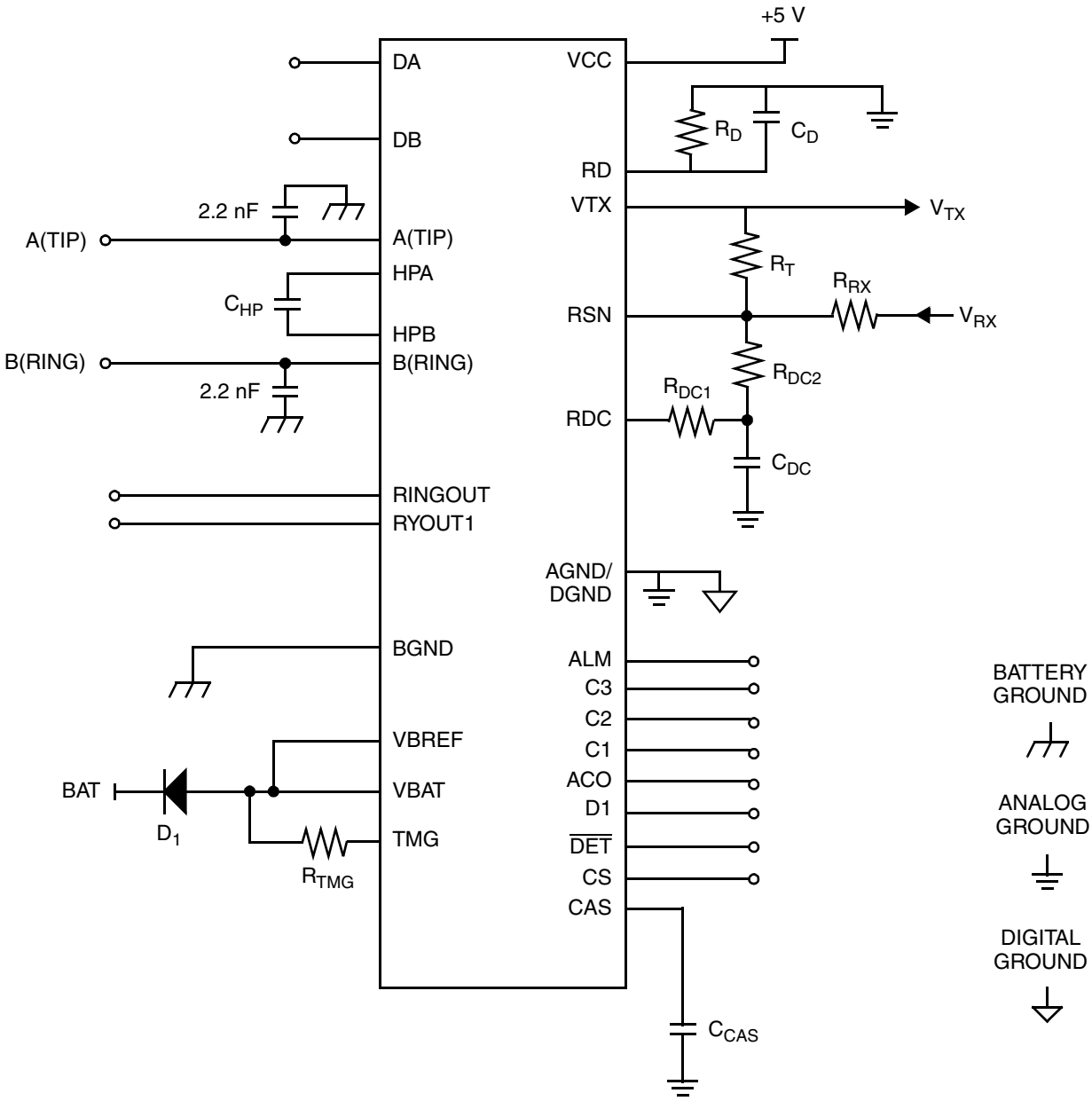
D. Two-Wire Return Loss Test Circuit

TEST CIRCUITS (continued)

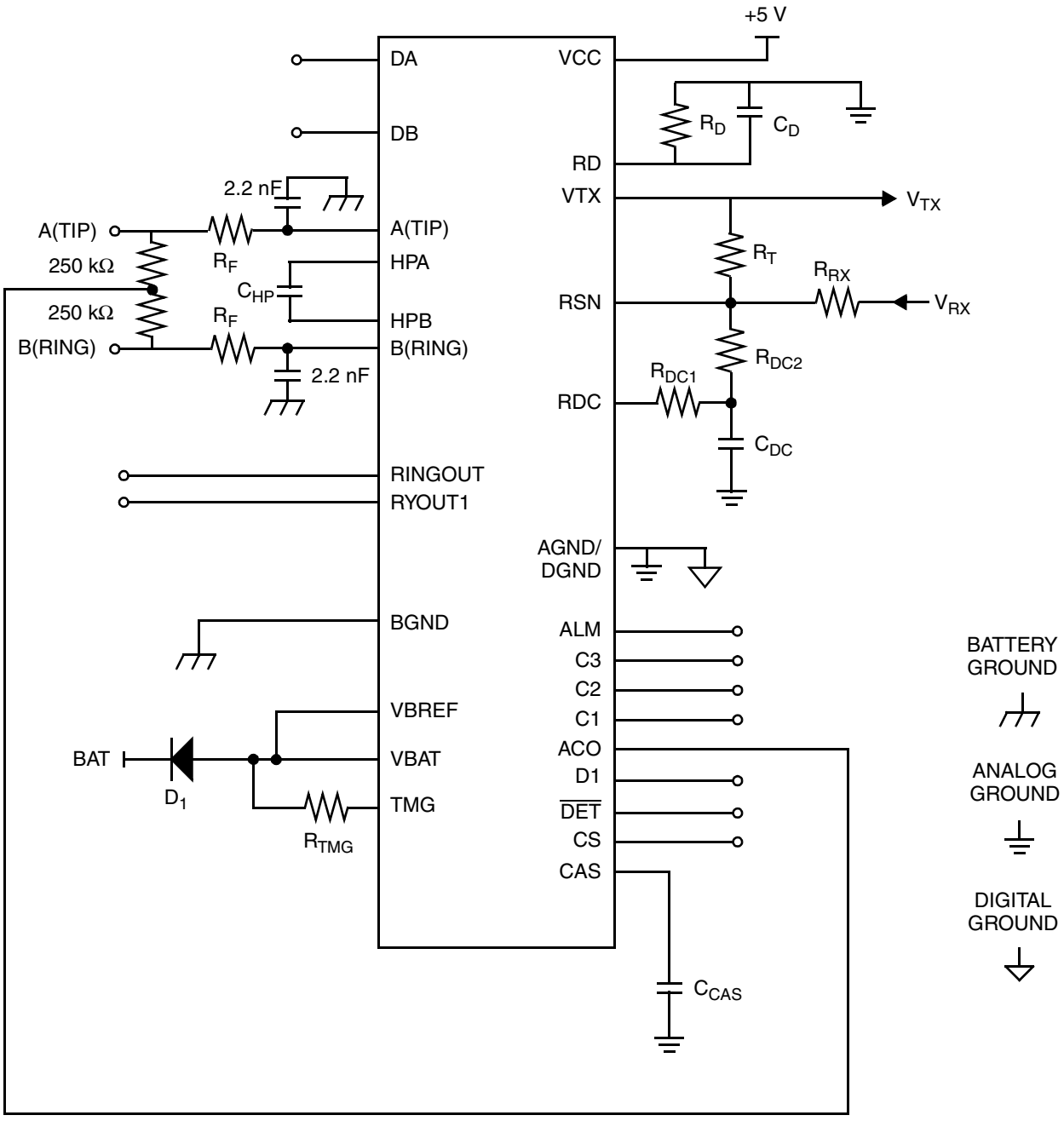


E. RFI Test Circuit

TEST CIRCUITS (continued)



F. Le7925 Test Circuit

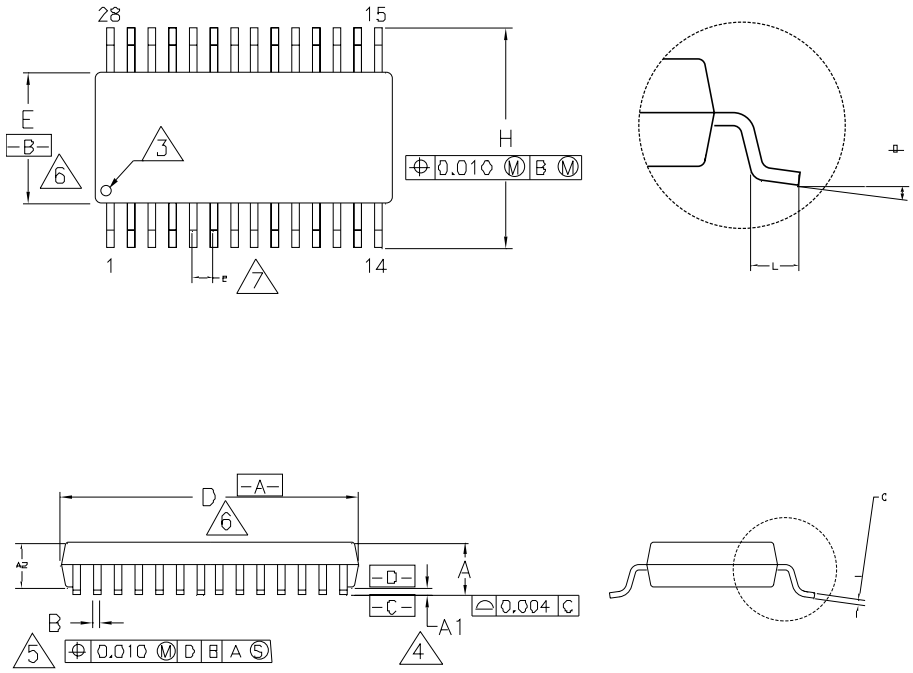


G. Le7925 Application Circuit

PHYSICAL DIMENSIONS

SOIC 028 (Wide Body)

28 SOP WIDE BODY



PACKAGE	28 SOP WIDE BODY		
JEDEC	MO-059 (B) AC		
SYMBOL	MIN.	NOM.	MAX.
A	.080	.095	.100
A1	.002	.007	.014
A2	.086	.088	.090
B	.014	.016	.020
C	.006	.008	.0125
D	.697	.714	.728
E	.324	.346	.350
e	.050 BSC		
H	.453	.470	.500
L	.016	.031	.050
θ	0°	4°	8°

NOTES:

1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. PIN 1 ID SHALL BE LOCATED ADJACENT TO PIN 1.
4. DIMENSION A1 IS MEASURED FROM THE BASE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE IS ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE (SEATING PLANE).
5. DIMENSION "B" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT EXCEED 0.006 INCHES PER SIDE.
6. DIMENSIONS "D" AND "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DO INCLUDE MOLD MISMATCH AS MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
7. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.
8. LEAD COPLANARITY SHALL BE WITHIN 0.004 INCHES AS MEASURED FROM THE SEATING PLANE.

REVISION HISTORY

Revision A1 to B1

- In Specifications, Thermal Performance, THD, changed 7 dBm to 4.7 dBm
- Updated Physical Dimensions drawing

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