T-51-10-90

MICRO POWER SYSTEMS

CMOS
13-Bit Monolithic A/D Converter
MP7550

FEATURES

- **Resolution: 13 Bits, 2's Complement**
- **Relative Accuracy: ±1/2 LSB**
- **"Quad Slope" Precision**
  - **Gaindrift: 1 ppm/°C**
  - **Offsetdrift: 1 ppm/°C**
- **Microprocessor Compatible**
- **Ratiometric**
- **Overrange Flag**
- **Very Low Power Dissipation**
- **TTL/CMOS Compatible**
- **CMOS Monolithic Construction**
- **Replaces AD7550**

GENERAL DESCRIPTION

The MP7550 is a 13-bit (2's complement) monolithic CMOS analog-to-digital converter on a 118 x 125 mil die packaged in a 40-pin ceramic DIP. Outstanding accuracy and stability (1 ppm/°C) is obtained due to its revolutionary integrating technique, called "Quad Slope." This conversion consists of four slopes of integration as opposed to the traditional dual slope and provides much higher precision.

The MP7550 parallel output data lines have three-state logic and are microprocessor compatible through the use of two enable lines which control the lower eight LSB's (low byte enable) and the five MBS's (high byte enable). An overrange flag is also available which together with the BUSY and $\overline{\text{BUSY}}$ flags can be interrogated through the STATUS ENABLE providing easy microprocessor interface.

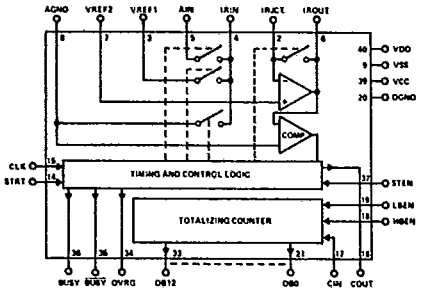
The MP7550 conversion time is about 40 ms with a 1 MHz clock. Clock can be externally controlled or internally generated by simply connecting a capacitor to the clock pin. A positive start pulse can be self-generated by having a capacitor on the start pin or can be externally applied.

For most applications, the MP7550 needs only three resistors, one capacitor, and a reference voltage since the integrating amplifier, comparator, switches and digital logic are all on the CMOS chip.

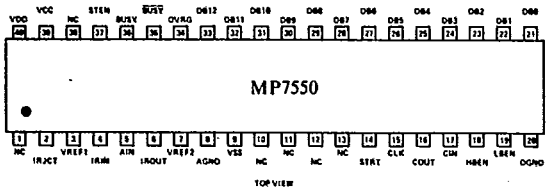
A wide range of power supply voltages (±5V to ±12V) with minuscule current requirements make the MP7550 ideal for low power and/or battery operated applications. Selection of the logic (VCC) supply voltage (+5V to VDD) provides direct TTL or CMOS interface on the digital input/output lines.

The MP7550 uses a high density CMOS process featuring double layer metal and silicon nitride passivation to ensure high reliability and long-term stability.

FUNCTIONAL DIAGRAM



PIN CONFIGURATION



See Section 7 for Ordering Information

(VDD = +12V, VSS = −5V, VCC = +5V, VREF1 = +4.25V unless otherwise noted)

PARAMETER[1]		TA = +25°C			OVER SPECIFIED TEMPERATURE RANGE		UNITS	TEST CONDITIONS
		MIN	TYP	MAX	MIN	MAX		
ACCURACY Resolution					13		Bits 2's Comp	f_{CLK} = 100 KHz, R_1 = 1 MΩ, C_1 = 0.005 μF, IRJCT Voltage Adjusted to $\frac{VREF1}{2}$ ±0.6%
Relative Accuracy				±0.5		±0.5	LSB	
Gain Error				±0.5			LSB	
Gain Error Drift[3]			1				ppm/°C	
Offset Error				±0.5			LSB	
Offset Error Drift[3]			1				ppm/°C	
ANALOG INPUTS AIN Input Resistance[2]		R_1					MΩ	
VREF1 Input Resistance[2]		R_1					MΩ	
VREF2 Leakage Current			10				pA	
DIGITAL INPUTS								
	INPUTS							
V_{INL}	CIN,			+0.8		+0.8	V	VCC = +5V
V_{INH}	LBEN,	+2.4			+2.4		V	
V_{INL}	HBEN,			+1.2		+1.2	V	VCC = +12V
V_{INH}		+10.8			+10.8		V	
I_{INL}, I_{INH}	STEN		5				nA	
V_{INL}	STRT			+0.8		+0.8	V	VCC = +5V to VDD
V_{INH}		+2.4			+2.4		V	
I_{INL}			−1				μA	VCC = +5V to VDD, BUSY = Low,
I_{INH}			+150				μA	VCC = +5V to VDD, BUSY = High
V_{INL}	CLK			+0.8		+0.8	V	VCC = +5V
V_{INH}		+3			+3		V	
V_{INL}				+1.2		+1.2	V	VCC = +12V
V_{INH}		+10.8			+10.8		V	
I_{INL}			−100				μA	V_{IN}=V_{INL};VCC = +5V to +12V
I_{INH}			+100				μA	V_{IN}=V_{INH};VDD = +5V to +12V
DIGITAL OUTPUTS V_{OUTL}				+0.5		+0.8	V	VCC = +5V, I_{SINK} = 1.6 mA
V_{OUTH}		+2.4			+2.4			VCC = +5V, I_{SOURCE} = 40 μA
V_{OUTL}				+1.2		+1.2	V	VCC = +12V, I_{SINK} = 1.6 mA
V_{OUTH}		+10.8			+10.8		V	VCC = +12V, I_{SOURCE} = 0.6 mA
Capacitance[3] (Floating State) (OVRG, $\overline{BUSY}$, BUSY, and DB0–DB12)			5				pF	

Specifications (cont.)

PARAMETER[1]	TA = +25°C			OVER SPECIFIED TEMPERATURE RANGE		UNITS	TEST CONDITIONS
	MIN	TYP	MAX	MIN	MAX		
DIGITAL OUTPUTS (con't)							
I_{LKG} (Floating State) (OVRG, $\overline{BUSY}$, BUSY, and DB0–DB12)		±5				nA	VCC = +5V to +12V V_{OUT} = 0V and VCC
DYNAMIC PERFORMANCE[3]							
Conversion Time		40				ms	$V_{IN(CLK)}$ = 0 to +3V, f_{CLK} = 1 MHz
STEN, HBEN, LBEN Propagation Delay t_{ON}, t_{OFF}		250	500			ns	V_{IN} (STEN, HBEN, LBEN) 0 to +3V
External STRT Pulse Duration	800					ns	$V_{IN(STRT)}$ = 0 to +3V
POWER SUPPLIES							
VDD Range	+10		+12			V	
VSS Range	−5		−12			V	
VCC Range	+5		VDD			V	
IDD		0.6	2			mA	f_{CLK} = 1 MHz
ISS		0.3	2			mA	
ICC		0.06	2			mA	

Notes
1 Specifications subject to change without notice.

2 The equivalent input circuit is the integrator resistor R_1 (1 MΩ MIN, 10 MΩ MAX) in series with a voltage source $\frac{VREF1}{2}$, (See Figure 1.)
3. Guaranteed but not production tested.

ABSOLUTE MAXIMUM RATINGS

VDD to AGND . . . . . 0V, +14V
VDD to DGND . . . . . 0V, +14V
VSS to AGND . . . . . 0V, −14V
VSS to DGND . . . . . 0V, −14V
AGND to DGND . . . . . 0V, +14V
VCC to DGND. . . . . 0V, VDD
VREF1 . . . . . VSS, VDD
VREF2 . . . . . AGND, VDD
AIN . . . . . VSS, VDD
IRIN . . . . . VSS, VDD
IRJCT . . . . . AGND, VDD
IROUT . . . . . VSS, VDD
Digital Input Voltage
HBEN, LBEN, STEN, CIN . . . . DGND, (DGND+27V)
CLK, START . . . . . DGND, VDD
Digital Output Voltage
DB0–DB12, OVRG, BUSY, $\overline{BUSY}$, COUT . DGND, VCC
Power Dissipation (Package)
Up to +50°C . . . . . 1000 mW
Derates above +50°C by . . . . . 10 mW/°C
Storage Temperature. . . . . −65°C to +150°C
Operating Temperature . . . . . −25°C to +85°C

CAUTION:

1. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times. Prior to pulling the devices from the conductive foam, ground the foam to deplete any accumulated charge.
2. VCC should never exceed VDD by more than 0.4V, especially during power ON or OFF sequencing.

Pin Function Description

PIN	MNEMONIC	DESCRIPTION
1	NC	No Connection
2	IRJCT	IntegratoR JunCTion. Summing junction (negative input) of integrating amplifier.
3	VREF1	Voltage REFerence Input
4	IRIN	IntegratoR INput. External integrator input R is connected between IRJCT and IRIN.
5	AIN	Analog INput. Unknown analog input voltage to be measured. Full-scale AIN equals VREF/2.125.
6	IROUT	IntegratoR OUTput. External integrating capacitor C_1 is connected between IROUT and IRJCT.
7	VREF2	Voltage REFerence ÷ 2 Input
8	AGND	Analog GrouND
9	VSS	Negative Supply (−5V to −12V)
10	NC	No Connection
11	NC	No Connection
12	NC	No Connection
13	NC	No Connection
14	STRT	STaRT Conversion. When STRT goes to a logic "1," the MP7550's digital logic is set up and BUSY is latched ""high." When STRT returns "low," conversion begins in synchronization with CLK. Reinitiating STRT during conversion causes a conversion restart. STRT can be driven from an external logic source, or can be programmed for continuous conversion by connecting an external capacitor between STRT and DGND. An externally applied STRT command must be a positive pulse of at least 800 nanoseconds to ensure proper set-up of the MP7550 logic.
15	CLK	CLocK Input. The CLK can be driven from external logic, or can be programmed for internal oscillation by connecting an external capacitor between CLK and DGND.
16	COUT	Count OUT provides a number (N) of gated clock pulses given by: $N = \left(\frac{AIN}{VREF1}\ 2.125 + 1\right)\ 4096$
17	CIN	Count IN is the input to the output counter. 2's complement binary data appears on the DB0 through DB12 output lines (if the HBEN and LBEN enable lines are "high") if COUT is connected to CIN.

PIN	MNEMONIC	DESCRIPTION
18	HBEN	High Byte ENable is the three-state logic enable input for the DB8–DB12 data outputs. When HBEN is low, the DB8–DB12 outputs are floating. When HBEN is "high," digital data appears on the data lines.
19	LBEN	Low Byte ENable is the three-state logic enable for DB0–DB7. When LBEN is "low," DB0–DB7 are floating. When "high," digital data appears on the data lines.
20	DGND	Digital GrouND is the ground return for all digital logic and the comparator.
21	DB0	Data Bit 0 (least significant bit)
22	DB1	
23	DB2	
24	DB3	
25	DB4	
26	DB5	
27	DB6	CODE: 2's Complement
28	DB7	
29	DB8	
30	DB9	
31	DB10	
32	DB11	
33	DB12	Data Bit 12 (most significant bit)
34	OVRG	OVer Range indicates a logic "1" if AIN exceeds plus or minus full scale by at least 1/2 LSB. OVRG is a three-state output and floats until STEN is addressed with a logic "1."
35	$\overline{BUSY}$	Not BUSY. $\overline{BUSY}$ indicates whether conversion is complete or in progress. $\overline{BUSY}$ is a three-state output which floats until STEN is addressed with a logic "1." When addressed, $\overline{BUSY}$ will indicate either a "1" (conversion complete) or a "0" (conversion in progress).
36	BUSY	BUSY indicates conversion status. BUSY is a three-state output which floats until STEN is addressed with a logic "1." When addressed, BUSY indicates a "0" (conversion complete) or a "1" (conversion in progress.)
37	STEN	STatus ENable is the three-state control input for BUSY, $\overline{BUSY}$, and OVRG.
38	NC	No Connection
39	VCC	Logic Supply. Digital inputs and outputs are TTL compatible if VCC = +5V, CMOS compatible for VCC = +10V to VDD.
40	VDD	Positive Supply. +10V to +12V.

2

Principles of Operation

BASIC OPERATION

The essence of the quad slope technique is best explained through Figures 1 and 2.

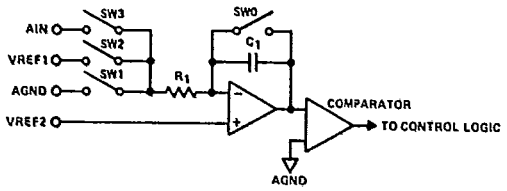


Figure 1. Quad Slope Integrator Circuit

The inputs AGND (analog ground), VREF1, AIN (analog input) and VREF1 are applied in sequence to an integrator (Figure 1), creating four slopes (phases 1 through 4, Figure 2) at the integrator output. Voltage VREF2 is normally equal to $\frac{VREF1}{2}$, but if not, will create an error count "n" that will be minimized by the "quad-slope" conversion process. VREF1 and VREF2 must be positive voltages.

The equivalent integrator input voltages and their integration times are shown in Table I.

TABLE I
INTEGRATOR EQUIVALENT INPUT VOLTAGES AND INTEGRATION TIMES

Phase	Input Voltage	Integration Time
1	AGND–VREF2	$t_1 = K_1t$
2	VREF1–VREF2	$t_2 = (K_1 + n)t$
3	AIN–VREF2	$t_3 = (2K_1 - n)t$
4	VREF1–VREF2	$t_4 = (K_3 - 2K_1 + n - 2N)t$

where:
- t = The CLK period
- n = System error count
- K_1 = A fixed count equal to 4352 counts
- K_2 = A fixed count equal to 17408 counts ($K_2 = 4K_1$)
- K_3 = A fixed count equal to 25600 counts
- N = Digital output count corresponding to the analog input voltage, AIN

PHASE 0
After the start pulse is applied, switch SW2 is closed (all other switches open) and the integrator output is ramped to comparator zero crossing. Phase 0 can be considered the reset phase of the converter, and always has a duration $t_0 = R_1C_1$ (integrator time constant). Upon zero crossing, counters K_1 and K_2 are started, switch SW2 is opened and SW1 is closed.

PHASE 1
Phase 1 integrates (AGND − VREF2) for a fixed period of time (by counter K_1) equal to $t_1 = K_1t$. At the end of phase 1, switch SW1 is opened and SW2 is closed.

PHASE 2
The integrator input is switched to (VREF1−VREF2) and the output ramps down until zero crossing is achieved. The integration time $t_2 = (K_1 + n)t$ includes the error count "n" due to offsets, etc. At the end of phase 2, switch SW2 is opened, SW3 is closed, and a third counter (K_3) is started.

PHASE 3
Phase 3 integrates the analog input (AIN − VREF2) until counter K_2 counts $4K_1t$. At this time SW3 is opened and SW2 is closed again.

PHASE 4
Phase 4 integrates (VREF1−VREF2) and the comparator output ramps down until zero crossing once again is achieved. Since the comparator always approaches zero crossing from the same slope, propagation delay is constant and hysteresis effect is eliminated.

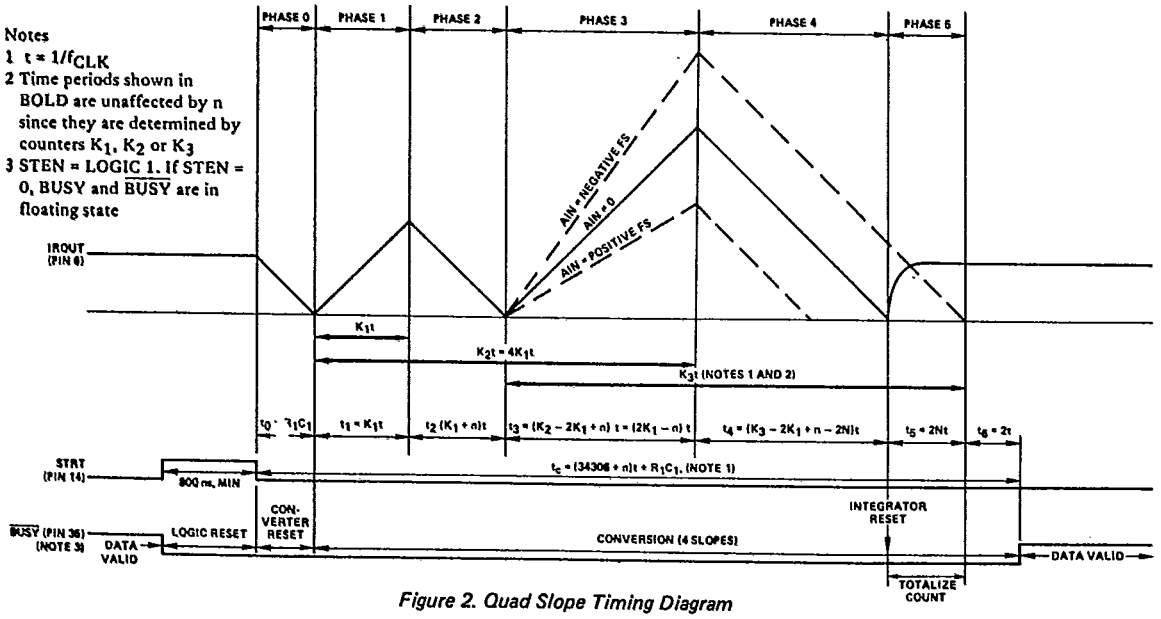


Figure 2. Quad Slope Timing Diagram

Principles of Operation (cont.)

BASIC OPERATION (continued)

The time t_5 between the phase 4 zero crossing and the termination of counter K_3 is considered equal to 2N counts. N, the number of counts at the COUT terminal, is obtained by a divide-by-two counter stage. This reduces "jitter" effects. Barring third (and higher) order effects, it can be proven that:

(EQN 1)

$$N = \underbrace{\left(\frac{AIN}{VREF1} - 1\right) \cdot 2K_1 + \frac{K_3}{2}}_{\text{ideal transfer function}} + \underbrace{\left(\frac{AIN}{VREF1} - 1\right) \cdot \left[\frac{AGND}{VREF1}(1 + 2\alpha) - \alpha^2\right] \cdot 2K_1}_{\text{error term}}$$

where:

$$\alpha = \frac{2VREF2 - VREF1}{VREF1}$$

The ideal case assumes:

AGND = 0V

$VREF2 = \frac{VREF1}{2}$, therefore $\alpha = 0$

Then (EQN 1) simplifies to:

$$\boxed{N = \frac{AIN}{VREF1} \cdot 8704 + 4096} \quad \text{(EQN 2)}$$

or

$$\boxed{N = \frac{AIN}{V_{FS}} \cdot 4096 + 4096} \quad \text{(EQN 3)}$$

where:

V_{FS} = full scale input voltage = $\frac{VREF1}{2.125}$

The parallel output (DB0–DB12) of the MP7550 represents the number N in binary 2's complement coding when the COUT pin is connected to the CIN pin (see Table II).

TABLE II
OUTPUT CODING (Bipolar 2's Complement)

Analog Input (Note 1)	N (Note 2)	Parallel Digital Output (Note 3)												
		OVRG	DB12											DB0
+Overrange	—	1	0	1	1	1	1	1	1	1	1	1	1	1
+VFS (1-2⁻¹²)	8191	0	0	1	1	1	1	1	1	1	1	1	1	1
+VFS (2⁻¹²)	4097	0	0	0	0	0	0	0	0	0	0	0	0	1
0	4096	0	0	0	0	0	0	0	0	0	0	0	0	0
−VFS (2⁻¹²)	4095	0	1	1	1	1	1	1	1	1	1	1	1	1
−VFS	0	0	1	0	0	0	0	0	0	0	0	0	0	0
−Overrange	—	1	1	0	0	0	0	0	0	0	0	0	0	0

Notes
1 VFS = $\frac{VREF1}{2.125}$
2 N = number of counts at COUT pin
3 COUT strapped to CIN; LBEN and HBEN = logic 1

ERROR ANALYSIS

Equation 1 shows that only α and AGND generate error terms. Their impact can be analyzed as follows:

Case 1: AGND = 0, $\alpha \neq 0$

Error sources such as capacitor-leakage (I_L) and op amp offset (e) cause α to be different from zero.

Under this condition,

$$\alpha = \frac{2(e + I_L R_1)}{VREF1}$$

where $I_L R_1$ is the equivalent error voltage generated by leakage I_L.

The evaluation of this error term is best demonstrated through the following example:

Assume:

e = 5 mV, I_L = 5 nA, R_1 = 1 MΩ and VREF1 = 4.25V.

Then:

$\alpha = 4.7 \times 10^{-3}$

and:

$$N = \left[\frac{AIN}{VREF1} - 1\right] \times 8704 + 12800 - \underbrace{\left[\frac{AIN}{VREF1} - 1\right] \times 22.1 \times 10^{-6} \times 8704}_{\text{error term } N_\epsilon}$$

Therefore, the error count N_ϵ is as follows:

For AIN = $-V_{FS}$: N_ϵ = 0.28 counts = 0.28 LSB
AIN = 0: N_ϵ = 0.19 counts = 0.19 LSB
AIN = $+V_{FS}$: N_ϵ = 0.09 counts = 0.09 LSB

The above example shows the strong reduction of the circuit errors because of the α^2 term in (EQN 1). Another consequence of this effect is that N_ϵ is always positive, regardless of the polarity of the circuit errors.

Case 2: AGND ≠ 0, α = 0

When AGND is different from the signal ground, then this error will come through on a first-order basis. Indeed:

$$N = \left[\frac{AIN}{VREF1} - 1\right] \cdot 8704 + 12800 + \underbrace{\left[\frac{AIN}{VREF1} - 1\right] \cdot \frac{AGND}{VREF1}}_{\text{error term } N_\epsilon}$$

The following example demonstrates the impact of AGND.

Let AGND = 1 mV and VREF1 = 4.25V.

For AIN = $-V_{FS}$, then N_ϵ = 3.01 counts
AIN = 0, then N_ϵ = 2.05 counts
AIN = $+V_{FS}$, then N_ϵ = 1.08 counts

Therefore, ground loops should be minimized because a 330 μV difference between AGND and signal ground will cause 1 count (1 LSB) of error when the analog input is at minus full scale. An optimized ground system is shown in Figure 7.

Operation Guidelines

OPERATING GUIDELINES

The following steps, in conjunction with Figure 3, explain the calculations of the component values required for proper operation.

1. DETERMINATION OF VREF1

When the full scale voltage requirement (VFS) has been ascertained, the reference voltage can be calculated by:

$$VREF1 = 2.125\ (VFS)$$

VREF1 must be positive for proper operation.

2. SELECTION OF C_3 (INTERNAL CLOCK OPERATION)

For internal clock operation, connect capacitor C_3 to the clock pin as shown in Figure 3. The clock frequency versus capacitor C_3 is shown in Figure 4.

The clock frequency must be limited to 1.3 MHz for proper operation.

3. SELECTION OF INTEGRATOR COMPONENTS (R_1 AND C_1)

To ensure that the integrator's output doesn't saturate to its bound (VDD) during the phase (3) integration cycle, the integrator time constant (R_1C_1) should be approximately equal to:

$$\tau = R_1C_1 = \frac{VREF1\ (9 \times 10^3)}{f_{CLK}\ (VDD - 4V)}$$

The integrator components R_1 and C_1 can be selected by referring to Figure 5 and/or Figure 6. Figure 5 plots the time constant (R_1C_1) versus clock frequency for different reference voltages. Figure 6 is a direct plot of the required C_1 versus f_{CLK} for R_1 values of 1 MΩ and 10 MΩ.

R_1 can be a standard 10% resistor, but must be selected between 1 MΩ to 10 MΩ.

The integrating capacitor "C_1" must be a low leakage, low dielectric absorption type such as teflon, polystyrene or polypropylene. To minimize noise, the outside foil of C_1 must be connected to IROUT.

4. CONVERSION TIME

As shown in Figure 2, the conversion time is independent of the analog input voltage AIN, and is given by:

$$t_{convert} = t_{STRT} + \frac{34306}{f_{CLK}} + R_1C_1$$

where:

t_{STRT} = STRT pulse duration
R_1C_1 = Integrator Time Constant
f_{CLK} = CLK Frequency

For example, if VREF1 = 4.25V, R_1 = 1 MΩ, C_1 = 400 pF and CLK = 1 MHz, the conversion time (not including t_{STRT}, which is normally only microseconds in duration) is approximately 40 milliseconds.

5. EXTERNAL OR AUTO STRT OPERATION

The STRT pin can be driven externally, or with the addition of C_2, made to self-start.

The size of C_2 determines the length of time from end of conversion until a new conversion is initiated. This is the "data valid" time and is given by:

$$t_{DAV} \approx (1.7 \times 10^6\Omega)\ C_2 + 20\ \mu s$$

When first applying power to the MP7550, a 0V to VDD positive pulse (power up restart) is required at the STRT terminal to initiate auto STRT operation.

6. INITIAL CALIBRATION

Trim R_4 (Figure 3) so that pin 2 (IRJCT) equals 1/2 VREF1 ±0.6%. When measuring the voltage on IRJCT, apply a logic 1 to the STRT terminal.

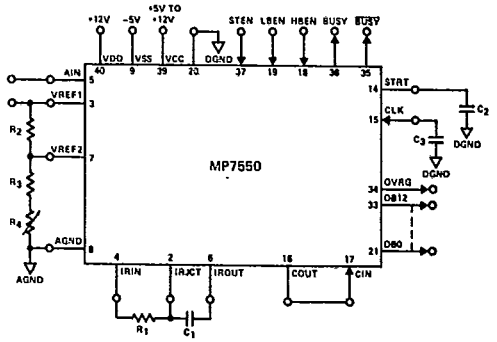


Figure 3. Operation Diagram

Operation Guidelines (cont.)

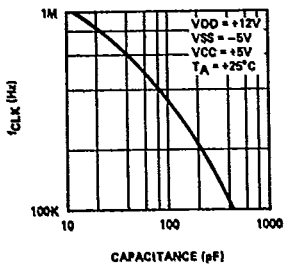


Figure 4. f_{CLK} vs. C_3

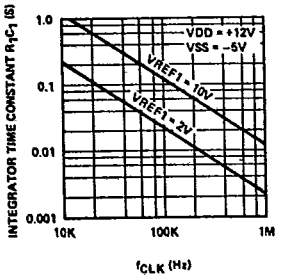


Figure 5. Integrator Time Constant (R_1C_1) vs. f_{CLK} for Different Reference Voltages

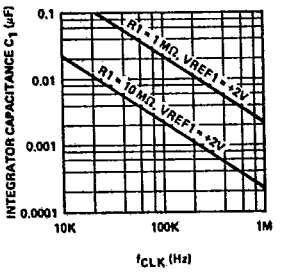


Figure 6. Integrator Capacitance (C_1) vs. f_{CLK} for Different Integrator Resistances (R_1)

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APPLICATION HINTS

When operating at f_{CLK} greater than 500 KHz, the following steps are recommended to minimize errors due to noise coupling, (see Figure 7).

1. Decouple AIN (pin 5), VREF1 (pin 3) and VREF2 (pin 7) through 0.01 μF to signal ground.
2. Signal ground must be located as close to pin 8 (AGND) as possible.
3. Keep the lead lengths of R_1 and C_1 toward pin 2 (IRJCT) as short as possible. In addition, both components should lie over the analog ground plane. If C_1 has an outside foil, connect it to pin 6 (IROUT), not pin 2.
4. Hold the data bit enables (HBEN, LBEN) in the 0 state during conversion. This is easily accomplished by tying $\overline{\text{STEN}}$ to the 1 state and driving HBEN and LBEN with $\overline{\text{BUSY}}$. This prevents the DB0 through DB12 outputs from coupling noise into the integrator during the phase 1–4 active integration periods.

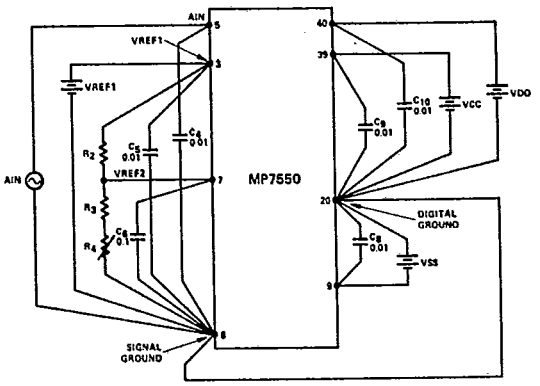

Figure 7. Ground System