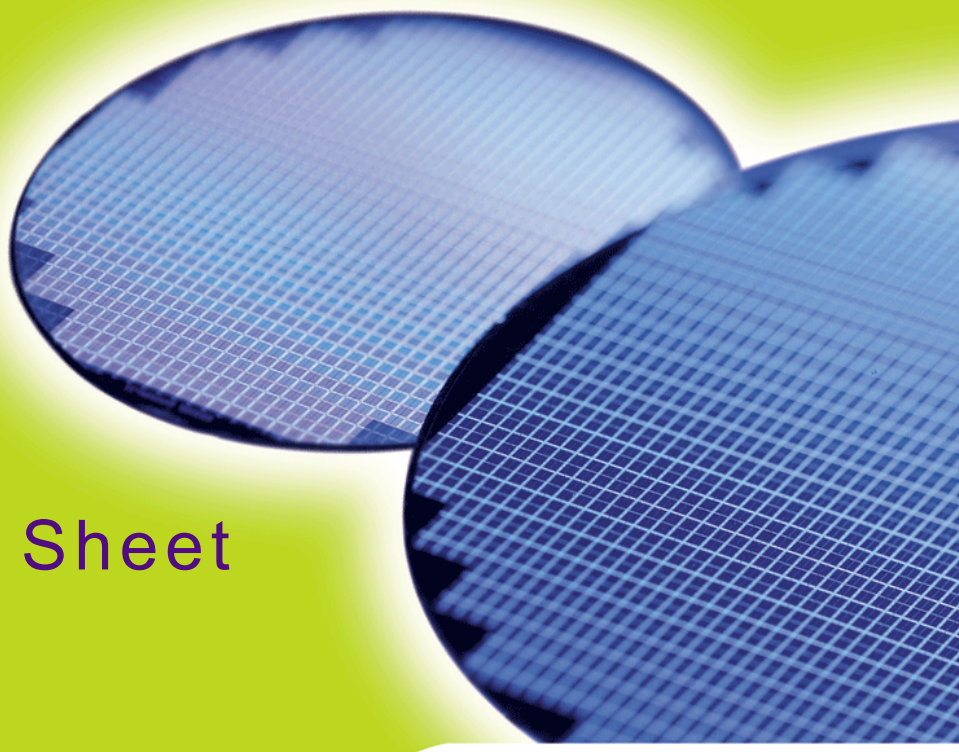
December 2007

HYB18H512321BF–11/12/14
HYB18H512321BF–08/10

512-Mbit GDDR3 Graphics RAM
GDDR3 Graphics RAM
RoHS compliant



Internet Data Sheet

Rev. 1.3

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HYB18H512321BF–11/12/14
HYB18H512321BF–08/10

Revision History: 2007-12, Rev. 1.3

Page	Subjects (major changes since last revision)
33	Table 20, t_{WR} for Speed bins -8 and -10 changed from 14 to 13
34	Table 20, t_{XSNR} (Self refresh exit followed by non-Read command) added
Previous Revision: Rev. 1.2, 2007-11	
All	Boundary Scan deleted
32	Table 20 f_{CK}(min) for CL 10 to 7 changed from 400 to 350 MHz and note 1, 2 updated.
Previous Revision: Rev. 1.1, 2007-09	
32	Table 20 max. CL changed from 16 to 13
Previous Revision: Rev. 1.0, 2007-05	
32	Table 20 - Timing Parameters for -8 updated

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1 Overview

This chapter lists all main features of the product family HYB18H512321BF and the ordering information.

1.1 Features

- 2.0 V V_{DDQ} IO voltage HYB18H512321BF–08/10
- 2.0 V V_{DD} core voltage HYB18H512321BF–08/10
- 1.8 V V_{DDQ} IO voltage HYB18H512321BF–11/12/14
- 1.8 V V_{DD} core voltage HYB18H512321BF–11/12/14
- Organization: 2048K × 32 × 8 banks
- 4096 rows and 512 columns (128 burst start locations) per bank
- Differential clock inputs (CLK and $\overline{CLK}$)
- CAS latencies of 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17
- Write latencies of 3, 4, 5, 6, 7
- Burst sequence with length of 4, 8.
- 4n pre fetch
- Short RAS to CAS timing for Writes
- t_{RAS} Lockout support
- t_{WR} programmable for Writes with Auto-Precharge
- Data mask for write commands
- Single ended READ strobe (RDQS) per byte. RDQS edge-aligned with READ data
- Single ended WRITE strobe (WDQS) per byte. WDQS center-aligned with WRITE data
- DLL aligns RDQS and DQ transitions with Clock
- Programmable IO interface including on chip termination (ODT)
- Autoprecharge option with concurrent auto precharge support
- 8k Refresh (32ms)
- Autorefresh and Self Refresh
- PG–TFBGA–136 package (10mm × 14mm)
- Calibrated output drive. Active termination support
- RoHS Compliant Product[1)]

green Product

TABLE 1
Ordering Information

Part Number[1)]	Organisation	Clock (MHz)	Package
HYB18H512321BF–11/12/14 HYB18H512321BF–08/10	×32	1200/1000/900/800/700	PG–TFBGA–136

1) HYB: designator for memory components
18H: V_{DDQ} = 1.8 V
512: 512-Mbit density
32: Organization
B: Product revision
F: Lead- and Halogen-Free

1) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.

1.2 Description

The Qimonda 512-Mbit GDDR3 Graphics RAM is a high speed memory device, designed for high bandwidth intensive applications like PC graphics systems. The chip's 8 bank architecture is optimized for high speed.

HYB18H512321BF uses a double data rate interface and a 4n-pre fetch architecture. The GDDR3 interface transfers two 32 bit wide data words per clock cycle to/from the I/O pins. Corresponding to the 4n-pre fetch a single write or read access consists of a 128 bit wide, one-clock-cycle data transfer at the internal memory core and four corresponding 32 bit wide, one-half-clock-cycle data transfers at the I/O pins.

Single-ended unidirectional Read and Write Data strobes are transmitted simultaneously with Read and Write data respectively in order to capture data properly at the receivers of both the Graphics SDRAM and the controller. Data strobes are organized per byte of the 32 bit wide interface. For read commands the RDQS are edge-aligned with data, and the WDQS are center-aligned with data for write commands.

The HYB18H512321BF operates from a differential clock (CLK and $\overline{\text{CLK}}$). Commands (addresses and control signals) are registered at every positive edge of CLK. Input data is registered on both edges of WDQS, and output data is referenced to both edges of RDQS.

In this document references to "the positive edge of CLK" imply the crossing of the positive edge of CLK and the negative edge of $\overline{\text{CLK}}$. Similarly, the "negative edge of CLK" refers to the crossing of the negative edge of CLK and the positive edge of $\overline{\text{CLK}}$. References to RDQS are to be interpreted as any or all RDQS<3:0>. WDQS, DM and DQ should be interpreted in a similar fashion.

Read and write accesses to the HYB18H512321BF are burst oriented. The burst length is fixed to 4 and 8 and the two least significant bits of the burst address are "Don't Care" and internally set to LOW. Accesses begin with the registration of an ACTIVATE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVATE command are used to select the bank and the row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the column location for the burst access. Each of the 8 banks consists of 4096 row locations and 512 column locations. An AUTO PRECHARGE function can be combined with READ and WRITE to provide a self-timed row precharge that is initiated at the end of the burst access. The pipe lined, multibank architecture of the HYB18H512321BF allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

The "On Die Termination" interface (ODT) is optimized for high frequency digital data transfers and is internally controlled. The termination resistor value can be set using an external ZQ resistor or disabled through the Extended Mode Register.

The output driver impedance can be set using the Extended Mode Register. It can either be set to ZQ / 6 (auto calibration) or to 35, 40 or 45 Ohms.

Auto Refresh and Power Down with Self Refresh operations are supported.

An industrial standard PG–TFBGA–136 package is used which enables ultra high speed data transfer rates and a simple upgrade path from former DDR Graphics SDRAM products.

2 Configuration

FIGURE 1
Ballout 512-Mbit GDDR3 Graphics RAM [Top View, MF = Low]

1	2	3	4		5	6	7	8	9	10	11	12
V_{DDQ}	V_{DD}	V_{SS}	ZQ	A					MF	V_{SS}	V_{DD}	V_{DDQ}
V_{SSQ}	DQ0	DQ1	V_{SSQ}	B					V_{SSQ}	DQ9	DQ8	V_{SSQ}
V_{DDQ}	DQ2	DQ3	V_{DDQ}	C					V_{DDQ}	DQ11	DQ10	V_{DDQ}
V_{SSQ}	WDQS0	RDQS0	V_{SSQ}	D					V_{SSQ}	RDQS1	WDQS1	V_{SSQ}
V_{DDQ}	DQ4	DM0	V_{DDQ}	E					V_{DDQ}	DM1	DQ12	V_{DDQ}
V_{DD}	DQ6	DQ5	$\overline{CAS}$	F					$\overline{CS}$	DQ13	DQ14	V_{DD}
V_{SS}	V_{SSQ}	DQ7	BA0	G					BA1	DQ15	V_{SSQ}	V_{SS}
V_{REF}	A1	$\overline{RAS}$	CKE	H					$\overline{WE}$	BA2	A5	V_{REF}
V_{SS}	RFU	RFU	V_{DDQ}	J					V_{DDQ}	$\overline{CK}$	CK	V_{SS}
V_{DD}	A10	A2	A0	K					A4	A6	A8/AP	V_{DD}
V_{SS}	V_{SSQ}	DQ25	A11	L					A7	DQ17	V_{SSQ}	V_{SS}
V_{DD}	DQ24	DQ27	A3	M					A9	DQ19	DQ16	V_{DD}
V_{DDQ}	DQ26	DM3	V_{DDQ}	N					V_{DDQ}	DM2	DQ18	V_{DDQ}
V_{SSQ}	WDQS3	RDQS3	V_{SSQ}	P					V_{SSQ}	RDQS2	WDQS2	V_{SSQ}
V_{DDQ}	DQ28	DQ29	V_{DDQ}	R					V_{DDQ}	DQ21	DQ20	V_{DDQ}
V_{SSQ}	DQ30	DQ31	V_{SSQ}	T					V_{SSQ}	DQ23	DQ22	V_{SSQ}
V_{DDQ}	V_{DD}	V_{SS}	SEN	V					RESET	V_{SS}	V_{DD}	V_{DDQ}

2.1 Ball Definition and Description

TABLE 2
Ball Description

Ball	Type	Detailed Function
CLK, $\overline{\text{CLK}}$	Input	**Clock:** CLK and $\overline{\text{CLK}}$ are differential clock inputs. Address and command inputs are latched on the positive edge of CLK. Graphics SDRAM outputs (RDQS, DQs) are referenced to CLK. CLK and $\overline{\text{CLK}}$ are not internally terminated.
CKE	Input	**Clock Enable:** CKE HIGH activates and CKE LOW deactivates the internal clock and input buffers. Taking CKE LOW provides Power Down. If all banks are precharged, this mode is called Precharge Power Down and Self Refresh mode is entered if a Auto Refresh command is issued. If at least one bank is open, Active Power Down mode is entered and no Self Refresh is allowed. All input receivers except CLK, $\overline{\text{CLK}}$ and CKE are disabled during Power Down. In Self Refresh mode the clock receivers are disabled too. Self Refresh Exit is performed by setting CKE asynchronously HIGH. Exit of Power Down without Self Refresh is accomplished by setting CKE HIGH with a positive edge of CLK. The value of CKE is latched asynchronously by Reset during Power On to determine the value of the termination resistor of the address and command inputs. CKE is not allowed to go LOW during a RD, a WR or a snoop burst.
$\overline{\text{CS}}$	Input	**Chip Select:** $\overline{\text{CS}}$ enables the command decoder when low and disables it when high. When the command decoder is disabled, new commands with the exception of DTERDIS are ignored, but internal operations continue. $\overline{\text{CS}}$ is one of the four command balls.
$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$	Input	**Command Inputs:** Sampled at the positive edge of CLK, $\overline{\text{CAS}}$, $\overline{\text{RAS}}$, and $\overline{\text{WE}}$ define (together with $\overline{\text{CS}}$) the command to be executed.
DQ<0:31>	I/O	**Data Input/Output:** The DQ signals form the 32 bit data bus. During READs the balls are outputs and during WRITEs they are inputs. Data is transferred at both edges of RDQS.
DM<0:3>	Input	**Input Data Mask:** The DM signals are input mask signals for WRITE data. Data is masked when DM is sampled HIGH with the WRITE data. DM is sampled on both edges of WDQS. DM0 is for DQ<0:7>, DM1 is for DQ<8:15>, DM2 is for DQ<16:23> and DM3 is for DQ<24:31>. Although DM balls are input-only, their loading is designed to match the DQ and WDQS balls.
RDQS<0:3>	Output	**Read Data Strobes:** RDQSx are unidirectional strobe signals. During READs the RDQSx are transmitted by the Graphics SDRAM and edge-aligned with data. RDQS have preamble and postamble requirements. RDQS0 is for DQ<0:7>, RDQS1 for DQ<8:15>, RDQS2 for DQ<16:23> and RDQS3 for DQ<24:31>.
WDQS<0:3>	Input	**Write Data Strobes:** WDQSx are unidirectional strobe signals. During WRITEs the WDQSx are generated by the controller and center aligned with data. WDQS have preamble and postamble requirements. WDQS0 is for DQ<0:7>, WDQS1 for DQ<8:15>, WDQS2 for DQ<16:23> and WDQS3 for DQ<24:31>.

Ball	Type	Detailed Function
BA<0:2>	Input	**Bank Address Inputs:** BA select to which internal bank an ACTIVATE, READ, WRITE or PRECHARGE command is being applied. BA are also used to distinguish between the MODE REGISTER SET and EXTENDED MODE REGISTER SET commands.
A<0:11>	Input	**Address Inputs:** During ACTIVATE, A0-A11 defines the row address. For READ/WRITE, A2-A7 and A9 defines the column address, and A8 defines the auto precharge bit. If A8 is HIGH, the accessed bank is precharged after execution of the column access. If A8 is LOW, AUTO PRECHARGE is disabled and the bank remains active. Sampled with PRECHARGE, A8 determines whether one bank is precharged (selected by BA<0:2>, A8 LOW) or all 8 banks are precharged (A8 HIGH). During (EXTENDED) MODE REGISTER SET the address inputs define the register settings. A<0:11> are sampled with the positive edge of CLK.
ZQ	-	**ODT Impedance Reference:** The ZQ ball is used to control the ODT impedance.
RESET	Input	**Reset pin:** The RES pin is a V_{DDQ} CMOS input. RES is not internally terminated. When RES is at LOW state the chip goes into full reset. The chip stays in full reset until RES goes to HIGH state. The Low to High transition of the RES signal is used to latch the CKE value to set the value of the termination resistors of the address and command inputs. After exiting the full reset a complete initialization is required since the full reset sets the internal settings to default.
MF	Input	**Mirror function pin:** The MF pin is a V_{DDQ} CMOS input. This pin must be hardwired on board either to a power or to a ground plane. With MF set to HIGH, the command and address pins are reassigned in order to allow for an easier routing on board for a back to back memory arrangement.
SEN	Input	**Enables Boundary Scan Functionality:** No Boundary Scan support. This pin should be connected to GND.
V_{REF}	Supply	**Voltage Reference:** V_{REF} is the reference voltage input.
V_{DD}, V_{SS}	Supply	**Power Supply:** Power and Ground for the internal logic.
V_{DDQ}, V_{SSQ}	Supply	**I/O Power Supply:** Isolated Power and Ground for the output buffers to provide improved noise immunity.
NC, RFU	-	Please do not connect. Reserved for Future Use balls.

2.2 Mirror Function

The GDDR3 Graphics RAM provides a ball mirroring feature that is enabled by applying a logic HIGH on ball MF. This function allows for efficient routing in a clam shell configuration.

Depending of the logic state applied on MF, the command and address signals will be assigned to different balls. The default ball configuration (see **Figure 2**) corresponds to MF = LOW.

The DC level (HIGH or LOW) must be applied on the MF pin at power up and is not allowed to change after that.

Table 3 shows the ball assignment as a function of the logic state applied on MF.

TABLE 3
Ball Assignment with Mirror

MF Logic State		Signal
LOW	**HIGH**	
H3	H10	$\overline{RAS}$
F4	F9	$\overline{CAS}$
H9	H4	$\overline{WE}$
F9	F4	$\overline{CS}$
H4	H9	CKE
K4	K9	A0
H2	H11	A1
K3	K10	A2
M4	M9	A3
K9	K4	A4
H11	H2	A5
K10	K3	A6
L9	L4	A7
K11	K2	A8
M9	M4	A9
K2	K11	A10
L4	L9	A11
G4	G9	BA0
G9	G4	BA1
H10	H3	BA2

2.3 Truth Tables

2.3.1 Function Truth Table for more than one Activated Bank

If there is more than one bank activated in the Graphics SDRAM, some commands can be performed in parallel due to the chip's multibank architecture. The following table defines for which commands such a scheme is possible. All other transitions are illegal. Notes 1-11 define the start and end of the actions belonging to a submitted command. This table is based on the assumption that there are no other actions ongoing on bank n or bank m. If there are any actions ongoing on a third bank t_{RRD}, t_{RTW} and t_{WTR} have to be taken always into account.

TABLE 4
Function Truth Table I

Current State	Ongoing action on bank n	Possible action in parallel on bank m
ACTIVE	ACTIVATE[1)]	ACT, PRE, WRITE, WRITE/A, READ, READ/A[2)]
	WRITE[3)]	ACT, PRE, WRITE, WRITE/A, READ, READ/A[4)]
	WRITE/A[5)]	ACT, PRE, WRITE, WRITE/A, READ[6)]
	READ[7)]	ACT, PRE, WRITE, WRITE/A, READ, READ/A[8)]
	READ/A[9)]	ACT, PRE, WRITE, WRITE/A, READ, READ/A [8)]
	PRECHARGE[10)]	ACT, PRE, WRITE, WRITE/A, READ, READ/A[11)]
	PRECHARGE ALL [10)]	-
	POWER DOWN ENTRY[12)]	-
IDLE	ACTIVATE 1)	ACT
	POWER DOWN ENTRY [12)]	-
	AUTO REFRESH[13)]	-
	SELF REFRESH ENTRY [12)]	-
	MODE REGISTER SET (MRS)[14)]	-
	EXTENDED MRS [14)]	-
POWER DOWN	POWER DOWN EXIT[15)]	-
SELF REFRESH	SELF REFRESH EXIT[16)]	-

1) Action ACTIVATE starts with issuing the command and ends after t_{RCD}.
2) During action ACTIVATE an ACT command on another bank is allowed considering t_{RRD}, a PRE command on another bank is allowed any time. WR, WR/A, RD and RD/A are always allowed.
3) Action WRITE starts with issuing the command and ends tWR after the first pos. edge of CLK following the last falling WDQS edge.
4) During action WRITE an ACT or a PRE command on another bank is allowed any time. A new WR or WR/A command on another bank must be separated by at least one NOP from the ongoing WRITE. RD or RD/A are not allowed before t_{WTR} is met.
5) Action WRITE/A starts with issuing the command and ends tWR after the first positive edge of CLK following the last falling WDQS edge.
6) During action WRITE/A an ACT or a PRE command on another bank is allowed any time. A new WR or WR/A command on another bank has to be separated by at least one NOP from the ongoing command. RD is not allowed before or t_{WTR} is met. RD/A is not allowed during an ongoing WRITE/A action.
7) Action READ starts with issuing the command and ends with the first positive edge of CLK following the last falling edge of RDQS.
8) During action READ and READ/A an ACT or a PRE command on another bank is allowed any time. A new RD or RD/A command on another bank has to be separated by at least one NOP from the ongoing command. A WR or WR/A command on another bank has to meet t_{RTW}.
9) Action READ/A starts with issuing the command and ends with the first positive edge of CLK following the last falling edge of RDQS.
10) Action PRECHARGE and PRECHARGE ALL start with issuing the command and ends after t_{RP}.

11) During Action ACTIVE an ACT command on another banks is allowed considering t_{RRD} . A PRE command on another bank is allowed any time. WR, WR/A, RD and RD/A are always allowed.
12) During POWER DOWN and SELF REFRESH only the EXIT commands are allowed.
13) AUTO REFRESH starts with issuing the command and ends after t_{RFC}.
14) Actions MODE REGISTER SET and EXTENDED MODE REGISTER SET start with issuing the command and ends after t_{MRD}.
15) Action POWER DOWN EXIT starts with issuing the command and ends after t_{XPN}.
16) Action SELF REFRESH EXIT starts with issuing the command and ends after t_{XSC}.

2.4 Function Truth Table for CKE

TABLE 5
Function Truth Table II (CKE Table)

CKE N-1	CKE n	CURRENT STATE	COMMAND	ACTION
L	L	Power Down	X	Stay in Power Down
		Self Refresh	X	Stay in Self Refresh
L	H	Power Down	DESEL or NOP	Exit Power Down
		Self Refresh	DESEL or NOP	Exit Self Refresh [5]
H	L	All Banks Idle	DESEL or NOP	Entry Precharge Power Down
		Bank(s) Active	DESEL or NOP	Entry Active Power Down
		All Banks Idle	Auto Refresh	Entry Self Refresh

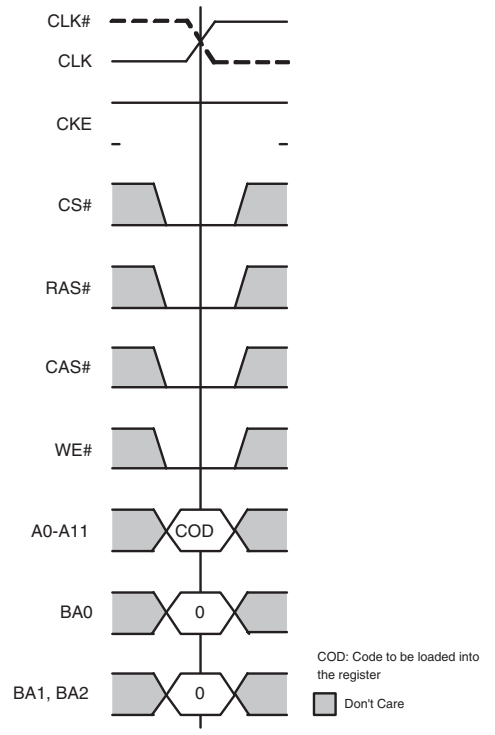
Notes

1. *CKEn is the logic step at clock edge n; CKEn-1 was the state of CKE at the previous clock edge.*
2. *Current state is the state of the GDDR3 Graphics RAM immediately prior to clock edge n.*
3. *COMMAND is the command registered at clock edge n, and ACTION is a result of COMMAND.*
4. *All states and sequences not shown are illegal or reserved.*
5. *DESEL or NOP commands should be issued on any clock edges occurring during the t_{XSR} period. A minimum of 1000 clock cycles is required before applying any other valid command.*

3 Functional Description

3.1 Mode Register Set Command (MRS)

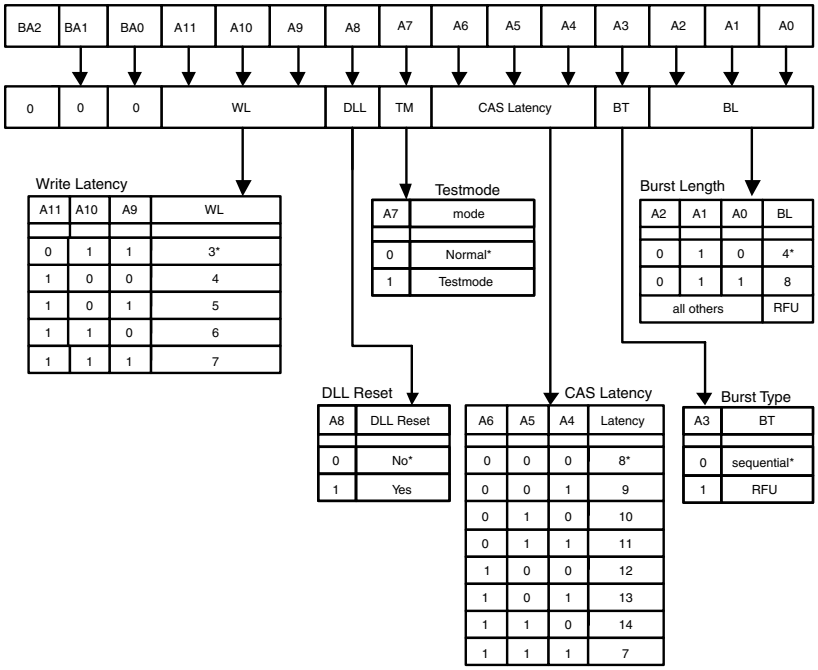
FIGURE 2
Mode Register Set Command



The Mode Register stores the data for controlling the operation modes of the memory. It programs CAS latency, test mode, DLL Reset , the value of the Write Latency and the Burst length. The Mode Register must be written after power up to operate the SGRAM. During a ModeRegister Set command the address inputs are sampled and stored in the Mode Register. The Mode Register content can only be set or changed when the chip is in Idle state. For non-READ commands following a Mode Register Set a delay of t_{MRD} must be met.

The Mode Register Bitmap is supported in two configurations. The first configuration is intended to support the Mid-Range-Speed application. The second configuration supports higher clock cycles for CAS latency and is therefore prepared to support high-speed application. The selected configuration is defined by Bit0 of EMRS2.

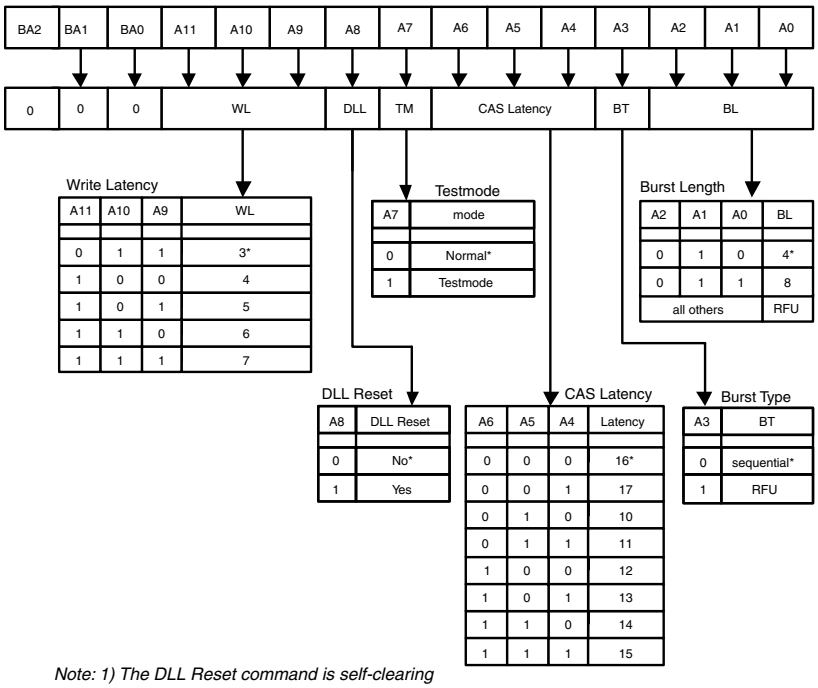
FIGURE 3
Mode Register Bitmap for Mid-Range-Speed Application



Note: 1) The DLL Reset command is self-clearing

** Defaults Settings*

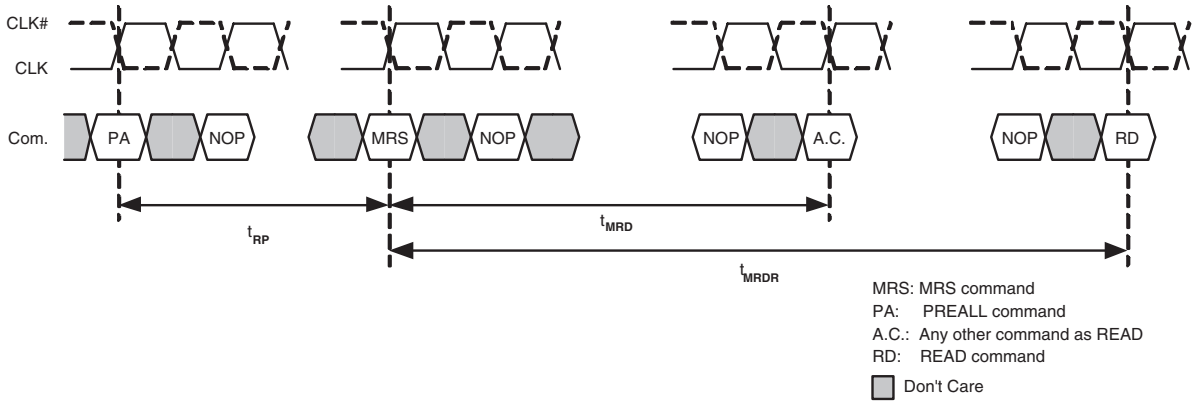
FIGURE 4
Mode Register Bitmap for High-Speed Application



Note: 1) The DLL Reset command is self-clearing

** Defaults Settings*

FIGURE 5
Mode Register Set Timing



3.1.1 Burst length

Read and Write accesses to the GDDR3 Graphics RAM are burst oriented with burst length of 4 and 8. This value must be programmed using the Mode Register Set command (A0 .. A2). The burst length determines the number of column locations that can be accessed for a given READ or WRITE command.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block if a boundary is reached. The starting location within this block is determined by the two least significant bits A0 and A1 which are set internally to the fixed value of zero each.Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

3.1.2 Burst type

Accesses within a given bank must be programmed to be sequential. This is done using the Mode Register Set command (A3). This device does not support the burst interleave mode.

TABLE 6
Burst Definition

Burst Length	Starting Column Address			Order of Accesses within a Burst (Type = sequential)
	A2	A1	A0	
4	—	X	X	0-1-2-3
8	0	X	X	0-1-2-3-4-5-6-7
	1	X	X	4-5-6-7-0-1-2-3

The value applied at the balls A0 and A1 for the column address is “Don’t care”.

3.1.3 CAS Latency

The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data.

If a READ command is registered at clock edge n, and the latency is m clocks, the data will be available nominally coincident with clock edge n+m.

The two Mode Register setups support different CAS Latencies in terms of clock cycles. The mid-range-speed Mode Register supports latencies from 7 to 14. The high-speed Mode Register supports latencies from 10 to 17. The active Mode Register setup is selected by Bit0 of EMRS2.

3.1.4 Write Latency

The WRITE latency, WL, is the delay, in clock cycles, between the registration of a WRITE command and the availability of the first bit of input data.

TABLE 7
ON/OFF mode of DQ/DM receivers

WL	DQ/DM-Receivers
3-4	Receivers are always on
5-6-7	Receivers are off and will be switched on by Write command and will be switched off again after WL+BL

The ON/OFF state of the DQ/DM receivers depends on the Write Latency. The dependence is given in **Table 7**.

3.1.5 Test mode

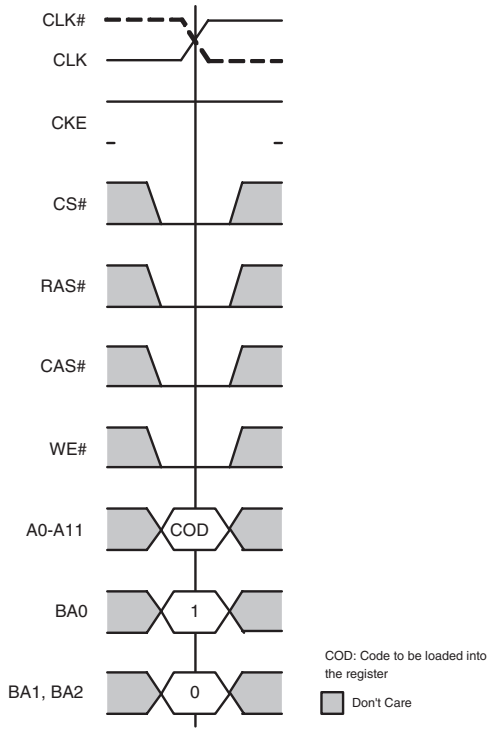
The normal operating mode is selected by issuing a Mode Register Set command with bit A7 set to zero and bits A0-A6 and A8-A11 set to the desired value.

3.1.6 DLL Reset

The normal operating mode is selected by issuing a Mode Register Set command with bit A8 set to zero and bits A0-A7 and A9-A11 set to the desired values. A DLL Reset is initiated by issuing a Mode Register Set command with bit A8 set to one and bits A0-A7 and A9-A11 set to the desired values. The GDDR3 Graphics RAM returns automatically in the normal mode of operations once the DLL reset is completed.

3.2 Extended Mode Register Set Command (EMRS1)

FIGURE 6
Extended Mode Register Set Command



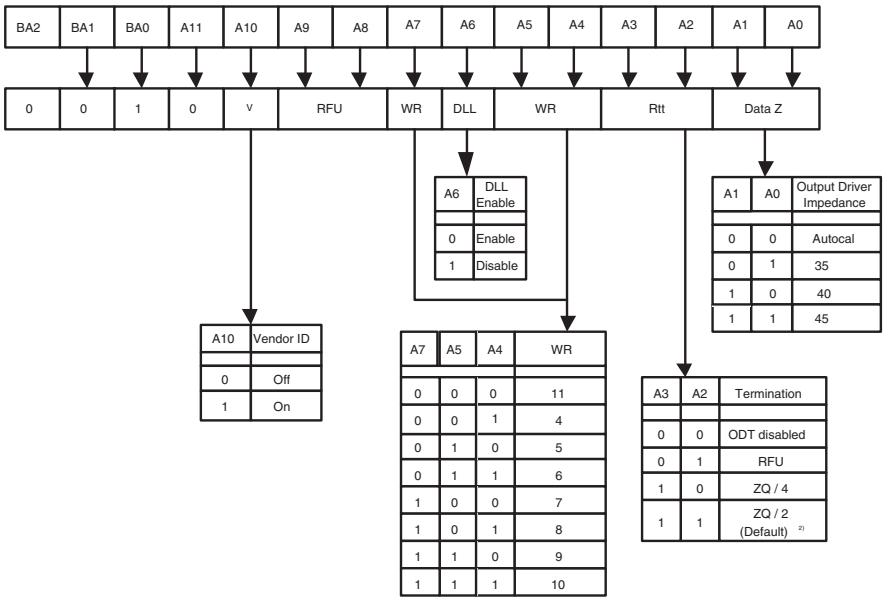
The Extended Mode Register is used to set the output driver impedance value, the termination impedance value, the Write Recovery time value for Write with Autoprecharge. It is used as well to enable/disable the DLL, to issue the Vendor ID and to enable/disable the Low Power mode. There is no default value for the Extended Mode Register. Therefore it must be written after power up to operate the GDDR3 Graphics RAM.

The Extended Mode Register can be programmed by performing a normal Mode Register Set operation and setting the BA0 bit to HIGH and BA1,BA2 bits to LOW. All other bits of the EMR register are reserved and should be set to LOW.

The Extended Mode Register must be loaded when all banks are idle and no burst are in progress. The controller must wait the specified time t_{MRD} before initiating any subsequent operation (**Figure 9**).

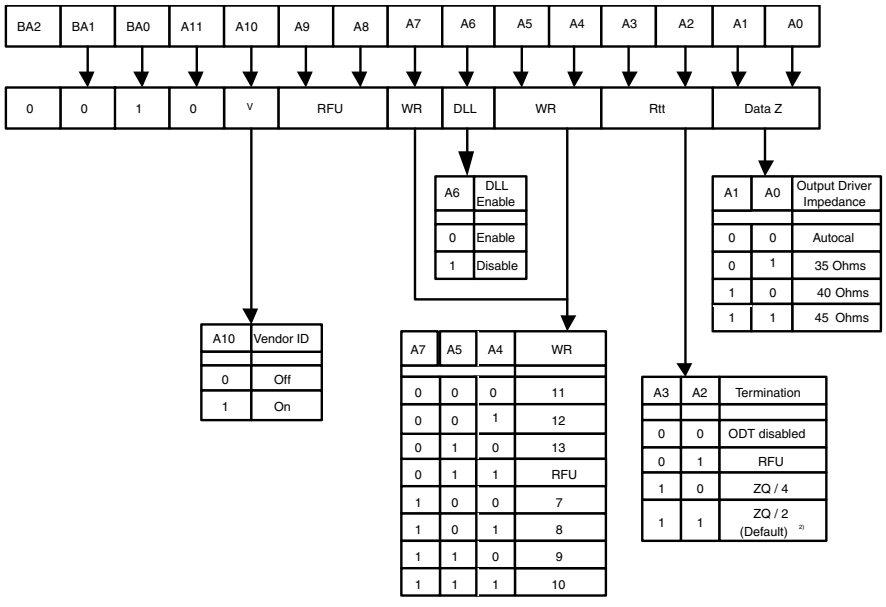
The timing of the EMRS command operation is equivalent to the timing of the MRS command operation.

FIGURE 7
Extended Mode Register Bitmap for Mid-Range-Speed Application



There are two bitmaps for the Extended Mode Register. One bitmap shown in **Figure 7** is supposed to support Mid-Speed applications. The other bitmap shown in **Figure 8** is more focused on the high-range-speed application. Both bitmaps distinguish different numbers in supported Write Recovery clock cycles. The mid-range bit map provides WR cycles from 4 to 11.The high-speed bitmap supports WR from 7 to 13.

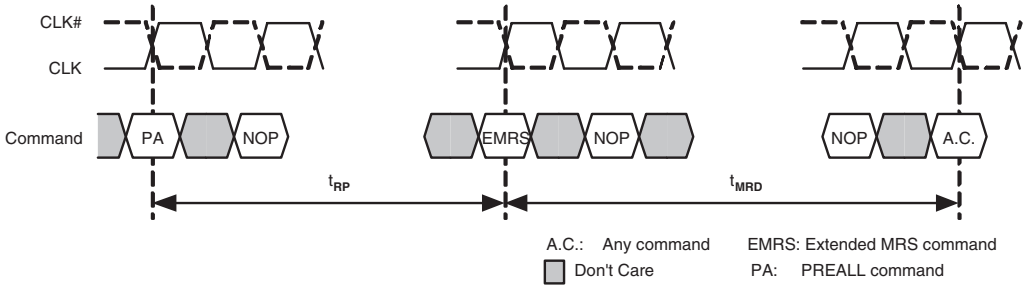
FIGURE 8
Extended Mode Register Bitmap for High-Speed Application



Notes

1. *These settings are for debugging purposes only.*
2. *Default termination values at Power Up.*
3. *The ODT disable function disables all terminators on the device.*
4. *If the user activates bits in the extended mode register in an optional field, either the optional field is activated (if option implemented in the device) or no action is taken by the device (if option not implemented).*
5. *WR (write recovery time for auto precharge) in clock cycles is calculated by dividing t_{WR} (in ns) and rounding up to the next integer (WR[cycles] = t_{WR}[ns] / t_{CK}[ns]). The mode register must be programmed to this value.*

FIGURE 9
Extended Mode Register Set Timing



3.2.1 DLL enable

The DLL must be enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation after having disabled the DLL. (When the device exits self-refresh mode, the DLL is enabled automatically). Anytime the DLL is enabled, 1000 cycles must occur before a READ command can be issued.

3.2.2 WR

The WR parameter is programmed using the register bits A4, A5 and A7. This integer parameter defines as a number of clock cycles the Write Recovery time in a Write with Autoprecharge operation.

The following inequality has to be complied with: WR * $t_{CK} \geq t_{WR}$, where t_{CK} is the clock cycle time. The high-speed bitmap supports WR from 7 to 13. The mid-range bitmap provides WR cycles from 4 to 11.

3.2.3 Termination Rtt

The data termination, Rtt, is used to set the value of the internal termination resistors. The GDDR3 DRAM supports ZQ / 4 and ZQ / 2 termination values. The termination may also be disabled for testing and other purposes.

3.2.4 Output Driver Impedance

The Output Driver Impedance extended mode register is used to set the value of the data output driver impedance. When the auto calibration is used, the output driver impedance is set nominally to ZQ / 6.

If the Output Driver Impendance is changed to 30, 40 or 45 Ohms the user needs to issue 16 AREF commands separated by t_{RFC} consecutively to make the change effective. The user must be aware that the Command bus needs to be stable for a time of t_{KO} after each AREF.

3.2.5 Vendor Code and Revision Identification

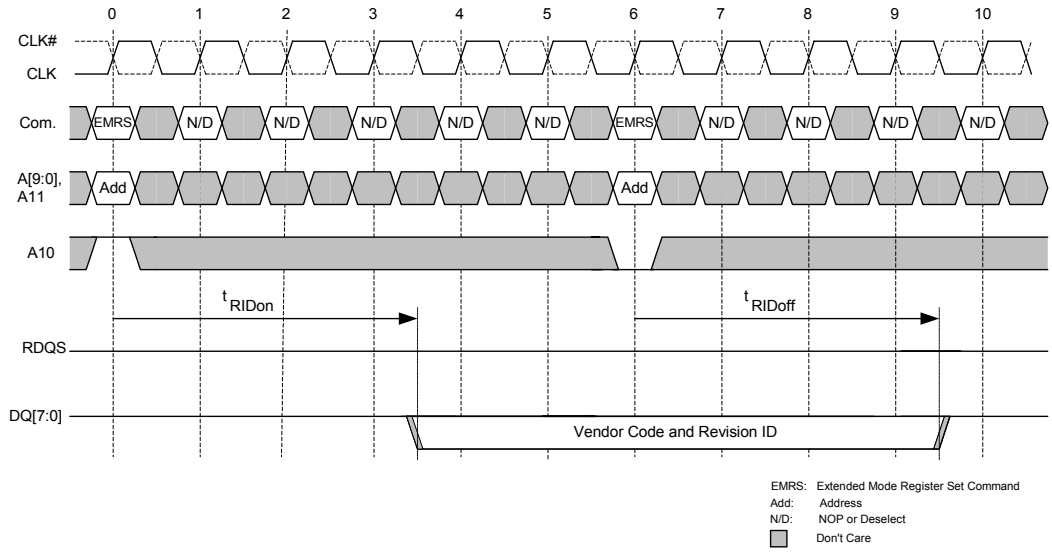
The Manufacturer Vendor Code is selected by issuing an Extended Mode Register Set command with bit A10 set to 1 and bits A0-A9 and A11 set to the desired value. When the Vendor Code function is enabled the GDDR3 DRAM will provide the Qimonda vendor code on DQ[3:0] and the revision identification on DQ[7:4]. The code will be driven onto the DQ bus after tRIDon following the EMRS command that sets A10 to 1. The Vendor Code and Revision ID will be driven on DQ[7:0] until a new EMRS command is issued with A10 set back to 0. After t_{RDoff} following the second EMRS command, the data bus is driven back to HIGH. This second EMRS command must be issued before initiating any subsequent operation. Violating this requirement will result in unspecified operation.

TABLE 8
Revision ID and Vendor Code

Revision Identification	Qimonda Vendor Code
DQ[7:4]	DQ[3:0]
0011	0010

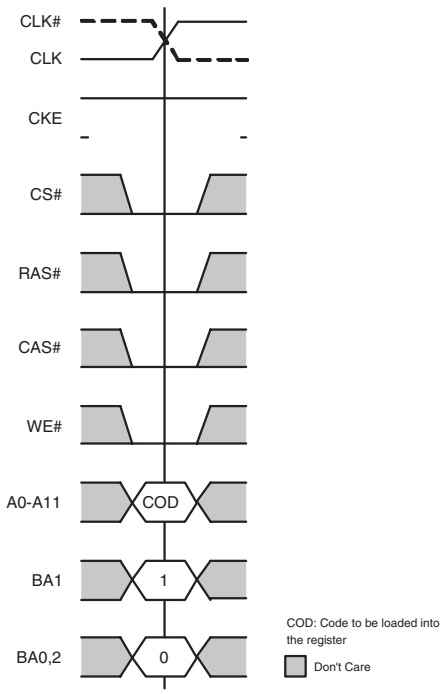
Note: Please refer to Revision Release Note for Revision ID value.

FIGURE 10
Timing of Vendor Code and Revision ID Generation on DQ[7:0]



3.3 Extended Mode Register 2 Set Command (EMRS2)

FIGURE 11
Extended Mode Register 2 Set Command

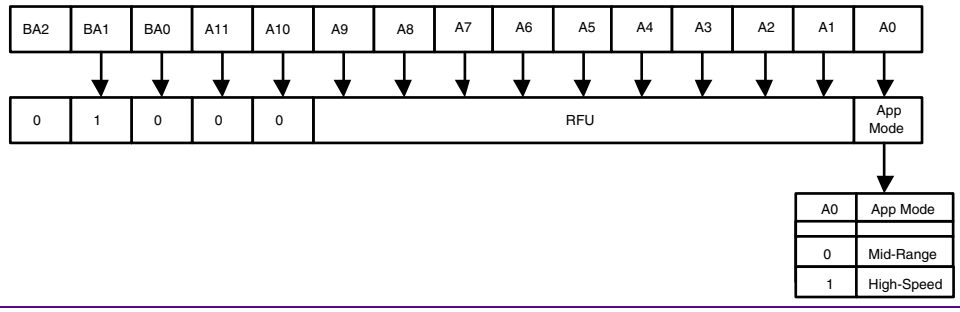


The Extended Mode Register 2 is used to define the active bitmap of the Mode Register and the Extended Mode Register.

The Extended Mode Register 2 must be written after power up to operate the GDDR3 Graphics RAM. It can be programmed by performing a normal Mode Register Set operation and setting the BA1 bit to HIGH and BA0, BA2 bits to LOW. All bits defined as RFU in the bitmap are reserved and must be set to LOW.

The Extended Mode Register 2 must be loaded when all banks are idle and no burst are in progress. The controller must wait the specified time t_{MRD} before initiating any subsequent operation. The timing of the EMRS2 command operation is equivalent to the timing of the MRS command operation.

FIGURE 12
Extended Mode Register 2 Bitmap



3.3.1 App Mode

The GDDR3 Graphics RAM provides two bitmaps for the Mode Register and the Extended Mode Register respectively. The Bitmaps are shown in the MRS and EMRS chapters.

The Bit0 of the Extended Mode Regsiter 2 defines which one of the two bitmaps is active. Bit0 set to LOW enables the mid-range bitmap and Bit0 set to HIGH enables the High-Speed bitmap.

4 Electrical Characteristics

4.1 Absolute Maximum Ratings and Operation Conditions

TABLE 9
Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit
		Min.	Max.	
Power Supply Voltage	V_{DD}	-0.5	2.5	V
Power Supply Voltage for Output Buffer	V_{DDQ}	-0.5	2.5	V
Input Voltage	V_{IN}	-0.5	2.5	V
Output Voltage	V_{OUT}	-0.5	2.5	V
Storage Temperature	T_{STG}	-55	+150	°C
Junction Temperature	T_J	—	+125	°C
Short Circuit Output Current	I_{OUT}	—	50	mA

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

4.2 DC Operation Conditions

4.2.1 Recommended Power & DC Operation Conditions

TABLE 10
Power & DC Operation Conditions (0 °C ≤ T_c ≤ 85 °C)

Parameter	Symbol	Limit Values			Unit	Note
		Min.	Typ.	Max.		
Power Supply Voltage	V_{DD}, V_{DDA}	1.9	2.0	2.1	V	1)2)
Power Supply Voltage for I/O Buffer	V_{DDQ}	1.9	2.0	2.1	V	1)2)

Parameter	Symbol	Limit Values			Unit	Note
		Min.	Typ.	Max.		
Power Supply Voltage	V_{DD}, V_{DDA}	1.7	1.8	1.9	V	1)3)
Power Supply Voltage for I/O Buffer	V_{DDQ}	1.7	1.8	1.9	V	1)3)
Reference Voltage	V_{REF}	0.69*V_{DDQ}	—	0.71*V_{DDQ}	V	4)
Output Low Voltage	$V_{OL(DC)}$	—	—	0.8	V	
Input leakage current	I_{IL}	–5.0	—	+5.0	µA	5)
CLK Input leakage current	I_{ILC}	–5.0	—	+5.0	µA	
Output leakage current	I_{OL}	–5.0	—	+5.0	µA	5)

1) V_{DDQ} tracks with V_{DD}. AC parameters are measured with V_{DD} and V_{DDQ} tied together.
2) HYB18H512321BF–08/10
3) HYB18H512321BF–11/12/14
4) V_{REF} is expected to equal 70% of V_{DDQ} for the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed ±2% V_{REF} (DC). Thus, from 70% of V_{DDQ}, V_{REF} is allowed ± 19mV for DC error and an additional ± 27mV for AC noise.
5) I_{IL} and I_{OL} are measured with ODT disabled.

4.3 DC & AC Logic Input Levels

TABLE 11
DC & AC Logic Input Levels (0 °C ≤ T_c ≤ 85 °C)

Parameter	Symbol	Limit Values		Unit	Note
		Min.	Max.		
Input logic high voltage, DC	V_{IH}(DC)	V_{REF} + 0.15	—	V	1)
Input logic low voltage, DC	V_{IL}(DC)	—	V_{REF} -0.15	V	1)
Input logic high voltage, AC	V_{IH}(AC)	V_{REF} + 0.25	—	V	2)3)
Input logic low voltage, AC	V_{IL}(AC)	—	V_{REF} - 0.25	V	2)3)
Input logic high, DC, RESET pin	V_{IHR}(DC)	0.65 × V_{DDQ}	V_{DDQ} + 0.3	V	
Input logic low, DC, RESET pin	V_{ILR}(DC)	-0.3	0.35 × V_{DDQ}	V	
Input Logic High, DC, MF pin	V_{IHMF}(DC)	V_{DD}	V_{DD} + 0.3	V	4)
Input Logic Low,DC, MF pin	V_{ILMF}(DC)	–0.3	0	V	

1) The DC values define where the input slew rate requirements are imposed, and the input signal must not violate these levels in order to maintain a valid level.
2) Input slew rate = 3 V/ns. If the input slew rate is less than 3 V/ns, input timing may be compromised. All slew rates are measured between V_{IL}(DC) and V_{IH}(DC).
3) V_{IH} overshoot: V_{IH}(max) = V_{DDQ}+0.5V for a pulse width ≤ 500ps and the pulse width cannot be greater than 1/3 of the cycle rate. V_{IL} undershoot: V_{IL}(min) = 0 V for a pulse width ≤ 500ps and the pulse width cannot be greater than 1/3 of the cycle rate.
4) The MF pin must be hard-wired on board to either V_{DD} or V_{SS}.

4.4 Differential Clock DC and AC Levels

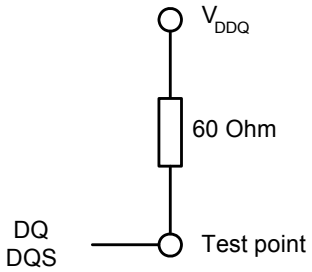
TABLE 12
Differential Clock DC and AC Input conditions (0 °C ≤ T_c ≤ 85 °C)

Parameter	Symbol	Limit Values		Unit	Note
		Min.	Max.		
Clock Input Mid-Point Voltage, CLK and $\overline{CLK}$	$V_{MP(DC)}$	0.7 × V_{DDQ} – 0.10	0.7 × V_{DDQ} + 0.10	V	1)
Clock Input Voltage Level, CLK and $\overline{CLK}$	$V_{IN(DC)}$	0.42	V_{DDQ} + 0.3	V	1)
Clock DC Input Differential Voltage, CLK and $\overline{CLK}$	$V_{ID(DC)}$	0.3	V_{DDQ}	V	1)
Clock AC Input Differential Voltage, CLK and $\overline{CLK}$	$V_{ID(AC)}$	0.5	V_{DDQ} + 0.5	V	1)2)
AC Differential Crossing Point Input Voltage	$V_{IX(AC)}$	0.7 × V_{DDQ} – 0.15	0.7 × V_{DDQ} + 0.15	V	1)3)

1) All voltages referenced to V_{SS}.
2) V_{ID} is the magnitude of the difference between the input level on CLK and the input level on $\overline{CLK}$.
3) The value of V_{IX} is expected to equal 0.7 × V_{DDQ} of the transmitting device and must track variations in the DC level of the same.

4.5 Output Test Conditions

FIGURE 13
Output Test Circuit



4.6 Pin Capacitances

TABLE 13
Pin Capacitances (VDDQ = 1.8 V, TA = 25°C, f = 1 MHz)

Parameter	Symbol	Min.	Max.	Unit	Note
Input capacitance: A0-A11, , BA0-2, CKE, $\overline{CS}$, $\overline{CAS}$, $\overline{RAS}$, $\overline{WE}$, CKE, RES,CLK,CLK	CI,CCK	1.0	2.5	pF	
Input capacitance: DQ0-DQ31, RDQS0-RDQS3, WDQS0-WDQS3, DM0-DM3	CIO	2.0	3.0	pF	

4.7 Driver current characteristics

4.7.1 Driver IV characteristics at 40 Ohms

Figure 14 represents the driver Pull-Down and Pull-Up IV characteristics under process, voltage and temperature best and worst case conditions. The actual Driver Pull-Down and Pull-Up current must lie between these two bounding curves. The value of the external ZQ resistor is 240 Ω, setting the nominal driver output impedance to 40 Ω.

FIGURE 14
40 Ohm Driver Pull-Down and Pull-Up Characteristics

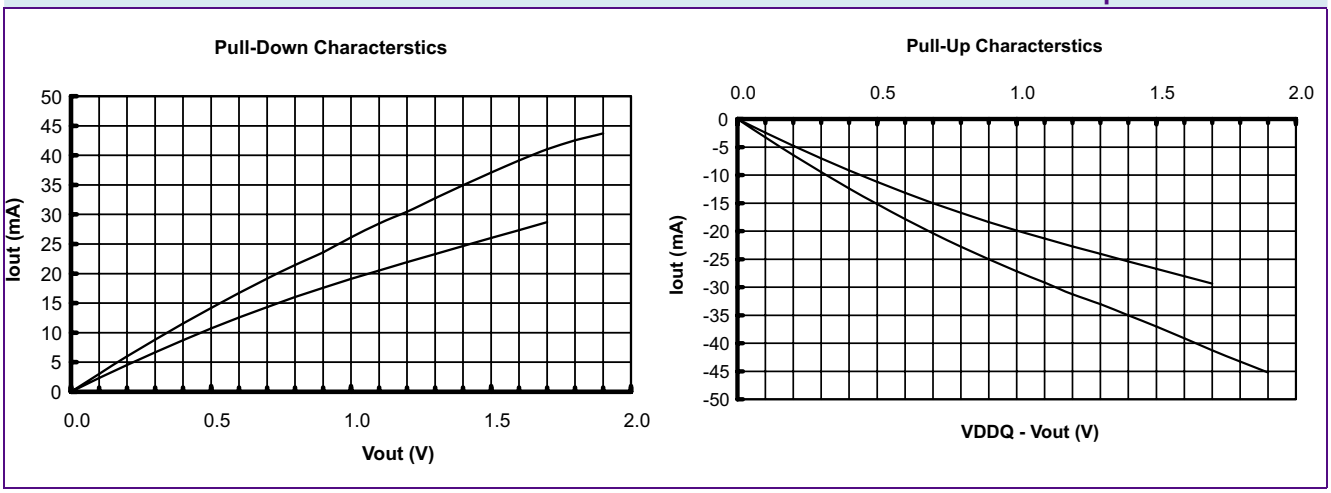


Table 14 lists the numerical values of the minimum and maximum allowed values of the output driver Pull-Down and Pull-Up IV characteristics.

TABLE 14
Programmed Driver IV Characteristics at 40 Ohm

Voltage (V)	Pull-Down Current (mA)		Pull-Up Current (mA)	
	Minimum	Maximum	Minimum	Maximum
0.1	2.32	3.04	-2.44	-3.27
0.2	4.56	5.98	-4.79	-6.42
0.3	6.69	8.82	-7.03	-9.45
0.4	8.74	11.56	-9.18	-12.37
0.5	10.70	14.19	-11.23	-15.17
0.6	12.56	16.72	-13.17	-17.83
0.7	14.34	19.14	-15.01	-20.37
0.8	16.01	21.44	-16.74	-22.78
0.9	17.61	23.61	-18.37	-25.04
1.0	19.11	26.10	-19.90	-27.17
1.1	20.53	28.45	.21.34	-29.17
1.2	21.92	30.45	-22.72	-31.25
1.3	23.29	32.73	-24.07	-33.00
1.4	24.65	34.95	-25.40	-35.00
1.5	26.00	37.10	-26.73	-37.00
1.6	27.35	39.15	-28.06	-39.14
1.7	28.70	41.01	-29.37	-41.25
1.8	30.08	42.53	-30.66	-43.29
1.9	—	43.71	—	-45.23
2.0	—	44.89	—	-47.07

4.7.2 Termination IV Characteristic at 60 Ohms

Figure 15 represents the DQ termination Pull-Up IV characteristic under process, voltage and temperature best and worst case conditions. The actual DQ termination Pull-Up current must lie between these two bounding curves. The value of the external ZQ resistor is 240 Ω, setting the nominal DQ termination impedance to 60 Ω. (Extended Mode Register programmed to ZQ/4).

FIGURE 15
60 Ohm Active Termination Characteristic

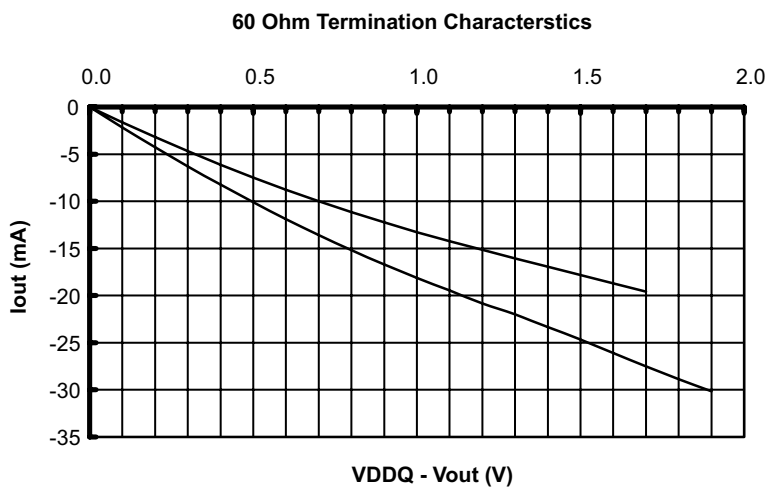


Table 15 lists the numerical values of the minimum and maximum allowed values of the output driver termination IV characteristic.

TABLE 15
Programmed Terminator Characteristics at 60 Ohm

Voltage (V)	Terminator Pull-Up Current (mA)			Voltage (V)	Terminator Pull-Up Current (mA)	
	Minimum	Maximum			Minimum	Maximum
0.1	-1.63	-2.18		1.1	-14.23	-19.45
0.2	-3.19	-4.28		1.2	-15.14	-20.83
0.3	-4.69	-6.30		1.3	-16.04	-22.00
0.4	-6.12	-8.25		1.4	-16.94	-23.33
0.5	-7.49	-10.11		1.5	-17.82	-24.67
0.6	-8.78	-11.89		1.6	-18.70	-26.09
0.7	-10.01	-13.58		1.7	-19.58	-27.50
0.8	-11.16	-15.19		1.8	-20.44	-28.86
0.9	-12.25	-16.69		1.9	—	-30.15
1.0	-13.27	-18.11		2.0	—	-31.38

4.8 Termination IV Characteristic at 120 Ohms

Figure 16 represents the DQ or ADD/CMD termination Pull-Up IV characteristic under process, voltage and temperature best and worst case conditions. The actual termination Pull-Up current must lie between these two bounding curves. The value of the external ZQ resistor is 240 Ω, setting the nominal termination impedance to 120 Ω. (Extended Mode Register programmed to ZQ/2 for DQ terminations or CKE = 0 at the RES transition during Power-Up for ADD/CMD terminations).

FIGURE 16
120 Ohm Active Termination Characteristic

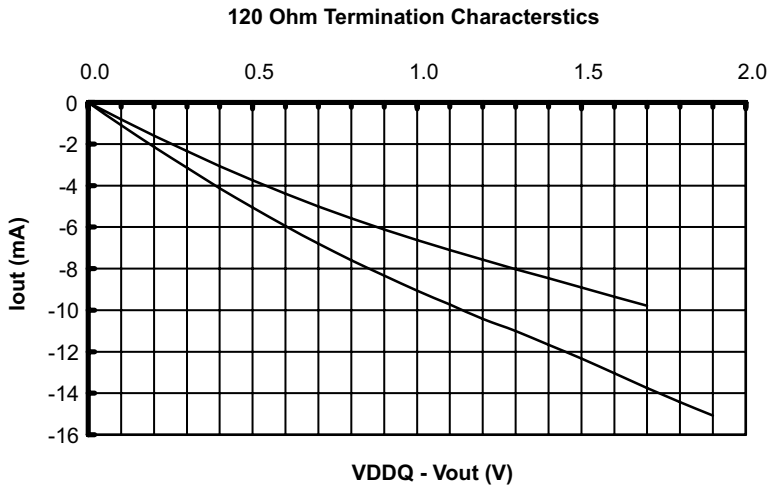


Table 16 lists the numerical values of the minimum and maximum allowed values of the termination IV characteristic.

TABLE 16
Programmed Terminator Characteristics of 120 Ohm

Voltage (V)	Terminator Pull-Up Current (mA)			Voltage (V)	Terminator Pull-Up Current (mA)	
	Minimum	Maximum			Minimum	Maximum
0.1	-0.81	-1.09		1.1	-7.11	-9.72
0.2	-1.60	-2.14		1.2	-7.57	-10.42
0.3	-2.34	-3.15		1.3	-8.02	-11.00
0.4	-3.06	-4.12		1.4	-8.47	-11.67
0.5	-3.74	-5.06		1.5	-8.91	-12.33
0.6	-4.39	-5.94		1.6	-9.35	-13.05
0.7	-5.00	-6.79		1.7	-9.79	-13.75
0.8	-5.58	-7.59		1.8	-10.22	-14.43
0.9	-6.12	-8.35		1.9	—	-15.08
1.0	-6.63	-9.06		2.0	—	-15.69

4.9 Termination IV Characteristic at 240 Ohms

Figure 17 represents the ADD/CMD termination Pull-Up IV characteristic under process, voltage and temperature best and worst case conditions. The actual ADD/CMD termination Pull-Up current must lie between these two bounding curves. The value of the external ZQ resistor is 240 Ω, setting the nominal termination impedance to 240 Ω. (CKE = 1at the RES transition during Power-Up for ADD/CMD terminations).

FIGURE 17
240 Ohm Active Termination Characteristic

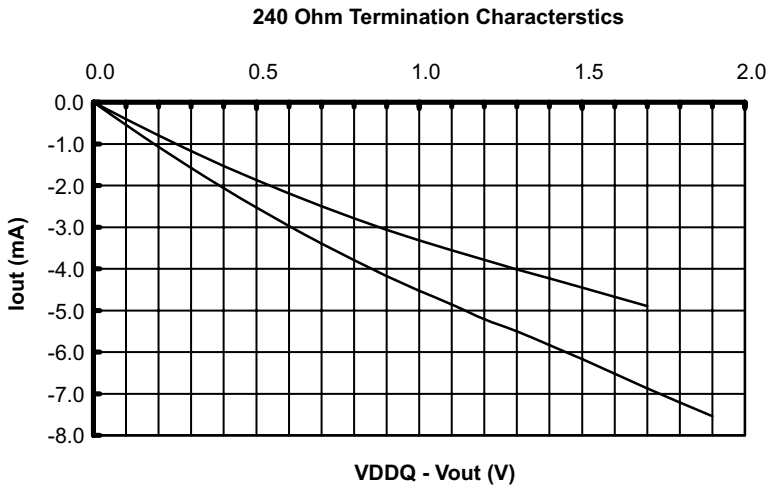


Table 17 lists the numerical values of the minimum and maximum allowed values of the ADD/CMD termination IV characteristic.

TABLE 17
Programmed Terminator Characteristics at 240 Ohm

Voltage (V)	Terminator Pull-Up Current (mA)			Voltage (V)	Terminator Pull-Up Current (mA)	
	Minimum	Maximum			Minimum	Maximum
0.1	-0.41	-0.55		1.1	-3.56	-4.86
0.2	-0.80	-1.07		1.2	-3.79	-5.21
0.3	-1.17	-1.58		1.3	-4.01	-5.50
0.4	-1.53	-2.06		1.4	-4.23	-5.83
0.5	-1.87	-2.53		1.5	-4.46	-6.17
0.6	-2.20	-2.97		1.6	-4.68	-6.52
0.7	-2.50	-3.40		1.7	-4.90	-6.88
0.8	-2.79	-3.80		1.8	-5.11	-7.21
0.9	-3.06	-4.17		1.9	—	-7.54
1.0	-3.32	-4.53		2.0	—	-7.85

4.10 Operating Currents

4.10.1 Operating Current Ratings for HYB18H512321BF

TABLE 18
Operating Current Ratings (0 °C ≤ T_c ≤ 85 °C)

Parameter	Symbol	Values					Unit	Note
		-8	–10	–11	–12	–14		
		Typ	Typ.	Typ.	Typ.	Typ.		
Operating Current	I_{DD0}	630	580	535	500	435	mA	1)2)3)
Operating Current	I_{DD1}	705	650	600	540	415	mA	1)2)3)
Precharge Power-Down Standby Current	I_{DD2P}	415	380	350	315	235	mA	1)2)3)
Precharge Floating Standby Current	I_{DD2F}	470	440	410	380	310	mA	1)2)3)
Precharge Quiet Standby Current	I_{DD2Q}	505	450	400	350	275	mA	1)2)3)
Active Power-Down Standy Current	I_{DD3P}	410	380	350	320	235	mA	1)2)3)
Active Standby Current	I_{DD3N}	585	540	500	460	395	mA	1)2)3)
Operating Current Burst Read	I_{DD4R}	885	810	740	670	575	mA	1)2)3)
Operating Current Burst Write	I_{DD4W}	890	800	720	660	565	mA	1)2)3)
Auto-Refresh Current (t_{RC}=min(t_{RFC}))	I_{DD5B}	740	700	660	620	535	mA	1)2)3)
Auto-Refresh Current at t_{REFI}	I_{DD5D}	520	475	435	400	350	mA	1)2)3)
Self Refresh Current	I_{DD6}	8	8	8	8	8	mA	1)2)3)4)
Operating Current	I_{DD7}	920	860	800	740	680	mA	1)2)3)

1) IDD specifications are tested after the device is properly initialized.
2) Input slew rate = 3 V/ns.
3) Measured with Output open and On Die termination off.
4) Enables on-chip refresh and address counter.

4.11 Operating Current Measurement Conditions

TABLE 19
Operating Current Measurement Conditions

Symbol	Parameter/Condition
I_{DD0}	Operating Current - One bank, Activate - Precharge t_{CK}=min(t_{CK}), t_{RC}=min(t_{RC}) Databus inputs are SWITCHING; Address and control inputs are SWITCHING, $\overline{CS}$ = HIGH between valid commands.
I_{DD1}	Operating Current - One bank, Activate - Read - Precharge One bank is accessed with t_{CK}=min(t_{CK}), t_{RC}=min(t_{RC}), CL = CL(min), Address and control inputs are SWITCHING; $\overline{CS}$ = HIGH between valid commands. I_{out}=0 mA
I_{DD2P}	Precharge Power-Down Standby Current All banks idle, power-down mode, CKE is LOW, t_{CK}=min(t_{CK}), Data bus inputs are STABLE (HIGH).
I_{DD2F}	Precharge Floating Standby Current All banks idle; $\overline{CS}$ is HIGH, CKE is HIGH, t_{CK}=min(t_{CK}); Address and control inputs are SWITCHING; Data bus input are STABLE (HIGH).
I_{DD2Q}	Precharge Quiet Standby Current $\overline{CS}$ is HIGH, all banks idle, CKE is HIGH, t_{CK}=min(t_{CK}), Address and other control inputs STABLE (HIGH), Data bus inputs are STABLE (HIGH).
I_{DD3P}	Active Power-Down Standby Current One bank active, CKE is LOW, Address and control inputs are STABLE (HIGH); Data bus inputs are STABLE (HIGH); standard active power-down mode.
I_{DD3N}	Active Standby Current One bank active, $\overline{CS}$ is HIGH, CKE is HIGH, t_{RAS}= $t_{RAS,max}$, t_{CK}=min(t_{CK}); Address and control inputs are SWITCHING; Data bus inputs are SWITCHING.
I_{DD4R}	Operating Current - Burst Read One bank active; Continuous read bursts, CL = CL(min); t_{CK}=min(t_{CK}); t_{RAS}= $t_{RAS,max}$; Address and control inputs are SWITCHING; Iout = 0 mA.
I_{DD4W}	Operating Current - Burst Write One bank active; Continuous write bursts; t_{CK}=min(t_{CK}); Address and control inputs are SWITCHING; Data bus inputs are SWITCHING.
I_{DD5B}	Burst Auto Refresh Current Refresh command at t_{RFC}=min(t_{RFC}); t_{CK}=min(t_{CK}); CKE is HIGH, $\overline{CS}$ is HIGH between all valid commands; Other command and address inputs are SWITCHING; Data bus inputs are SWITCHING.
I_{DD5D}	Distributed Auto Refresh Current t_{CK}=t_{CKmin}; Refresh command every t_{REFI}; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other command and address inputs are SWITCHING; Data bus inputs are SWITCHING.
I_{DD6}	Self Refresh Current CKE ≤ max(V_{IL}), external clock off, CK and $\overline{CK}$ LOW; Address and control inputs are STABLE (HIGH); Data Bus inputs are STABLE (HIGH).
I_{DD7}	Operating Bank Interleave Read Current All banks interleaving with CL = CL(min); t_{RCD} = t_{RCDRD}(min); t_{RRD} = t_{RRD}(min); I_{out}=0 mA; Address and control inputs are STABLE (HIGH) during DESELECT; Data bus inputs are SWITCHING.

Notes

1. *0 °C ≤ Tc ≤ 85 °C*
2. *Data Bus consists of DQ, DM, WDQS.*
3. *Definitions for IDD:*
   LOW is defined as VIN = 0.4 × VDDQ; HIGH is defined as V_{IN} = V_{DDQ};
   STABLE is defined as inputs are stable at a HIGH level.
   SWITCHING is defined as inputs are changing between HIGH and LOW every clock cycle for address and control signals, and inputs changing 50% of each data transfer for DQ signals.

4.12 AC Timings for HYB18H512321BF

TABLE 20
Timing Parameters for HYB18H512321BF

Parameter	CAS latency	Symbol	Limit Values										Unit	Note
			-8		–10		–11		–12		–14			
			Min	Max	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Clock and Clock Enable														
System frequency	CL=13	f_{CK13}	700	1200	—	—	—	—	—	—	—	—	MHz	1)
	CL= 12	f_{CK12}	500	1000	500	1000	—	—	—	—	—	—	MHz	1)
	CL= 11	f_{CK11}	400	900	400	900	400	900	400	800	400	700	MHz	1)
	CL =10	f_{CK10}	350	800	350	800	350	800	350	700	350	650	MHz	1)2)
	CL = 9	f_{CK9}	350	700	350	700	350	700	350	650	350	600	MHz	1)2)
	CL = 8	f_{CK8}	350	600	350	600	350	600	350	550	350	500	MHz	1)2)
	CL = 7	f_{CK7}	350	550	350	550	350	550	350	500	350	450	MHz	1)2)
Clock high level width		t_{CH}	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	
Clock low-level width		t_{CL}	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	
Minimum clock half period		t_{HP}	0.45	—	0.45	—	0.45	—	0.45	—	0.45	—	t_{CK}	3)
Command and Address Setup and Hold Timing														
Address/Command input setup time		t_{IS}	0.22	—	0.24	—	0.27	—	0.3	—	0.35	—	ns	
Address/Command input hold time		t_{IH}	0.22	—	0.24	—	0.27	—	0.3	—	0.35	—	ns	
Address/Command input pulse width		t_{IPW}	0.7	—	0.7	—	0.7	—	0.7	—	0.7	—	t_{CK}	
Mode Register Set Timing														
Mode Register Set cycle time		t_{MRD}	6	—	6	—	6	—	6	—	6	—	t_{CK}	4)5)
Mode Register Set to READ timing		t_{MRDR}	12	—	12	—	12	—	12	—	12	—	t_{CK}	
Row Timing														
Row Cycle Time		t_{RC}	40	—	37	—	35	—	34	—	30	—	t_{CK}	
Row Active Time		t_{RAS}	25	—	23	—	22	—	21	—	18	—	t_{CK}	6)
ACT(a) to ACT(b) Command period		t_{RRD}	10	—	9	—	8	—	8	—	7	—	t_{CK}	
Row Precharge Time		t_{RP}	15	—	14	—	13	—	13	—	12	—	t_{CK}	
Row to Column Delay Time for Reads		t_{RCDRD}	14	—	13	—	12	—	12	—	11	—	t_{CK}	
Row to Column Delay Time for Writes		t_{RCDWR}	$t_{RCDWR(Min)} = \max(t_{RCDRD(Min)} - (WL + 1) \times t_{CK}; 2 \times t_{CK})$										t_{CK}	7)
Four Active Windows within Rank		t_{FAW}	40	—	36	—	32	—	32	—	28	—	t_{CK}	

Parameter	CAS latency	Symbol	Limit Values										Unit	Note
			-8		–10		–11		–12		–14			
			Min	Max	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Column Timing														
CAS(a) to CAS(b) Command period		t_{CCD}	2	—	2	—	2	—	2	—	2	—	t_{CK}	8)
Internal write to Read Command Delay		t_{WTR}	8	—	7	—	6	—	6	—	5	—	t_{CK}	9)
Read to Write command delay		t_{RTW}	$t_{RTW(min)}$= (CL + BL/2 +2 -WL)										t_{CK}	10)
Write Cycle Timing Parameters for Data and Data Strobe														
Write command to first WDQS latching transition		t_{DQSS}	WL–0.25	WL+0.25	WL–0.25	WL+0.25	WL–0.25	WL+0.25	WL–0.25	WL+0.25	WL–0.25	WL+0.25	t_{CK}	
Data-in and Data Mask to WDQS Setup Time		t_{DS}	0.13	—	0.14	—	0.15	—	0.16	—	0.18	—	ns	
Data-in and Data Mask to WDQS Hold Time		t_{DH}	0.13	—	0.14	—	0.15	—	0.16	—	0.18	—	ns	
Data-in and DM input pulse width (each input)		t_{DIPW}	0.4	—	0.40	—	0.40	—	0.40	—	0.40	—	t_{CK}	
DQS input low pulse width		t_{DQSL}	0.45	—	0.40	—	0.40	—	0.40	—	0.40	—	t_{CK}	
DQS input high pulse width		t_{DQSH}	0.45	—	0.40	—	0.40	—	0.40	—	0.40	—	t_{CK}	
DQS Write Preamble Time		t_{WPRE}	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	t_{CK}	
DQS Write Postamble Time		t_{WPST}	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	t_{CK}	
Write Recovery Time		t_{WR}	13	—	13	—	13	—	12	—	10	—	t_{CK}	
Read Cycle Timing Parameters for Data and Data Strobe														
Data Access Time from Clock		t_{AC}	-0.20	-0.20	-0.21	0.21	-0.22	0.22	-0.22	0.22	–0.25	0.25	ns	
Read Preamble		t_{RPRE}	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	t_{CK}	
Read Postamble		t_{RPST}	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	t_{CK}	
Data-out high impedance time from CLK		t_{HZ}	t_{ACmin}	t_{ACmax}	t_{ACmin}	t_{ACmax}	t_{ACmin}	t_{ACmax}	t_{ACmin}	t_{ACmax}	t_{ACmin}	t_{ACmax}	ns	
Data-out low impedance time from CLK		t_{LZ}	t_{ACmin}	t_{ACmax}	t_{ACmin}	t_{ACmax}	t_{ACmin}	t_{ACmax}	t_{ACmin}	t_{ACmax}	t_{ACmin}	t_{ACmax}	ns	
DQS edge to Clock edge skew		t_{DQSCK}	-0.20	0.20	-0.21	0.21	-0.22	0.22	-0.22	0.22	–0.25	0.25	ns	
DQS edge to output data edge skew		t_{DQSQ}	—	0.110	—	0.120	—	0.130	—	0.140	—	0.160	ns	11)
Data hold skew factor		t_{QHS}	—	0.110	—	0.120	—	0.130	—	0.140	—	0.160	ns	
Data output hold time from DQS		t_{QH}	t_{HP}–t_{QHS}										ns	
Refresh/Power Down Timing														
Refresh Period (8192 cycles)		t_{REF}	—	32	—	32	—	32	—	32	—	32	ms	
Average periodic Auto Refresh interval		t_{REFI}	3.9		3.9		3.9		3.9		3.9		µs	

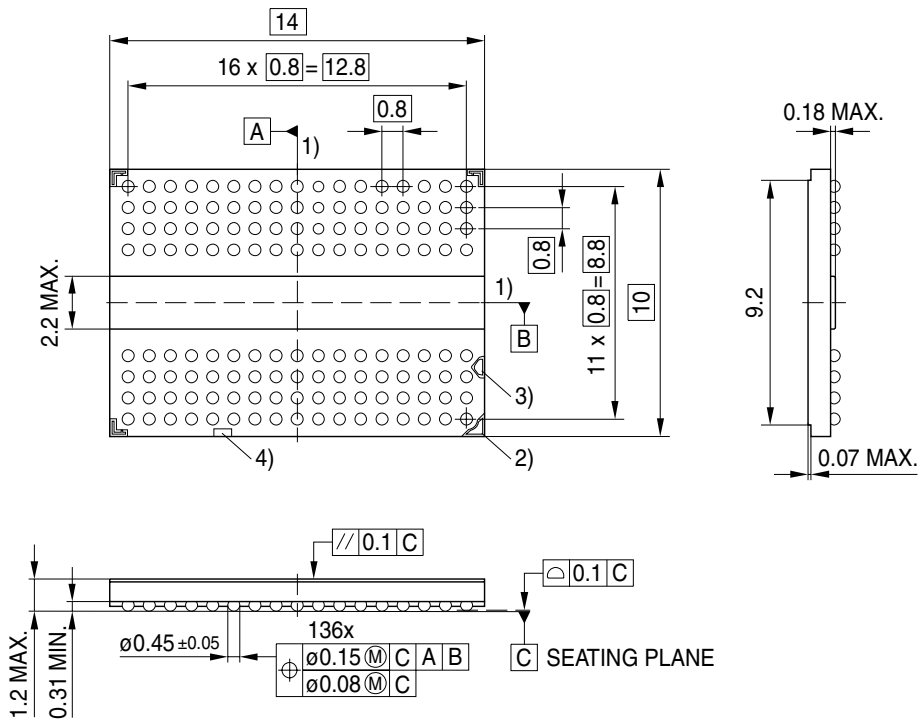
Parameter	CAS latency	Symbol	Limit Values										Unit	Note
			-8		–10		–11		–12		–14			
			Min	Max	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Delay from AREF to next ACT/ AREF		t_{RFC}	52.0	—	52.0	—	52.0	—	52.0	—	52.0	—	ns	
Self Refresh Exit time		t_{XSC}	1000	—	1000	—	1000	—	1000	—	1000	—	t_{CK}	
Self refresh exit followed by non-Read command		t_{XSNR}	200	—	200	—	200	—	200	—	200	—	t_{CK}	
Power Down Exit time		t_{XPN}	7	—	7	—	7	—	7	—	6	—	t_{CK}	
Other Timing Parameters														
RES to CKE setup timing		t_{ATS}	10	—	10	—	10	—	10	—	10	—	ns	
RES to CKE hold timing		t_{ATH}	10	—	10	—	10	—	10	—	10	—	ns	
Termination update Keep Out timing		t_{KO}	10	—	10	—	10	—	10	—	10	—	ns	
Rev. ID EMRS to DQ on timing		t_{RIDon}	—	20	—	20	—	20	—	20	—	20	ns	
Rev. ID EMRS to DQ off timing		t_{RIDoff}	—	20	—	20	—	20	—	20	—	20	ns	

1) f_{CK}(min), f_{CK}(max) for DLL on mode
2) f_{CK}(min) can go down to 200MHz, with t_{AC} and t_{DQSCK} shifted up to 1/2 t_{CK}
3) t_{HP} is the lesser of t_{CL} minimum and t_{CH} minimum actually applied to the device CLK, $\overline{CLK}$ inputs
4) This value of t_{MRD} applies only to the case where the “DLL reset” bit is not activated
5) t_{MRD} is defined from MRS to any other command then READ
6) t_{RASmax} is 8 × t_{REF}
7) $t_{RCDWR(Min)}$ may not drop below 2 × t_{CK}
8) t_{CCD} is either for gapless consecutive reads or gapless consecutive writes. BL =4
9) WTR and t_{WR} start at the first rising edge of CLK after the last valid (falling) WDQS edge of the slowest WDQS signal
10) Please round up t_{RTW} to the next integer of t_{CK}
11) This parameter is defined per byte

5 Package

5.1 Package Outline

FIGURE 18
Package Outline PG-TFBGA-136-054



1) Middle of packages edges
2) Package orientation mark A1
3) Bad unit marking (BUM)
4) SBA-Fiducial (Solder Ball Attach)

Lead free solder balls (Gren Solder Balls)

GPA01194

Note: The package is conforming with JEDEC MO-207i, VAR DR-z.

5.2 Package Thermal Characteristics

TABLE 21
PG-TFBGA-136 Package Thermal Resistances

	Theta_jA						Theta_jB	Theta_jC
JEDEC Board	1s0p			2s2p				
Air Flow	0 m/s	1 m/s	3 m/s	0 m/s	1 m/s	3 m/s	-	-
K/W	40	32	27	22	19	17	5	2

Notes

1. *Theta_jA: Junction to Ambient thermal resistance. The values have been obtained by simulation using the conditions stated in the JEDEC JESD-51 standard.*
2. *Theta_jB: Junction to Board thermal resistance. The value has been obtained by simulation.*
3. *Theta_jC: Junction to Case thermal resistance. The value has been obtained by simulation.*

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