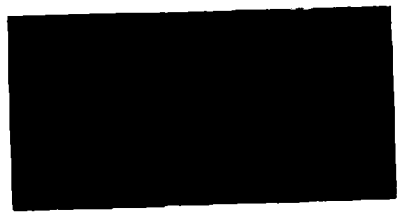
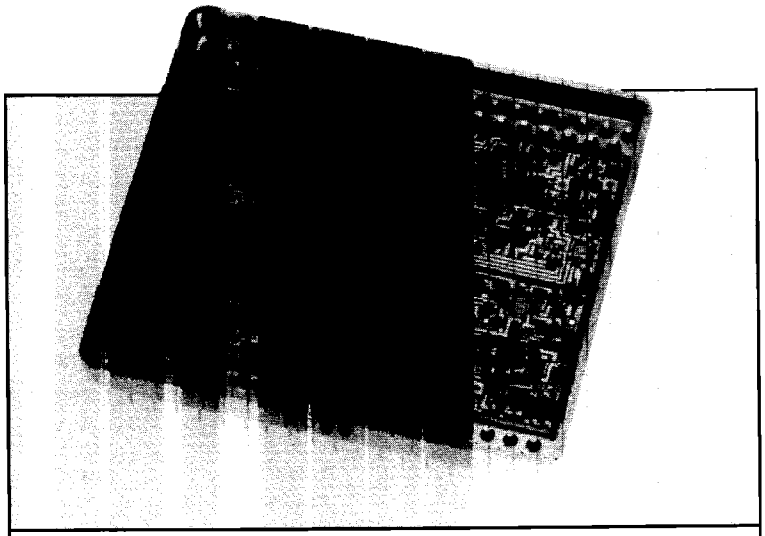
ARX-2452 AND ARX-2462
REMOTE TERMINAL UNIT
for MIL-STD-1553B

AEROFLEX
An ARX Company

Features

- **Complete dual redundant RTU in single package**
- **Dual low power transceivers**
- **Low power CMOS chip set**
- **Handles all mode codes for dual redundant operation**
- **Simple DMA data transfer to/from subsystem**
- **Continuous self test when transmitting**
- **Interchangeable with BUS 65112 and BUS 65113**
- **MIL-STD-883 screened**





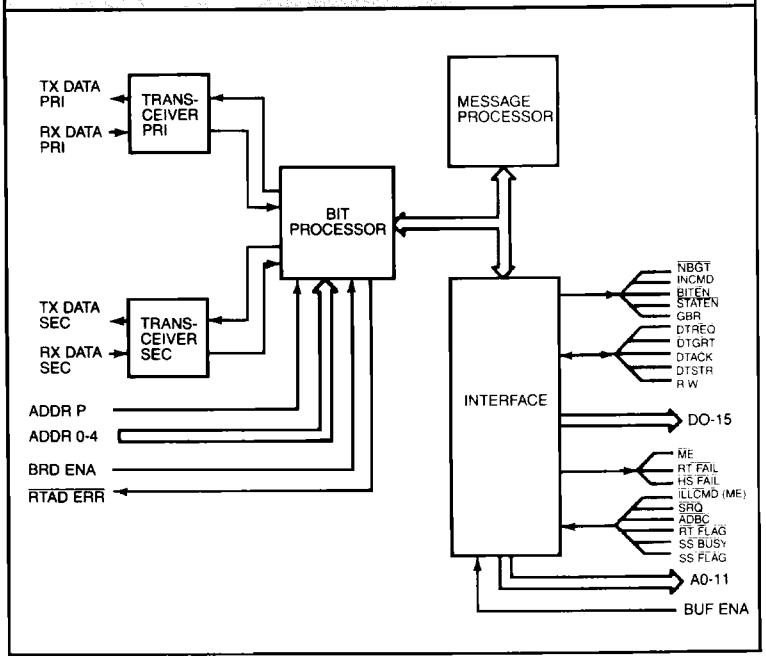


Figure 1: Block Diagram

Introduction

The Aeroflex Model ARX 2452 is a complete dual redundant Remote Terminal Unit in a single hybrid package. It satisfies all the protocol, timing and electrical requirements of MIL-STD-1553B for transmitting and receiving. Bidirectional subsystem interface is provided for simple direct memory access (DMA) data transfer and is double buffered to avoid data loss during transfer. The Built-In Test (BIT) word latches error information which can be furnished to the Bus Controller in response to the appropriate command.

The unit contains two low power transceivers, a bit processor chip which performs the encode and decode functions along with parallel/serial conversion and failsafe timeout, a message processor chip which controls all the protocol processing, and an interface chip which handles all data transfer to the subsystem. An Illegal Command input line permits an external PROM to be used to illegalize any command.

Transceivers

Transceivers are a second generation design which reflects particular attention to the electrical requirements of the MIL-STD 1553B. When connected to the appropriate transformers (see Figure 6 for connection and transformer information) the receiver will respond to data bus signals of 1.2 volts peak to peak and ignore signals below .6 volts peak to peak. Efficient transmitter electrical and thermal design keeps internal power dissipation to a minimum at any duty cycle.

Each channel of the dual transceivers is completely separate from the other and the digital section of the RTU and fully independent. This includes power leads as well as signal lines. Hence each channel may be connected to a different bus with no interaction between them.

Bit Processor

The Bit Processor is an application specific integrated circuit which contains two decoders, an encoder with channel select logic, command word detection, terminal address logic, failsafe timeout and clock dividers for the message processor and interface devices.

When operating in the transmit mode the encoder shifts parallel data from the message processor into serial, adds proper sync and parity and transfers it to the selected channel transceiver. In the receive mode the decoders perform sync detection, address decode of command words, examine for Manchester and parity errors and shift the serial data to parallel for protocol processing.

The failsafe timeout circuit detects transmissions in excess of approximately 768 microseconds and disables the encoder to inhibit further transmission.

The Bit Processor will establish the active channel for RT transmit based upon which channel a valid command word is received.

Message Processor

The Message Processor is an application specific integrated circuit which contains a protocol sequencer, internal word storage registers, wrap-around data verification logic and serves to control all RTU activities. Acting upon commands received from the bus controller it responds with receive, transmit or RT to RT transfers, as well as to mode commands and broadcast.

Error checking is performed on received and transmitted data. If an error is detected during a receive operation the MESSAGE ERROR ($\overline{ME}$) ouput is brought low, the corresponding bit of the Status Word is set and data transfer to the subsystem is inhibited. An error detected during transmission from continuous wrap-around self test or from activation of the failsafe timeout results in the REMOTE TERMINAL FAILURE ($\overline{RT\ FAIL}$) line being brought low and the Terminal Flag bit set in the Status Word.

Interface Chip

The Interface Control chip is an application specific integrated circuit which controls and monitors the DMA data transfers to and from the subsystem. It latches the received and transmitted data as well as status and BIT words.

RTU Operation

The INCMD line indicates the unit is processing a new command word. Contents of the command word, which are T/$\overline{R}$ bit, subaddress and word count/mode code are stored as latched outputs. Contents of the command word are transferred to the subsystem under control of the Interface chip.

When the command word establishes receive operation received data becomes available on the 16 bit data highway when DATA TRANSFER REQUEST ($\overline{DTREQ}$) goes low. The subsystem must be ready for data and take DATA TRANSFER GRANT ($\overline{DTGRT}$) low during that interval. The RTU will strobe data into the subsystem after taking DATA TRANSFER ACKNOWLEDGE ($\overline{DTACK}$) low. This cycle is repeated for each word of the message. The GOOD BLOCK RECEIVED ($\overline{GBR}$) going low will signify to the subsystem that all words of the message are valid and have been transferred. The STATUS ENABLE ($\overline{STATEN}$) line pulses low signifying that the Status Word is available on the 16 bit data highway for the subsystem to read.

When the command word establishes transmit operation the command word is transferred to the subsystem in the same manner as a data word in the receive mode. With the READ/WRITE (R/$\overline{W}$) taken high the RTU will request data from the subsystem by taking $\overline{DTREQ}$ low. The subsystem must make data available on the 16 bit data highway during the interval it takes $\overline{DTGRT}$ low. The RTU will respond by taking $\overline{DTACK}$ low and strobing the data into its buffers. This sequence is followed for all words of the message.

Latches

The ARX 2452 RTU contains several latches for storage of information needed for subsequent operation or data transfer. They are Command Word, Status Bits and BUILT-IN TEST (BIT) Word. The following paragraphs explain the function and use of each.

Command Word

Bits nine through nineteen of the command word, consisting of T/R bit (A11), subaddress–mode (A6-A10) and data word count–current word count (A0-A4) are included in these latches, along with one bit (A5) which designates if command or data words are being transferred.

The subaddress, T/R bit and word count bits may be fed into an external PROM to illegalize mode commands. The output of the PROM should be connected to ILLEGAL COMMAND ($\overline{ILLCMD}$) input.

Status Bits

The following status bits are available for setting by the subsystem:

1. Message Error. This is set automatically when messages are received with error. It may also be set if a PROM is used to illegalize mode commands, activated by the $\overline{ILLCMD}$ input line.
2. Service Request is set by the SERVICE REQUEST ($\overline{SRQ}$) input.
3. Busy is set by the SUBSYSTEM BUSY ($\overline{BUSY}$) line.
4. Subsystem Flag is set by the SUBSYSTEM FLAG ($\overline{SS\ FLAG}$) input.
5. Dynamic Bus Control Acceptance is set by ACCEPT DYNAMIC BUS CONTROL ($\overline{ADBC}$) input.
6. Terminal Flag is set automatically when an RT failure is detected or by REMOTE TERMINAL FLAG ($\overline{RT\ FLAG}$) input.

Built-In Test

Fourteen of the 16 bits of this word store information from the various sources of terminal error, malfunction or condition which will be transmitted to the Bus Controller upon receipt of the Transmit BIT Word mode command. The bit numbers and designations are as follows:

15 Set to zero
14 Set to zero
13 Failsafe timeout in channel B
12 Failsafe timeout in channel A
11 Wraparound failure in channel B
10 Wraparound failure in channel A
9 Transmitter shutdown in channel B
8 Transmitter shutdown in channel A
7 Non-mode broadcast command to transmit
6 Message Error caused by high word count
5 Message Error caused by low word count
4 Illegal bit set by $\overline{ILLCMD}$ input or illegal use of broadcast with mode code
3 Mode code–T/R error
2 Wraparound failure either channel
1 DMA handshake failure
0 Failsafe timeout in either channel

Timeout, handshake and wraparound failure bits (0-2, 10-13) are latched and cleared only by a mode code reset or master reset. Mode code and message error bits (3-7) are cleared on receipt of a new message and set at the end of the present message. Transmitter shutdown bits are set when a mode command for transmitter shutdown is implemented and cleared when a mode command to override transmitter shutdown, or a reset remote terminal mode command or a master reset is executed.

Specifications ARX 2452 & 2462

Absolute Maximum Ratings

	ARX 2452	ARX 2462
Supply Voltage V+	−0.3 to +18.0V	
Supply Voltage V−	+0.3 to −18.0V	
Supply Voltage V_{DD}	−0.3 to +7.0V	
Logic Input Voltage	−0.3 to V_{DD} + .3V	
Receiver Differential Input	40V p-p	
Receiver Input Voltage (Common Mode)	± 10V	
Driver Peak Output Current	300 mA	360 mA
Maximum Power Dissipation Total Hybrid At 100% Duty Cycle Total Hybrid At Standby	 3.32W 2.04W	 2.88W 1.85W

Power Data

CURRENTS, MAXIMUMS	ARX 2452		ARX 2462		ALL	UNITS
Duty Cycle	+15V	−15V	+12V	−12V	5V	
0% (Standby)	59	47	64	52	70	mA
50%	167	47	212	52	70	mA
100% Note 1	267	47	360	52	70	mA

Operating Tolerance for Power Supplies: ±12V and ±15V @ 5%; 5V @ 10%.

Physical

Temperature Operating (case) Storage (ambient)	 −55 to 125° C −65 to 150° C
Weight	1.7 oz. (48.28 gm.) typ.
Thermal Thermal Resistance Junction To Case, Θjc, for Hottest Die Temperature Rise Hottest Die, Junction To Case	 88° C per watt 45.5° C @ 100% duty cycle

NOTE 1. Parameter guaranteed by design, not production tested.

Electrical Characteristics

PARAMETER	CONDITION	SYMBOL	MIN	MAX	UNIT
Driver Differential Output Level	$R_L = 35$ ohms	V_O	6	9	V p-p
Driver Differential Output Impedance	TX off	Z_{OUT}	10K		ohms
Driver Differential Output Noise	TX off	V_{NOI}		10	mV p-p
Driver Output Offset (at point A-A in Figure 6, 2.5 uS after mid-bit crossing of the parity bit of the last word of a 660 uS message)	$R_L = 35$ ohms	V_{OS}		±90	mV
Driver Rise and Fall Times	t_R, t_P		100	300	nS
Receiver Differential Input Impedance	f = 1MHz	Z_{IN}	10K		ohms
Receiver Threshold Voltage (Sinewave Input Measured at point A-A, Fig. 6.)	100 KHz to 1MHz	V_{TH}	0.6	1.2	V p-p
Logic "1" Output Voltage 1 Pins 1, 2, 3, 16, 25, 27, 28, 35, 40, 41, 42 65, 73, 78.	$I_{OH} = .3$mA	V_{OH1}	2.4		V
Logic "1" Output Voltage 2 Pins 4, 5, 6, 7, 8, 9, 10, 11, 21, 22, 24, 26, 29, 32, 43, 44, 45, 46, 47, 48, 49, 50, 60 61, 63, 64.	$I_{OH} = 3$mA	V_{OH2}	2.4		V
Logic "0" Output Voltage 1 Pins 1, 2, 3, 25, 27, 28, 32, 35, 40, 41, 42 65, 73, 78.	$I_{OL} = -1.6$mA	V_{OL1}		0.4	V
Logic "0" Output Voltage 2 Pins 16, 21, 22, 24, 26, 29, 60, 61, 62, 63, 64.	$I_{OL} = -4$mA	V_{OL2}		0.4	V
Logic "0" Output Voltage 3 Pins 4, 5, 6, 7, 8, 9, 10, 11, 43, 44, 45, 46, 47, 48, 49, 50	$I_{OL} = -6$mA	V_{OL3}		0.4	V
Logic "0" Input Voltage		V_{IL}		0.7	V
Logic "1" Input Voltage		V_{IH}	2.4		V
Logic "0" Input Current 1 (no pull ups) Pins 13, 14, 15, 30, 53, 54, 68, 71, 72	$V_{IL} = 0.7$V	I_{IL1}	−20	20	uA
Logic "0" Input Current 2 (pull ups) Pins 4, 5, 6, 7, 8, 9, 10, 11, 12, 23, 33, 34, 43, 44, 45, 46, 47, 48, 49, 50, 55, 66, 67, 69	$V_{IL} = 0.7$V	I_{IL2}		−330.	uA
Logic "1" Input Current 1 (no pull ups) Pins 13, 14, 15, 30, 56, 68, 71, 72	$V_{IH} = 2.7$V	I_{IH1}	−20	20	uA
Logic "1" Input Current 2 (pull ups) Pins 4, 5, 6, 7, 8, 9, 10, 11, 12, 23, 33, 34, 43, 44, 45, 46, 47, 48, 49, 50, 55, 66, 67, 69	$V_{IH} = 2.7$V	I_{IH2}	−20	20	uA
Logic Input Capacitance	f = 1 MHz	C_I		5	pF

ARX 2452 Pin Function Table

PIN	SIGNAL NAME	I/O	DESCRIPTION
1	A10	O	Bit 4 (MSB) of the subaddress field of the command word.
2	A8	O	Bit 2 of the subaddress field of the command word.
3	A6	O	Bit 0 (LSB) of the subaddress field of the command word.
4	D1	I/O	Data highway bit 1
5	D3	I/O	Data highway bit 3
6	D5	I/O	Data highway bit 5
7	D7	I/O	Data highway bit 7
8	D9	I/O	Data highway bit 9
9	D11	I/O	Data highway bit 11
10	D13	I/O	Data highway bit 13
11	D15	I/O	Data highway bit 15 (MSB)
12	BRO ENA	I	Broadcast enable. When low inhibits response to broadcast (RTU address 31); when high recognizes broadcast command.
13	ADR4	I	Remote terminal address bit 4 (MSB).
14	ADR2	I	Remote terminal address bit 2
15	ADR0	I	Remote terminal address bit 0 (LSB)
16	RTADERR	O	Address parity error detected when low; RTU will not respond to a terminal address other than broadcast if BRO ENA is high.
17	TX DATA B	O	Secondary bus channel transmitter low output.
18	+15V B	I	Secondary channel transceiver positive supply voltage.
19	GND B	I	Secondary channel power supply return.
20	RX DATA B	I	Secondary bus channel receiver high input.
21	A3	O	When command word subaddress is mode code or INCMD is low, bit 3 of mode code/ word count field; otherwise bit 3 of current word counter.
22	A1	O	When command word subaddress is mode code or INCMD is low, bit 1 of mode code/ word count field; otherwise bit 1 of current word counter.
23	DTGRT	I	Data transfer grant. A low indicates subsystem is ready for data transfer.
24	INCMD	O	In command. A high indicates the RTU is servicing a command.
25	HSFAIL	O	Handshake fail. A low indicates subsystem has not supplied DTGRT in sufficient time following DTREQ to permit data transfer. Clears following next NBGT.
26	DTSTR	O	Data transfer strobe. Permits data present on the I/O data highway to be latched into memory or registers. The rising edge should be used to clock data in.
27	A5	O	Low when command word is being transferred; high when a data word is being transferred.
28	RTFAIL	O	Remote terminal failure. A low indicates that a wraparound self test failure has occurred. Clears on the start of next message.
29	DTREQ	O	Data transfer request. A low indicates the RT has data ready or needed for transfer and requires subsystem response. Remains low until transfer is completed or subsystem does not respond within required time limit.
30	ADBC	I	Accept dynamic bus control. A low indicates subsystem has accepted bus controller operation in response to valid Dynamic Bus Control mode command; causes Dynamic Bus Control Acceptance bit in status word register to be set.
31	nc		No connection.
32	A11	O	T/R bit of command word.
33	ILLCMD	I	Illegal command. A low indicates that subsystem has recognized an illegal command. Sets the Message Error bit in the status word register.
34	SRQ	I	Subsystem service request. A low indicates subsystem service request to bus controller. Sets Service Request bit in status word register.
35	BITEN	O	Built-in test word enable. A low indicates BIT word is enabled onto the I/O data highway.
36	RX DATA A	I	Primary bus channel receiver low input.
37	+5V A	I	Primary channel transceiver 5V power supply input.
38	−15V A	I	Primary channel transceiver negative supply voltage.
39	TX DATA A	O	Primary bus channel driver high output.
40	NBGT	O	New bus grant. A low indicates RTU has started to process a new command word.
41	A9	O	Bit 3 of subaddress field of the command word.
42	A7	O	Bit 1 of subaddress field of the command word.
43	D0	I/O	Data highway bit 0 (LSB)
44	D2	I/O	Data highway bit 2
45	D4	I/O	Data highway bit 4
46	D6	I/O	Data highway bit 6
47	D8	I/O	Data highway bit 8
48	D10	I/O	Data highway bit 10
49	D12	I/O	Data highway bit 12
50	D14	I/O	Data highway bit 14
51	+5V	I	+5V power supply input to digital logic.
52	GND	I	Power supply return from digital logic.
53	ADR3	I	Remote terminal address bit 3
54	ADR1	I	Remote terminal address bit 1
55	ADRP	I	Remote terminal address parity bit. Must be set for odd address parity.
56	TX DATA B	O	Secondary bus channel high output.
57	−15V B	I	Secondary channel transceiver negative supply voltage.
58	+5V B	I	Secondary channel transceiver 5V supply.
59	RX DATA B	I	Secondary bus channel receiver low input.
60	A2	O	When command subaddress is a mode code or INCMD is low, bit 2 of mode code/word count field; otherwise bit 2 of the current word counter.
61	A0	O	When command subaddress is a mode code or INCMD is low, bit 0 (LSB) of mode code/ word count field; otherwise bit 0 (LSB) of current word counter.
62	DTACK	O	Data transfer acknowledge. A low indicates data is being transferred to or from subsystem following DTGNT response to DTREQ. May be connected to BUF ENA when data is to be transferred to subsystem.
63	A4	O	When command subaddress is a mode code or INCMD is low, bit 4 (MSB) of mode code/ word count field; otherwise bit 4 (MSB) of current word counter.
64	R/W	O	Read/write. Controls the direction of data highway transfers. When low data is transferred to subsystem; when high data is transferred from the subsystem. The line is high during the interval DTREQ is active.
65	GBR	O	Good block received. A low indicates the command word and all data words of a message transferred to the subsystem are valid and without error.
66	CLK	I	12 MHz clock input to the Bit Processor.
67	BUF ENA	I	Buffer enable. A low enables the data highway tri-state buffers for transfer to subsystem. May be activated by DTACK.
68	RESET	I	Master reset. Resets the entire RTU.
69	RTFLAG	I	Remote terminal flag. A low sets the terminal flag bit in the status word register. May be activated by RTFAIL.
70	nc		No connection
71	BUSY	I	Subsystem busy. A low sets the busy bit in the status word register. When activated the RTU will not request data transfer from the subsystem following receipt of a receive or transmit command.
72	SSFLAG	I	Subsystem flag. A low sets the subsystem flag bit in the status word register.
73	ME	O	Message error. A low indicates an error in the received word of the message being processed. Clears on the next NBGT activation.
74	RX DATA A	I	Primary bus channel receiver high input.
75	GND A	I	Primary channel transceiver power supply return.
76	+15V A	I	Primary channel transceiver positive supply voltage.
77	TX DATA A	I	Primary bus channel transmitter low output.
78	STATENA	O	Status word enable. A low indicates the status word register is being enabled onto the data highway.

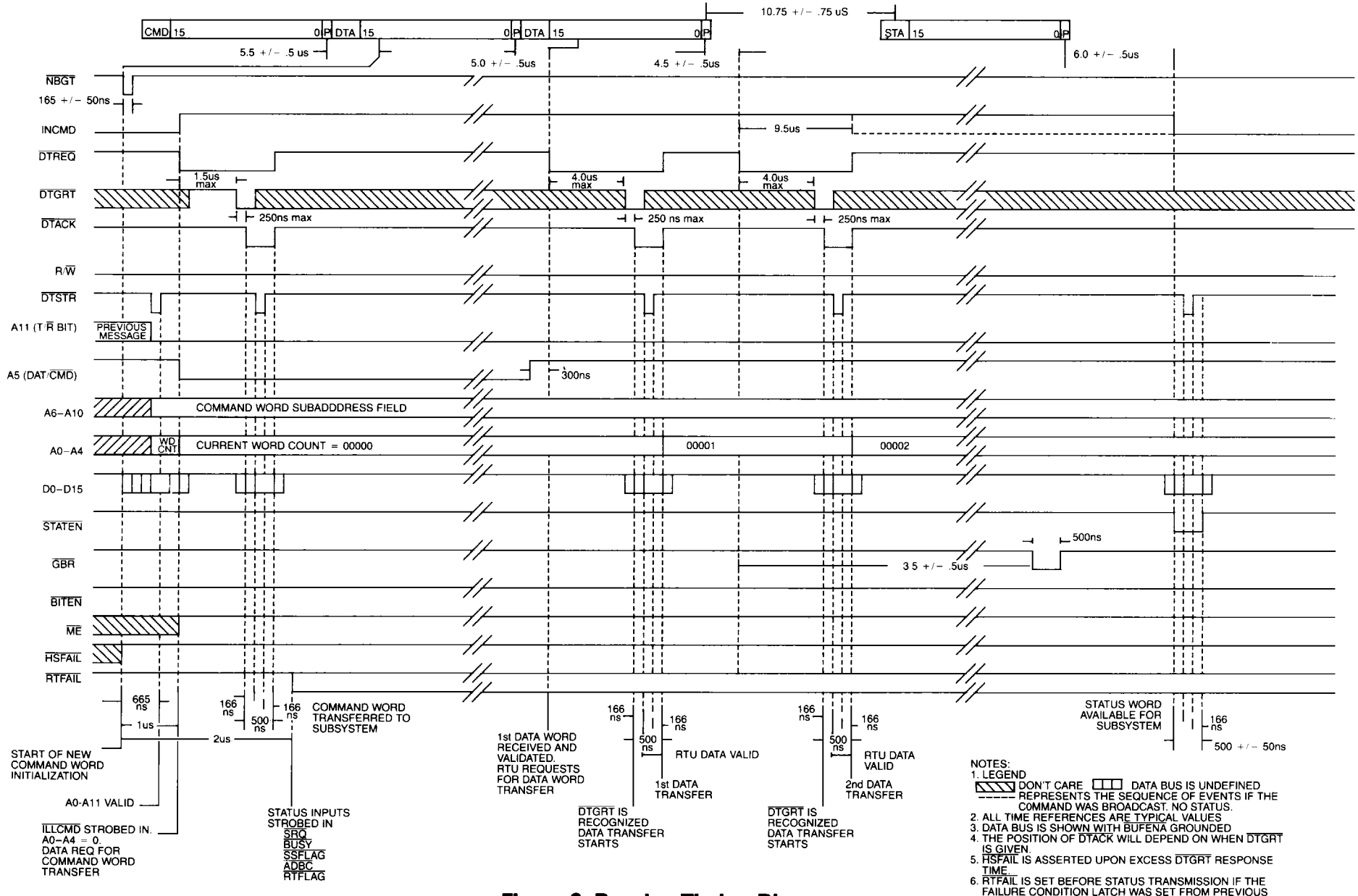


Figure 2: Receive Timing Diagram

NOTES:
1. LEGEND
   - ▨ DON'T CARE ▭ DATA BUS IS UNDEFINED
   - ----- REPRESENTS THE SEQUENCE OF EVENTS IF THE COMMAND WAS BROADCAST. NO STATUS.
2. ALL TIME REFERENCES ARE TYPICAL VALUES
3. DATA BUS IS SHOWN WITH BUFENA GROUNDED
4. THE POSITION OF DTACK WILL DEPEND ON WHEN DTGRT IS GIVEN.
5. HSFAIL IS ASSERTED UPON EXCESS DTGRT RESPONSE TIME.
6. RTFAIL IS SET BEFORE STATUS TRANSMISSION IF THE FAILURE CONDITION LATCH WAS SET FROM PREVIOUS MESSAGE. THE CONDITION LATCH IS RESET AT THE END OF THE MESSAGE.

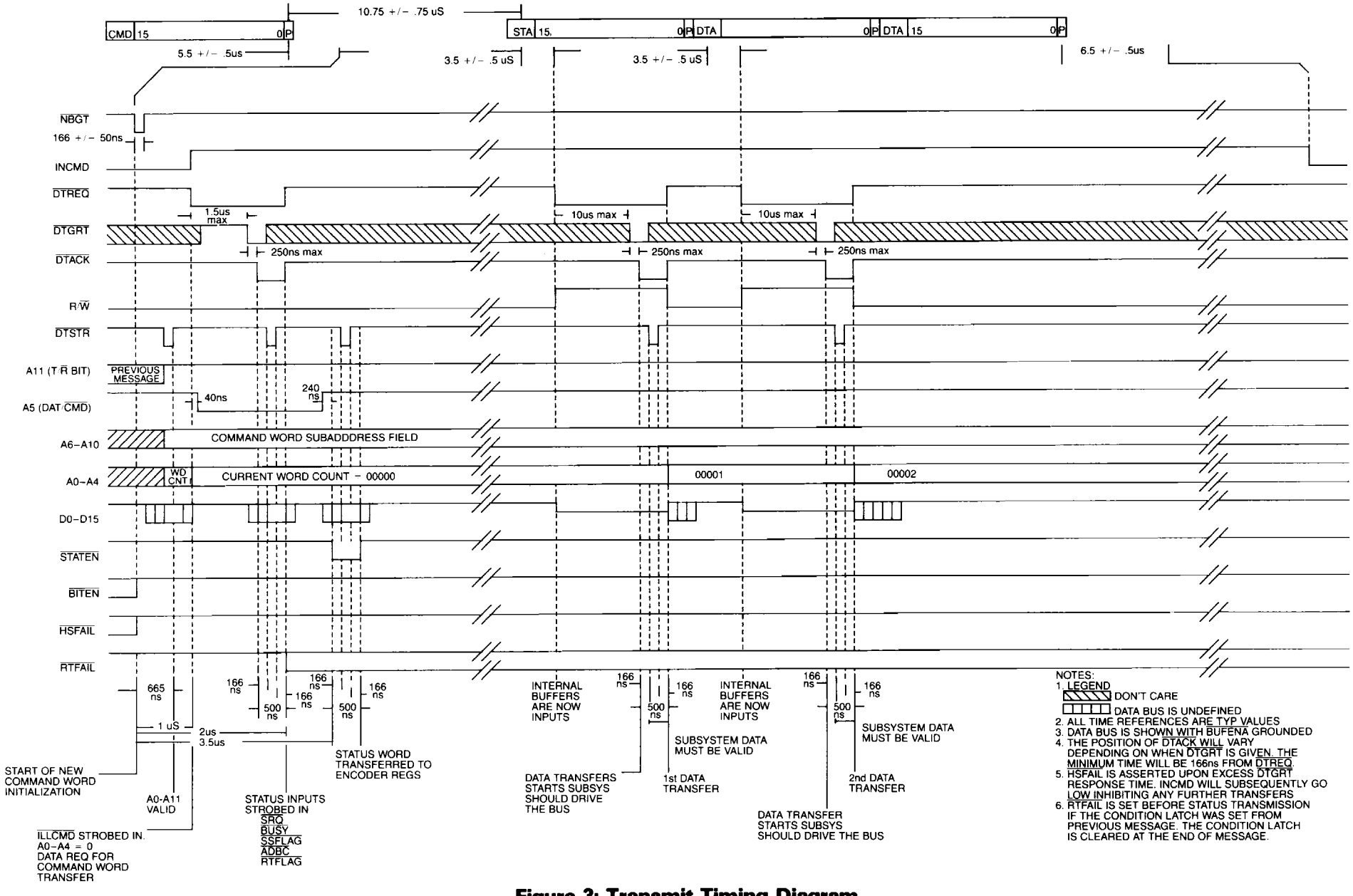


Figure 3: Transmit Timing Diagram

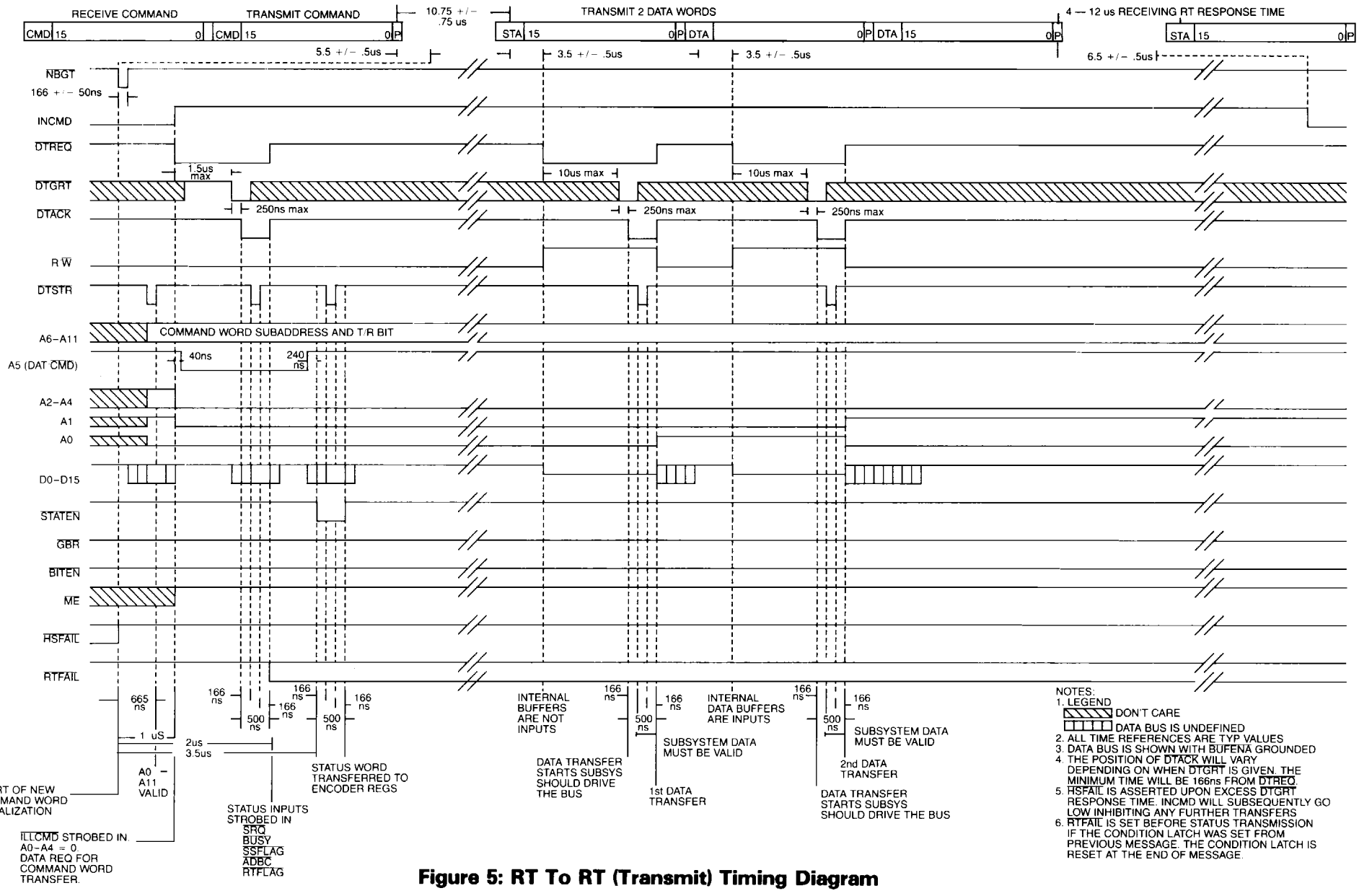
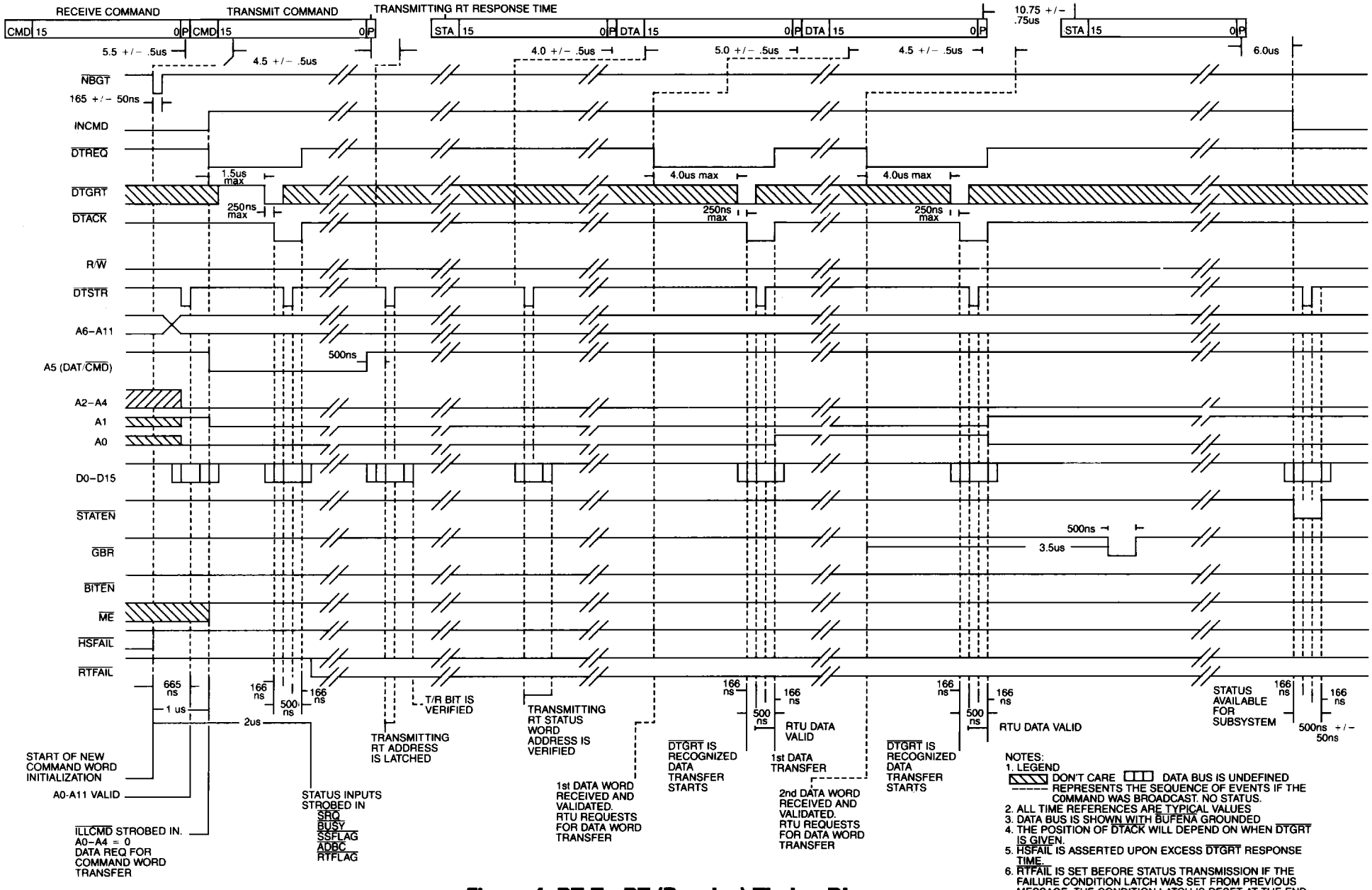


Figure 5: RT To RT (Transmit) Timing Diagram



NOTES:
1. LEGEND
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   - REPRESENTS THE SEQUENCE OF EVENTS IF THE COMMAND WAS BROADCAST. NO STATUS.
2. ALL TIME REFERENCES ARE TYPICAL VALUES
3. DATA BUS IS SHOWN WITH BUFENA GROUNDED
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Figure 4: RT To RT (Receive) Timing Diagram

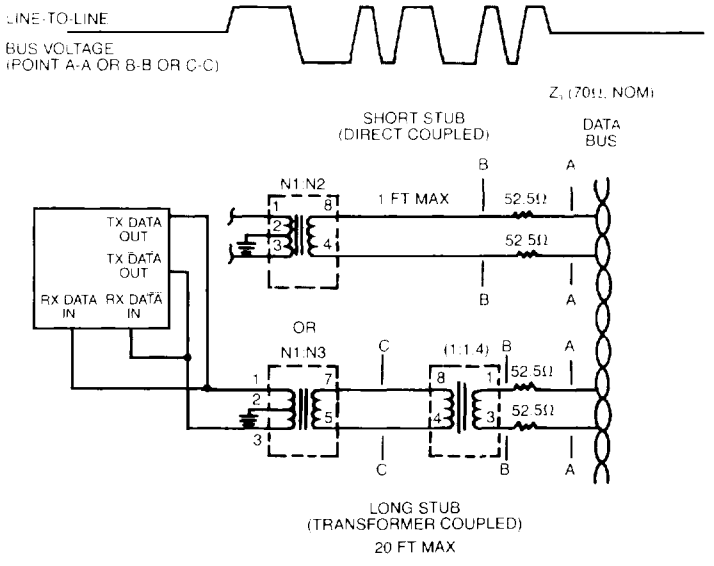
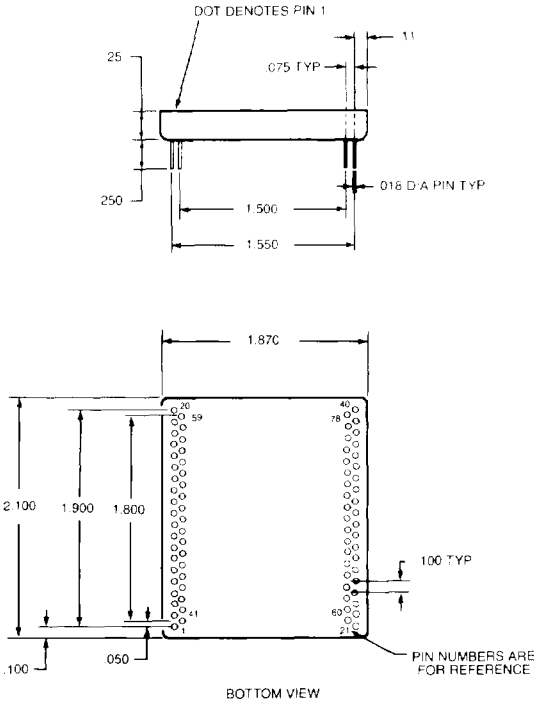


Figure 6: (One Channel Shown)



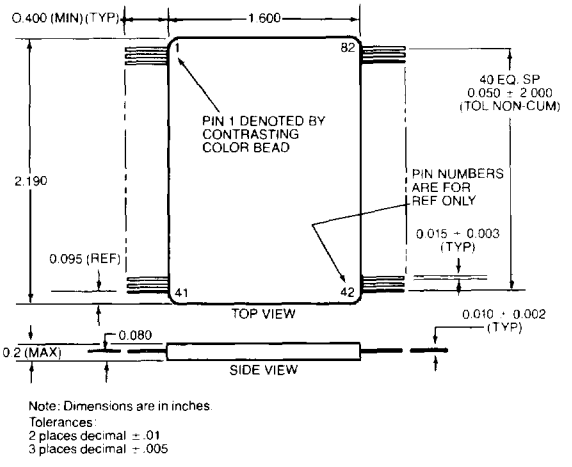
PLUGIN

Figure 7: Configurations

MODEL	POWER SUPPLY	N1:N2	N1:N3
ARX 2452	± 15V & 5V	1.4:1	2:1
ARX 2462	± 12V & 5V	1:1	1:.707

Ordering Information:

Model ARX 2452 Plug In
Model ARX 2452FP Flat Pack
Model ARX 2462 Plug In
Model ARX 2462FP Flat Pack



FLATPACK

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Specifications subject to change without notice.