SONET/SDH SERIAL TO PARALLEL/PARALLEL TO SERIAL CONVERTER S3022

FEATURES

- Performs serial to parallel conversion for SONET STS-12 or STS-3 data streams.
- Operates at equivalent SDH data rates for processing STM-4 or STM-1 data streams.
- Converts a 622 Mbit/s or 155 Mbit/s bit serial stream into a 78 Mbyte/s or 19 Mbyte/s 8-bit byte serial data stream, respectively.
- Performs partial framing to A1 and A2 bytes.
- Checks for three A1 bytes followed by three A2 bytes as required for SONET/SDH or optionally checks for a single A1 byte followed by a single A2 byte as required for 139 Mbit/s ATM interfaces.
- Selectable Coded Mark Inversion (CMI) line decoding for STS-3 electrical interfaces at 155 Mbit/s and 139 Mbits/s ATM interfaces.
- Performs parallel to serial conversion for SONET STS-12 or STS-3 data streams.
- Operates at equivalent SDH data rates for processing STM-4 or STM-1 data streams.
- Converts a 78 Mbyte/s or 19 Mbyte/s 8-bit byte serial data stream into a 622 Mbit/s or 155 Mbit/s bit serial stream, respectively.
- Selectable Coded Mark Inversion (CMI) line encoding for STS-3 electrical interfaces at 155 Mbit/s and 139 Mbits/s ATM interfaces.
- Supports diagnostic (transmit to receive) loopback and line (receive to transmit) loopback modes.
- Directly interfaces to the PMC-Sierra PM5301 SSTX SONET/SDH Section Terminating Transceiver device, the PM5312 STTX SONET/SDH Transport Terminating Transceiver, and the PM5355 SUNI-622 Saturn User Network Interface devices.
- Simple TTL/CMOS-level interface on the low speed side, ECL-level (100K) on the high speed side
- +5 Volt, -4.5 Volt power supplies.
- 120-pin Thermally Enhanced Package (TEP).

APPLICATIONS

- Section Repeaters
- Add-Drop Multiplexers
- Broadband Cross-Connects
- ATM Switching Systems
- Fiber Optic Terminals
- Fiber Optic Test Equipment

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Figure 1. S3022 Block Diagram

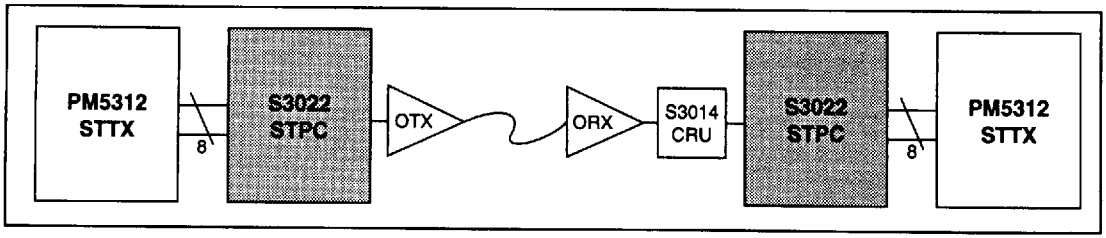
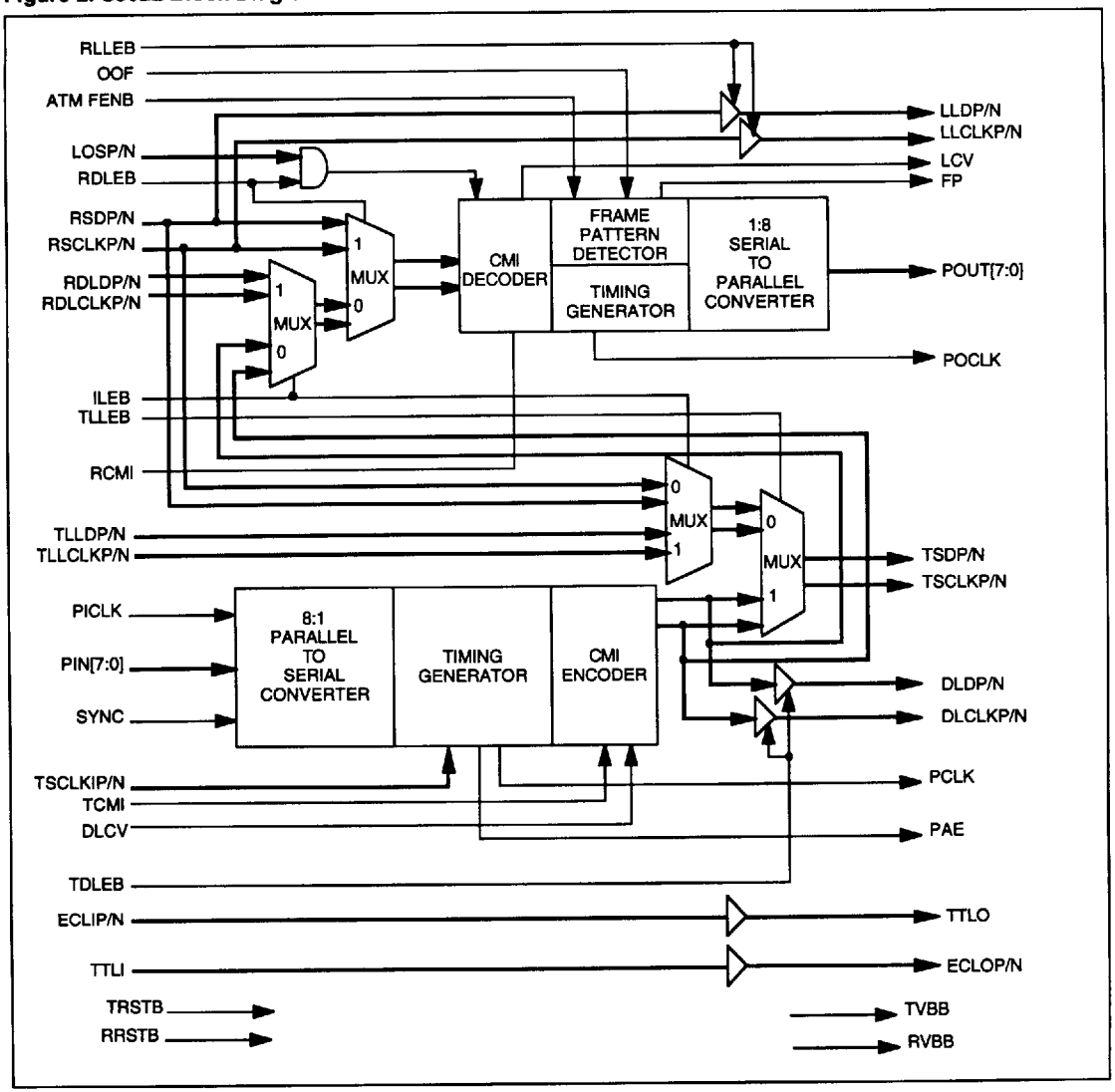


Figure 2. S3022 Block Diagram



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GENERAL DESCRIPTION

The S3022 STPC SONET/SDH Serial to Parallel/ Parallel to Serial Converter is a fully integrated high speed Synchronous Optical Network (SONET) compatible front and back end. It is also fully compatible with the CCITT Synchronous Digital Hierarchy (SDH) standards for STM-4 and STM-1 operation.

The STPC serial to parallel converter section provides the first stage of digital processing of a receive SONET STS-12 or STS-3 bit-serial stream. The STPC converts the bit-serial 622 Mbit/s or 155 Mbit/s data stream into a 78 Mbyte/s or 19 Mbyte/s byte-serial data format. A Coded Mark Inversion (CMI) decoder can be enabled during 155 Mbit/s operation for decoding STS-3 or 139 Mbit/s ATM electrical signals. CMI mode is selected by an input pin.

The STPC parallel to serial converter section provides the last stage of digital processing of a transmit SONET STS-12 or STS-3 bit-serial stream. The STPC converts the 78 Mbyte/s or 19 Mbyte/s byte-serial data stream into a bit-serial 622 Mbit/s or 155 Mbit/s data format. A Coded Mark Inversion (CMI) encoder can be enabled during 155 Mbit/s or 139 Mbit/s ATM for encoding STS-3 electrical signals. CMI mode is selected by an input pin.

The STPC is designed to interface with the PMC-Sierra PM5301 SSTX SONET/SDH Section Terminating Transceiver which performs frame confirmation, descrambling, and other processing of the receive data stream and performs frame insertion, scrambling, and other processing of the transmit data stream.

Clock recovery is performed external to the STPC device and the recovered clock must be provided to the STPC serial to parallel converter section. High speed clock generation is also performed external to the STPC device and the high speed transmit clock must be provided to the STPC parallel to serial converter section.

Loopback mode enable and signal pins are provided for diagnostic loopback (transmitter to receiver) and line loopback (receiver to transmitter) functions. These signal paths may be implemented internally or external pins may be utilized to implement such loopbacks.

FUNCTIONAL DESCRIPTION

Frame and Byte Boundary Detection

The SONET/SDH fundamental frame format consists of three transport overhead bytes followed by Synchronous Payload Envelope (SPE) bytes. This pattern of 3 overhead and 87 SPE bytes is repeated 9 times in each frame. The first byte in the frame is the overhead A1 (F6H) framing byte. The next is the A2 (28H) framing byte. All bytes, except for A1, A2, and one subsequent overhead byte, are scrambled.

For STS-3 or STM-1, the number of bytes is tripled, so that there are 9 overhead bytes followed by 261 SPE bytes, repeated 9 times per frame. The frame signature becomes three A1 bytes followed by three A2 bytes. For STS-12 or STM-4, the frame signature becomes twelve A1 bytes followed by twelve A2 bytes.

The Frame and Byte Boundary Detection block searches the incoming data for three consecutive A1 bytes followed immediately by three consecutive A2 bytes. This pattern occurs in both STS-3 and STS-12. Framing pattern detection is enabled and disabled by the out of frame (OOF) input. Detection is enabled by a rising edge on OOF, and remains enabled for the duration OOF is set high. It is disabled when a framing pattern is detected and OOF is no longer set high. When framing pattern detection is enabled, the framing pattern is used to locate byte and frame boundaries in the incoming data stream (RSD or DLD). The timing generator block takes the byte boundary and uses it to block the incoming data stream into bytes for output on the parallel output data bus (POUT[7:0]). The frame boundary is reported on the frame pulse (FP) output when any 48-bit pattern matching the framing pattern is detected on the incoming data stream. When framing pattern detection is disabled, the byte boundary is frozen to the location found when detection was previously enabled. Only framing patterns aligned to the fixed byte boundary are indicated on the FP output.

The probability that random data in an STS-3 or STS-12 stream will generate the 48-bit framing pattern is extremely small. It is very improbable for a mimic pattern to occur within one frame of data. Therefore, the time to find the first frame pattern and to verify it with downstream circuitry, at the next occurrence of the pattern, is expected to be less than the required 250 µs, even for extremely high bit error rates.

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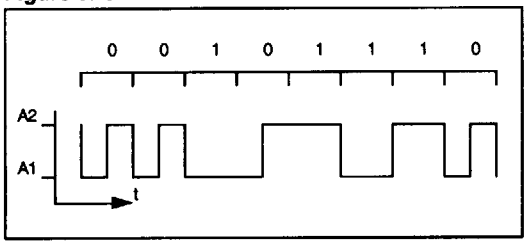
Once downstream overhead circuitry has verified that frame and byte synchronization are correct, the OOF input should be set low to disable the frame search process from trying to synchronize to a mimic frame pattern.

Serial To Parallel Converter

The Serial To Parallel Converter block consists of three 8-bit registers. The first is a serial-in, parallel-out shift register, which performs serial to parallel conversion clocked by the receive serial clock. The second is an 8-bit internal holding register, which transfers data from the serial to parallel register on byte boundaries as determined by the frame and byte boundary detection block. On the falling edge of the free running POCLK, the data in the holding register is transferred to an output holding register which drives POUT[7:0].

The delay through the Serial to Parallel converter can vary from 1.5 to 2.5 byte periods (12 to 20 serial bit periods) measured from the first bit of an incoming byte to the beginning of the parallel output of that byte. The variation in the delay is dependent on the alignment of the internal parallel load timing, which is synchronized to the data byte boundaries with respect to the falling edge of POCLK, which is independent of the byte boundaries. The advantage of this serial to parallel converter is that POCLK is neither truncated nor extended during reframe sequences.

Figure 3. CMI Encoded Data



CMI Decoder

The Code Mark Inversion (CMI) Decoder block converts CMI encoded data to NRZ data. The CMI format ensures at least one data transition per bit period, thus aiding the clock recovery process. Zeros are represented by a Low state for one half a bit period, followed by a High state for the next half bit period. Ones are represented by a steady Low or High state for a full bit period. The state of the one's bit period alternates at each occurrence of a one. The STS-3 electrical interface is specified to have CMI coded data. Figure 3 shows an example of CMI encoded data.

The CMI decoder accepts serial data from the receive stream at a rate of 311.04 MHz, decodes the data from CMI format to NRZ format, and shifts it out at a rate of 155.52 Mbit/s. The decoder is only in the data path when the STS-3 CMI mode is selected.

CMI coding violations, such as a corrupted bit represented by a high logic level followed by a low logic level, or two consecutive ones represented by the same logic level, result in a pulse on the LCV output. Each LCV pulse is asserted for one POCLK period and is aligned to the byte on POUT[7:0] containing the line code violation.

The CMI decoder assumes one of two phase alignments as required to correctly process CMI encoded data. If an excessive number of closely spaced line code violations occur, the CMI decoder assumes that it is incorrectly phase aligned to bit boundaries and switches to the alternate phase alignment for subsequent decoding. At bit error rates below 10^{-3}, the error multiplication incurred is negligible.

Note that there will be four LCV's reported when a phase adjustment is made.

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Diagnostic Loopback

The Diagnostic Loopback circuitry consists of alternate serial data inputs which can be connected to the serial output of a SONET transmitter, or connected internally to set up a transmit to receive loopback.

The differential ECL input RDLD is the Diagnostic Loopback serial data input. When the Receive Diagnostic Loopback Enable (RDLEB) input is set low and Internal Loopback Enable (ILEB) is set high, the RDLD input is routed in place of the normal data stream (RSD). Similarly, the RDLCLK input replaces the RSCLK input. When DLD and DLCLK outputs are connected to the RDLD and RDLCLK inputs and TDLEB and RDLEB are low, a loopback from the transmitter to the receiver at the serial data rate can be set up for diagnostic purposes.

When the Receive Diagnostic Loopback Enable (RDLEB) input is set low, and Internal Loopback Enabled (ILEB) is set low, the output of the parallel to serial converter section is routed in place of the normal data stream (RSD). Similarly, the STPC transmit serial clock replaces the RSCLK input. An internal loopback from the transmitter to receiver at the serial data rate is set up for diagnostic purposes, without any external connections necessary.

When TDLEB is set high, RDLD and RDLCLK outputs are inactive.

Line Loopback

The Line Loopback circuitry consists of alternate clock and data output drivers. The Line Loopback Clock (LLCLK) and Line Loopback Data (LLD) outputs may be connected to the Line Loopback inputs of a SONET receiver device or internally to establish a receive to transmit loopback.

The differential ECL input TLLD is the Line Loopback serial data input. When the Transmit Line Loopback Enable (TLLEB) input is set low and with the Internal Loopback disabled (ILEB set high), the TLLD inputs are routed in place of the normal internal data stream. Similarly, the TLLCLK inputs replaces the TSCLKI inputs. When the LLD and LLCLK outputs are connected to the TLLD and TLLCK inputs with the TLLEB set low and ILEB set high, a loopback from the receiver to transmitter at the serial data rate can be set up for line loopback purposes.

When the Transmit Line Loopback Enable (TLLEB) input is set low, with the Receive Line Loopback enabled (RLLEB set low), and Internal Loopback enabled (ILEB set low), the receive serial data (RSD) input is routed in place of the normal internal data stream. Similarly, the receive clock (RSCLK) input replaces the TSCLKI input. When TLLEB and ILEB are low, a loopback from the receiver to transmitter at the serial data rate can be set up for line loopback purposes, without any external connections necessary.

When RLLEB is low, LLD and LLCLK outputs are enabled. When RLLEB is high, LLD and LLCLK outputs are disabled.

Timing Generation

The Timing Generation block provides three separate functions. It generates a byte rate version of TSCLKI, generates an internal byte rate clock which loads the parallel to serial shift register, and provides a mechanism for aligning the phase between the incoming byte clock and the clock which loads the parallel to serial shift register.

The PCLK output is a byte rate version of TSCLKI. In normal mode, PCLK is equal to TSCLKI divided by eight, and in CMI mode, PCLK is equal to TSCLKI divided by sixteen. PCLK is intended for use as a byte speed clock for upstream multiplexing and overhead processing circuits, such as the PM5301 SSTX SONET/SDH Section Terminating Transceiver. Using PCLK for upstream circuits will ensure a stable frequency and phase relationship between the data coming into and leaving the STPC device. PCLK is generated by a free running divider that is clocked by TSCLKI.

In the parallel to serial conversion process, the incoming data is passed from the PICLK byte clock timing domain to the internally generated byte clock timing domain, which is phase aligned to TSCLKI. Although the frequency of PICLK and the internally generated byte clock must be identical, their phase relationship is arbitrary. To prevent errors caused by short setup or hold times between the two timing domains, the timing generator circuitry monitors the phase relationship between PICLK and the internally generated byte clock. Should the magnitude of the phase difference be less than one TSCLKI bit period, and if the SYNC input is high, the timing block inverts the internal byte clock.

Since the inversion of the internal byte clock will corrupt one byte of data, SYNC should be held low except when a phase correction is desired. When a timing domain phase difference of less than one bit period is detected, the Phase Alignment Event output (PAE) pulses high for one PCLK clock period. If the condition persists, PAE will remain high. When PAE conditions occur, SYNC should be activated until the condition is no longer present. Upon reset, the internal byte clock is aligned to be 180° out of phase with respect to PICLK.

Parallel To Serial Converter

The Parallel to Serial converter block is comprised of two byte-wide registers. The first register latches the data from the PIN[7:0] bus on the rising edge of PICLK. The second register is a parallel loadable shift register which takes its parallel input from the first register.

An internally generated byte clock, which is phase aligned to TSCLKI as described in the Timing Generator block description, activates the parallel data transfer between registers. In normal mode, the serial data shifts out of the second register and into the output selection logic at the TSCLKI rate. In CMI mode, the serial data shifts out of the register and into the CMI encoder at one half the TSCLKI rate (normally 155.52 Mbit/s). The data from the CMI encoder shifts into the output selection logic at the TSCLKI rate (normally 311.04 Mbit/s). The CMI input controls whether the CMI encoder is in the data path.

CMI Encoder

The CMI encoder accepts serial data from the Parallel To Serial Converter block at 155.52 bit/s, encodes the data into CMI format, and shifts the result out at the 311.04 MHz rate of TSCLKI. The encoder is only in the data path when CMI mode is selected. A single CMI violation can be inserted for diagnostic purposes by applying a low to high transition on DLCV. This violation is either an inverted zero code or an inversion of the alternating ones logic level, depending on the state of the data. Subsequent one codes take into account the induced violation to avoid error multiplication.

FUNCTIONAL TIMING

Figure 4 shows a typical reframe sequence in which a byte realignment is made. The frame and byte boundary detection is enabled by the rising edge of OOF and remains enabled while OOF is high. Both boundaries are recognized upon receipt of the third A2 byte which is the first data byte to be reported with the correct byte alignment on the outgoing data bus (POUT[7:0]). Concurrently, the frame pulse is set high for one POCLK cycle.

When interfacing with a PM5301 SSTX device, the OOF input remains high for one full frame after the first frame pulse while the SSTX verifies internally that the frame and byte alignment are correct, as shown in Figure 4. Since at least one framing pattern has been detected since the rising edge of OOF, boundary detection is disabled when OOF is set low.

OOF Operation Timing

The frame and byte boundary detection block is activated by the rising edge of OOF, and stays active until the first FP pulse or until OOF goes low, which ever occurs last. Figure 5 shows a typical OOF timing pattern which occurs when the SPTC is connected to a down stream PM5301 SSTX device. OOF remains high for one full frame after the first FP pulse. The frame and byte boundary detection block is active until OOF goes low.

Alternate OOF Timing

Figure 6 shows the frame and byte boundary detection activation by a rising edge of OOF, and deactivated by the first FP pulse.

Figure 7 shows the input timing between the parallel input clock (PICLK) and the parallel input data (PIN[7:0]). PIN[7:0] data is sampled on the rising edge of the PICLK.

Pin[7:0] Input Timing

The timing relationship between the input line/diagnostic loopback clock (TLLCLK/RDLCLK) and the line/diagnostic loopback data (TLLD/RDLD) is shown in Figure 8a. TLLD is sampled on the rising edge of the TLLCLK clock input and RDLD is sampled on the rising edge of the RDLCLK clock input.

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Figure 4. Frame and Byte Detection Timing

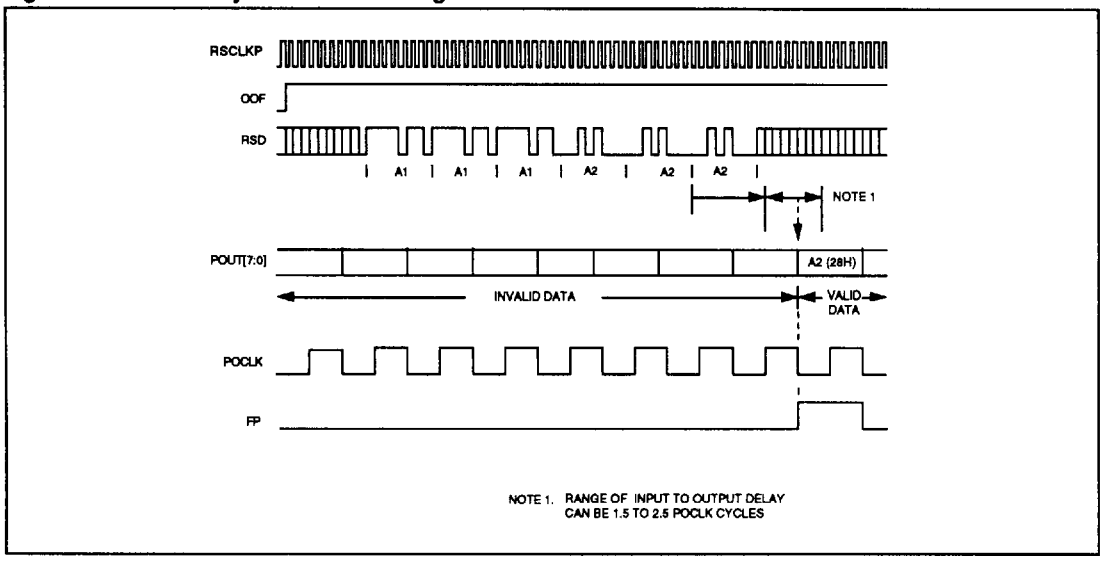

Figure 5. OOF Operation Timing

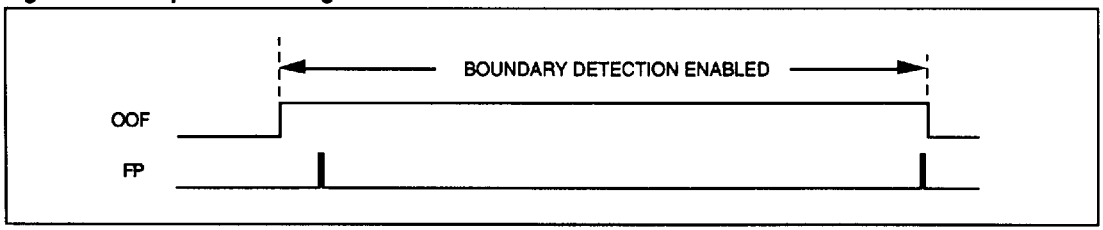

Figure 6. Alternate OOF Timing

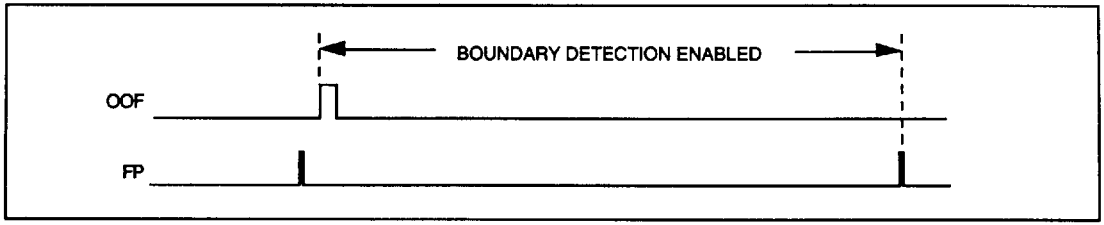

Figure 7. Pin[7:0] Input Timing

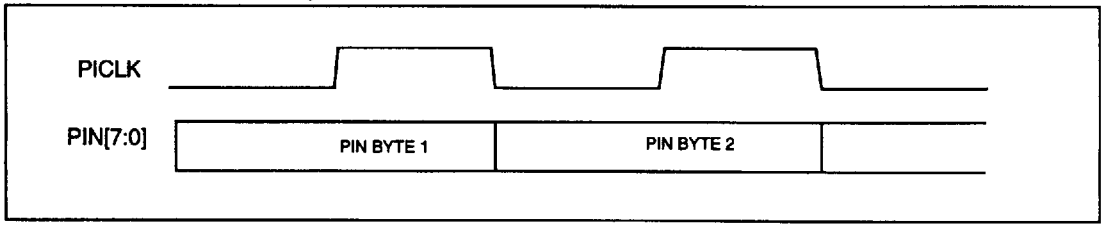

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Figure 8b shows the output timing of the line/diagnostic loopback data (LLD/DLD) in relation to the line/diagnostic loopback clock (LLCLK/DLCLK). LLD is updated on the falling edge of LLCLKP and DLD is updated on the falling edge of DLCLKP. DLDP is held at a logic low and DLCLKP is held at a logic high when diagnostic loopback is disabled (TDLEB high). LLDP is held at a logic low and LLCLKP is held at a logic high when line loopback is disabled (RLLEB high).

Figure 9a shows the output timing of the transmit serial data (TSD) in relation to the transmit output clock (TSCLK). TSD is updated on the falling edge of TSCLKP.

Figure 9b shows the input timing of the receive serial data (RSD) in relation to the receive output clock (RSCLK). RSD is sampled on the rising edge of RSCLKP.

As shown in Figure 10 the phase alignment error (PAE) signal is updated on the falling edge of the parallel clock (PCLK).

The parallel input data (PIN[7:0]) is sampled into a holding register on the rising edge of the parallel input clock (PICLK). The data is periodically transferred from the holding register to a parallel-in, serial-out shift register. The delay from PICLK to the transmit serial data (TSD) output ranges from 1 to 9 TSCLK periods depending on the alignment of PICLK and the transfer point. If PICLK rises within one bit period (lead or lag) of the transfer point, a phase alignment error alarm is raised by setting PAE high for one parallel clock (PCLK) period. In NRZ mode, the bit period and the TSCLK period are identical. In CMI mode, the bit period is twice the TSCLK period. The internal transfer point is realigned if a phase alignment error is detected and the synchronization enable (SYNC) signal is active. Figure 11a shows the effect of the realignment of the transfer point when PICLK leads the transfer point by less than one bit period. Figure 11b shows the effect of the realignment when PICLK lags.

Figure 8a. Loopback Input Timing

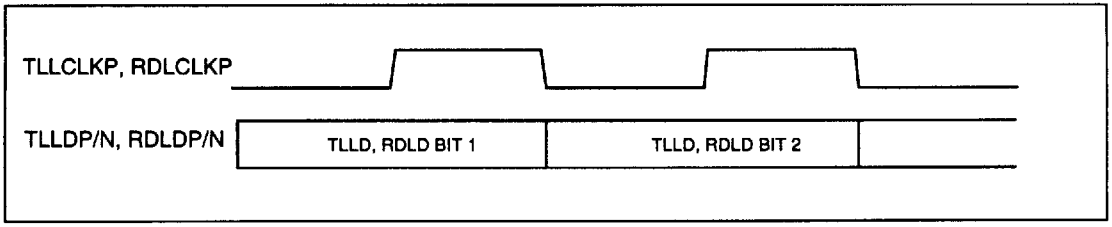

Figure 8b. Loopback Output Timing

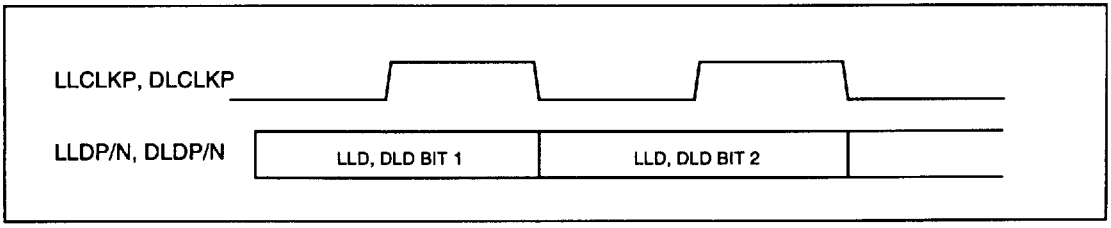

Figure 9a. TSD Output Timing

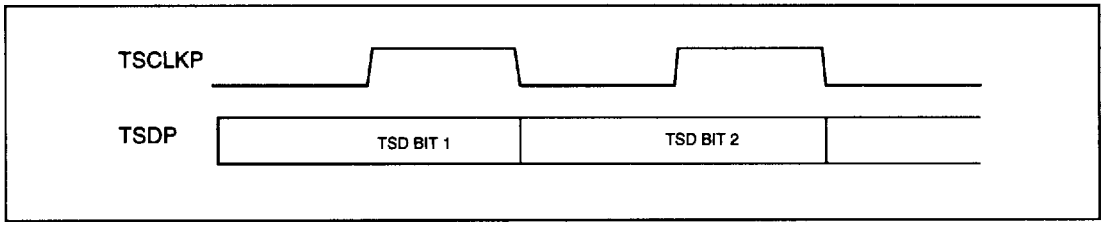

Figure 9b. RSD Input Timing

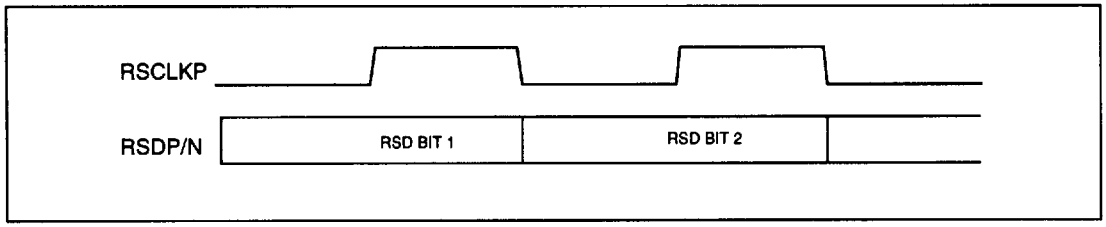

Figure 10. PCLK & PAE Output Timing

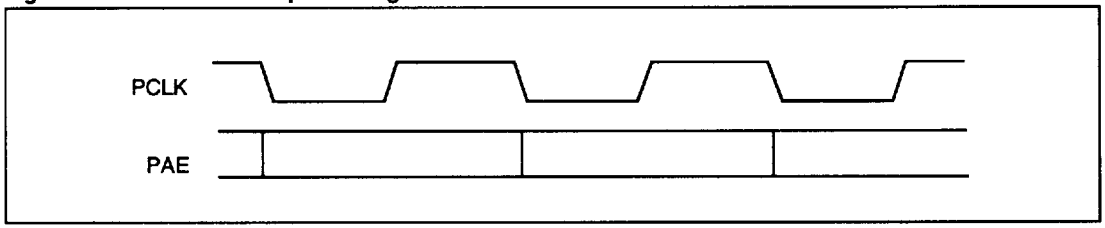

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Figure 11a. Data Delay and Phase Correction Operation (PICLK leading)

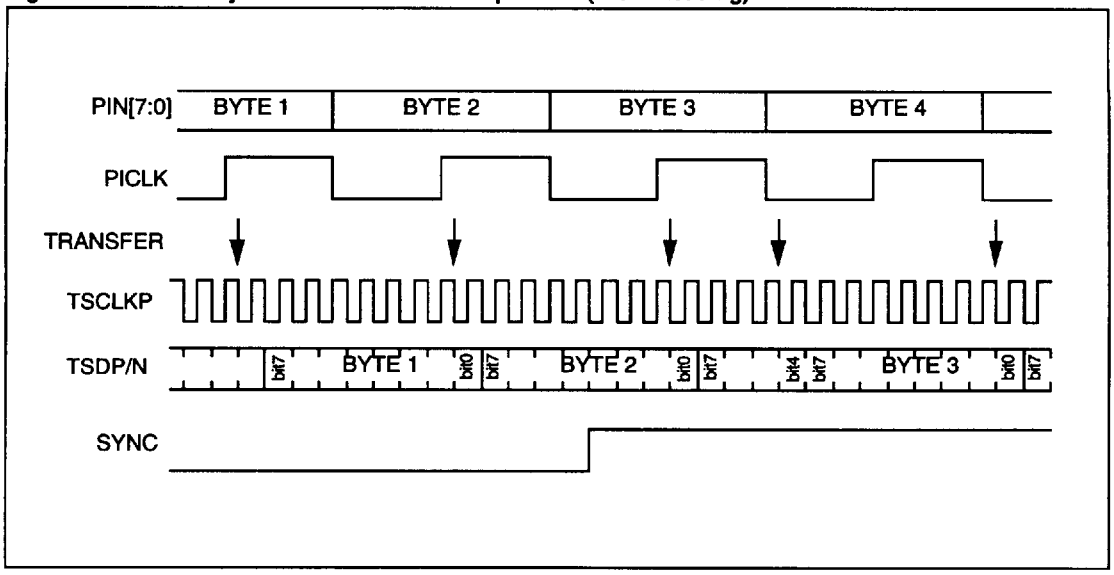
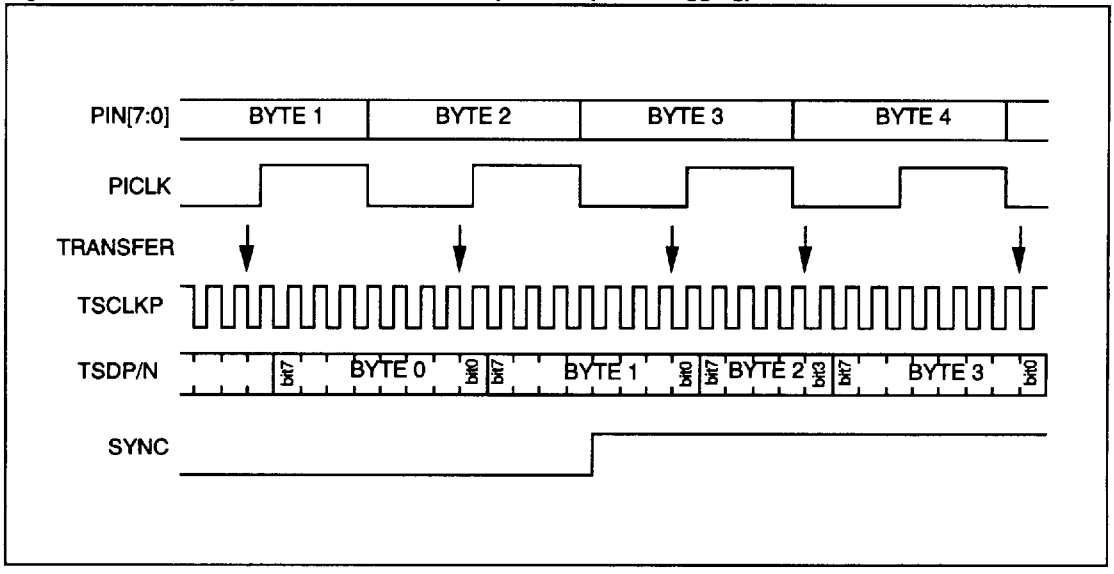


Figure 11b. Data Delay and Phase Correction Operation (PICLK lagging)



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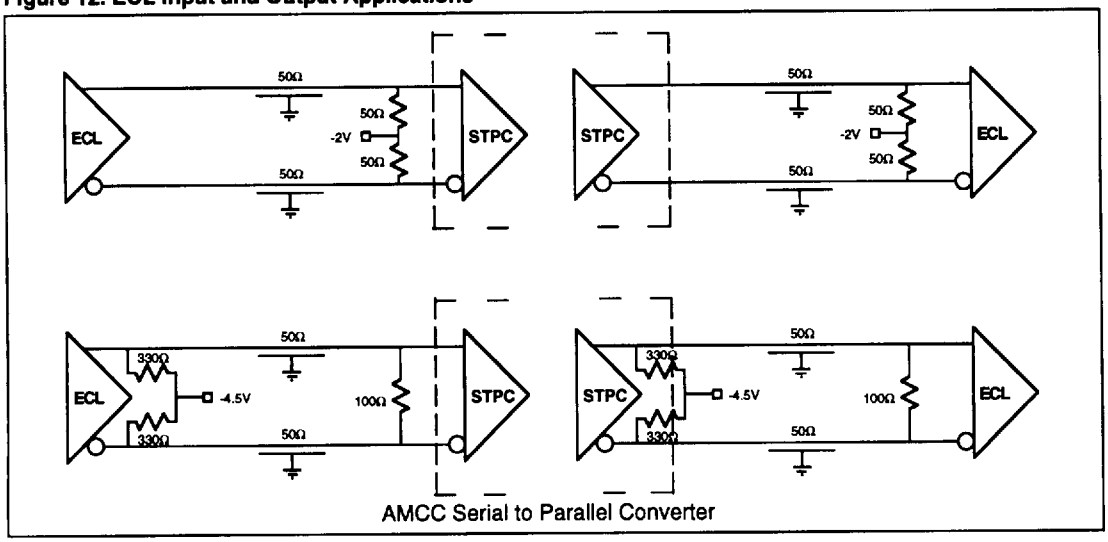
ECL Inputs and Outputs

The ECL compatible differential outputs are standard 100K style emitter follower outputs capable only of sourcing current. They are designed to be terminated with 50 Ω from each output to -2 Volts, assuming that each output drives a 50 Ω transmission line. As with standard 100K ECL logic, the requirement for a -2 Volt supply can be avoided by terminating into a Thevinen equivalent "H" network or by biasing the outputs at the source with pull down resistors connected to a -4.5 Volt supply and terminating the transmission lines at the sink with 50 Ω terminations to AC ground (or equivalently with 100 Ω between the differential signals).

The high speed ECL compatible differential inputs have no built in termination and are assumed to be terminated externally as required by the source that is driving them. To accommodate single-ended ECL input signals it is recommended that one differential input be tied to TVBB or RVBB (VBB outputs, both are equivalent) and the other utilized so as to produce the desired logic function. The VBB outputs are high impedance voltage sources capable of 50µA current drive only and must, therefore, not be used as DC bias in an AC coupled configuration. Figure 12 shows some examples of ECL input and output connections.

Figure 12. ECL Input and Output Applications



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PIN DESCRIPTIONS

Receive Serial Data [RSDP/N]—Differential ECL Input. ECL level serial data stream signals, normally connected to an external clock and data recovery device or directly to an optical receiver module having integral clock and data recovery. The RSD inputs are sampled on the rising edge of RSCLKP.

Receive Serial Clock [RSCLKP/N]—Differential ECL Input. ECL level signals used as the receive master clock for the STPC device. RSCLK may be either a 622, 311, or 155 MHz clock, depending on the operating mode of the STPC. POCLK is derived from RSCLK when diagnostic loopback is not enabled. When diagnostic loopback is enabled (RDLEB) and internal loopback is disabled (ILEB), POCLK is derived from the external DLCLK input. When diagnostic loopback is enabled (RDLEB), transmit diagnostic loopback is enabled (TDLEB), and internal loopback is enabled (ILEB), POCLK is derived from the internal DLCLK output. During transitions, the jitter induced on POCLK is typically less than 1/8 UI.

Diagnostic Loopback Data Input [RDLDP/N]—Differential ECL Input. ECL level serial data stream signals, normally connected to a companion device or to the STPC itself for diagnostic loopback purposes. The RDLD inputs are sampled on the rising edge of RDLCLKP.

Diagnostic Loopback Clock Input [RDLCLKP/N]—Differential ECL Input. ECL-level signals, normally connected to a companion device or to the STPC itself for diagnostic loopback purposes. RDLCLK may be either a 622, 311, or 155 MHz clock, depending on the operating mode of the STPC. POCLK is derived from RDLCLK when diagnostic loopback is enabled and internal loopback is disabled (ILEB). POCLK is derived from the internal RDLCLK when diagnostic loopback is enabled, transmit diagnostic loopback is enabled (TDLEB) and internal loopback is enabled (ILEB). When diagnostic loopback is disabled, POCLK is derived from RSCLK. During transitions, the jitter induced on POCLK is typically less than 1/8 UI.

Receive Bias Voltage Output [RVBB]—Analog Output. Provided to facilitate configuring differential inputs to accept single-ended ECL signals. RVBB is approximately -1.3V and should be connected to each unused differential input in order to set the switching threshold of the other input when it is used for single-ended reception. RVBB should not be loaded in any manner except for connections to STPC ECL inputs and optional 0.1uF capacitor decoupling to ground.

Receive Diagnostic Loopback Enable [RDLEB]—TTL Input. Selects diagnostic loopback. When high, the STPC device uses the receive serial data and clock inputs (RSD and RSCLK). When low, the STPC device uses the diagnostic loopback data and clock inputs. The Internal Loopback (ILEB) pin selects between the external loopback data and clock (RDLD and RDLCLK) or the internal loopback data and clock. RDLEB has an integral pull-up resistor.

Out of Frame [OOF]—TTL Input. Used to enable framing pattern detection logic in the STPC. The framing pattern detection logic is enabled by a rising edge on OOF, and remains enabled until frame boundary is detected or when OOF is set low, which ever is longer. OOF may be an asynchronous signal but must have a minimum pulse width of 6 ns. OOF has an integral pull-up resistor.

Loss of Signal [LOSP/N]—Differential ECL Input. Differential ECL inputs that are used by the external optical receiver module to indicate a loss of received optical power. When LOS is high, the data on the received serial data (RSD) pins will be squelched. The effect is equivalent to externally forcing the RSD inputs to an all zeros condition (after CMI decoding if RCMI is enabled). The LOS input is disabled when the Diagnostic Loopback (DLEB) pin is low. When LOS is low, data on the RSD pin will be processed normally.

Receive CMI Enable [RCMI]—TTL Input. Used to enable the CMI decoder. To configure the operating mode of the device as 622 Mbit/s (STS-12 or STM-4) or 155 Mbit/s (STS-3 or STM-1) one must set the RCMI input low and apply 622 MHz or 155 MHz clocks as appropriate. To select 155 Mbit/s CMI operation (STS-3 electrical) one must set the RCMI input high and apply a 311 MHz clock. RCMI has an integral pull-up resistor.

ATM Framing Enable [ATMFENB]—TTL Input. Used to enable the alternate framing approach used for 139 Mbit/s ATM streams. When ATMFENB is high, the STPC frames to three A1 bytes followed by three A2 bytes as required for SONET/SDH. When ATMFENB is low, the STPC frames to a single A1 byte followed by a single A2 byte. ATMFENB has an integral pull-up resistor.

Receive Master Reset [RRSTB]—TTL Input. Pulling RRSTB low will reset the receive side (serial to parallel section) of the device. RRSTB must have a minimum pulse width of 6 ns. After reset, frame boundary detection is disabled until OOF goes high. RRSTB has an integral pull-up resistor.

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Line Loopback Data Output [LLDP/N]—Differential ECL Output. ECL level signals that carry a regenerated version of the receive serial data (RSD) input in normal mode. The LLDO pins carry the diagnostic loopback data input (RDLD) when in receive diagnostic loopback mode (RDLEB set low) and the internal loopback mode disabled (ILEB set high). The LLD pins carry the STPC transmit serial data (TSD) outputs when in receive diagnostic loopback mode (RDLEB set low), with the transmit diagnostic loopback enabled (TDLEB set low), and the internal loopback mode enabled (ILEB set low). LLD is updated on the falling edge of LLCLK. The LLD outputs are held in the inactive state, except when RLLEB is low.

Line Loopback Clock Output [LLCLKP/N]—Differential ECL Output. ECL level signals, phase aligned with the line loopback data output (LLD) signals. LLCLK is a buffered version of the receive serial clock (RSCLK) input in normal mode. The LLCLK is the diagnostic loopback clock input (RDLCLK) when in receive diagnostic loopback mode (RDLEB set low) and the internal loopback disabled (ILEB set high). The LLCLK carries the STPC transmit serial data clock (TSCLK) output when in receive diagnostic loopback mode (RDLEB set low), with the transmit diagnostic loopback enabled (TDLEB set low) and the internal loopback enabled (ILEB set low). The LLCLK outputs are held in the inactive state, except when RLLEB is low.

Receive Line Loopback Enable [RLLEB]—TTL Input. Selects line loopback. When high, the STPC device disables the line loopback outputs to save power and reduce noise (LLD and LLCLK forced to logic 0). When low, the STPC device enables the line loopback data and clock outputs (LLD and LLCLK active). RLLEB has an integral pull-up resistor.

Parallel Output Data [POUT<7:0>]—TTL/CMOS Output. A 77.76 Mbyte/s or 19.44 Mbyte/s byte serial stream, aligned to the parallel output clock (POCLK). POUT[7] is the most significant bit (corresponding to bit 1 of each PCM word, the first bit received). POUT[0] is the least significant bit (corresponding to bit 8 of each PCM word, the last bit received). POUT[7:0] is updated on the falling edge of POCLK.

Line Code Violation [LCV]—TTL/CMOS Output. Set high to indicate that one or more bits of the byte currently presented on POUT[7:0] contains a CMI line code violation. LCV is only active in CMI mode. LCV is updated on the falling edge of POCLK.

Frame Pulse [FP]—TTL/CMOS Output. Indicates frame boundaries in the incoming data stream (RSD). If framing pattern detection is enabled, as controlled by the out of frame (OOF) input, FP pulses high for one POCLK cycle when any 48-bit sequence matching the framing pattern is detected on the RSD inputs. When framing pattern detection is disabled, FP pulses high when the incoming data stream, after byte alignment, matches the framing pattern. FP is updated on the falling edge of POCLK. When ATMFEB is low, the framing pattern detector only looks for a matching 16-bit sequence.

Parallel Output Clock [POCLK]—TTL/CMOS Output. A 77.76 MHz or 19.44 MHz, 50% duty cycle, byte rate output clock that is aligned to the POUT[7:0] byte serial output data. POUT[7:0], LCV and FP are updated on the falling edge of POCLK. When RCMI is low, POCLK is equal to RSCLK (or RDLCLK) divided by eight. When RCMI is high, POCLK is equal to RSCLK (or RDLCLK) divided by sixteen.

Transmit Serial Data [TSDP/N]—Differential ECL Output. ECL level serial data stream signals, normally connected to an optical transmitter module. The TSD outputs are updated on the falling edge of TSCLK+. When line loopback mode is enabled (TLLEB set low) and with internal loopback disabled (ILEB set high), TSD is derived from TLLD. When line loopback mode is enabled (TLLEB set low), with receive line loopback enabled (RLLEB set low), and internal loopback enabled (ILEB set low), TSD is derived from the receive serial data (RSD) input.

Transmit Serial Clock Input [TSCLKIP/N]—Differential ECL Input. ECL level signals, normally used as the master clock for the parallel to serial converter portion of the STPC device. TSCLK may be either a 622, 311, or 155 MHz clock, depending on the operating mode of the STPC. PCLK is derived from TSCLK.

Transmit Serial Clock [TSCLKP/N]—Differential ECL Output. ECL level signals, phase aligned with the transmit serial data (TSD) output signals. TSCLK may be either a 622, 311, or 155 MHz clock, depending on the operating mode of the STPC. TSCLK is derived from TSCLKI in normal mode. When transmit line loopback mode is enabled (TLLEB set low) and with internal loopback disabled (ILEB set high), TSCLK is derived from TLLCLK. When transmit line loopback mode is enabled (TLLEB set low), with receive line loopback enabled (RLLEB set low) and with internal loopback enabled (ILEB set low), TSCLK is derived from receive serial clock (RSCLK) input.

Line Loopback Data Input [TLLDP/N]—Differential ECL Input. ECL level serial data stream signals, normally connected to a companion device or to the STPC itself for line loopback purposes. The TLLD inputs are sampled on the rising edge of TLLCLKP.

Line Loopback Clock Input [TLLCLKP/N]—Differential ECL Input. ECL level signals, normally connected to a companion device or to the STPC itself for line loopback purposes. TLLCLK may be either a 622, 311, or 155 MHz clock, depending on the operating mode of the STPC.

Transmit Bias Voltage Output [TVBB]—Analog Output. Provided to facilitate configuring differential inputs to accept single-ended ECL signals. TVBB is approximately -1.3V and should be connected to each unused, differential input in order to set the switching threshold of the other input when it is used for single-ended reception. TVBB should not be loaded in any manner except for connections to STPC ECL inputs and optional 0.1uF decoupling to ground.

Transmit Line Loopback Enable [TLLEB]—TTL Input. Selects transmit line loopback. When high, the STPC device sources data and clock to the transmit serial data and clock from the parallel to serial converter using its own timing (PIN[7:0], PICLK and TSCLKI). When low and with the internal loopback disabled (ILEB set high), the STPC device sources data and clock to the transmit serial data and clock directly from the line loopback data and clock inputs (TLLD and TLLCLK). When low, with the receive line loopback enabled (RLLEB set low), and with the internal loopback enabled (ILEB set low), the STPC device sources data and clock to the transmit serial data and clock directly from the receive serial data and clock inputs (RSD and RSCLK). TLLEB has an integral pull-up resistor.

Synchronization Enable [SYNC]—TTL Input. The active high (SYNC) input enables the timing generator to invert the internal byte transfer clock if transfers from the PIN[7:0] input holding register are occurring less than one bit period before or after clocking new data into the holding register. The SYNC pin is an asynchronous input which is sampled by and synchronized by TSCLKI. The SYNC pulse should be high for a minimum of two TSCLKI clock cycles. SYNC has an integral pull-up resistor.

Transmit CMI Enable [TCMI]—TTL Input. Used to enable the CMI decoder. To configure the operating mode of the device as 622 Mbit/s (STS-12 or STM-4) or 155 Mbit/s (STS-3 or STM-1) one must set the TCMI input low and apply 622 MHz or 155 MHz clocks as appropriate. To select 155 Mbit/s CMI operation (STS-3 electrical) one must set the TCMI input high and apply a 311 MHz clock. TCMI has an integral pull-up resistor.

Transmit Master Reset [TRSTB]—TTL Input. Pulling TRSTB low will reset the parallel to serial converter portion of the STPC device. TRSTB must have a minimum pulse width of 6 ns. After reset, the internal transfer of the input parallel data to the serial shift register is aligned such that the transfer occurs on the falling edge of PICLK (PICLK samples the data on the rising edge). This guard bands against a phase alignment event. TRSTB has an integral pull-up resistor.

Diagnostic Loopback Data Output [DLDP/N]—Differential ECL Output. ECL level signals are a duplicated copy of the transmit serial data (TSD) output in normal mode and continue to reflect the output of the parallel to serial converter when in transmit line loopback mode (TLLEB set low). DLD is updated on the falling edge of DLCLKP. The DLD outputs are held in the inactive state, except when TDLEB is low.

Diagnostic Loopback Clock Output [DLCLKP/N]—Differential ECL Output. ECL level signals, phase aligned with the diagnostic loopback data output (DLD) signals. DLCLK is a buffered version of the transmit serial clock input (TSCLKI). The DLCLK outputs are held in the inactive state, except when TDLEB is low.

Transmit Diagnostic Loopback Enable [TDLEB]—TTL Input. Selects transmit diagnostic loopback. When high, the STPC device disables the diagnostic loopback outputs to save power and reduce noise (DLD and DLCLK). When low, the STPC device enables the diagnostic loopback data and clock outputs (DLD and DLCLK). TDLEB has an internal pull-up resistor.

Parallel Input Data [PIN <7:0>]—TTL Input. This bus is a 77.76 Mbyte/s or 19.44 Mbyte/s byte serial stream, aligned to the parallel input clock (PICLK). PIN[7] is the most significant bit (corresponding to bit 1 of each PCM word, the first bit transmitted). PIN[0] is the least significant bit (corresponding to bit 8 of each PCM word, the last bit transmitted). PIN[7:0] is sampled on the rising edge of PICLK.

Parallel Input Clock [PICLK]—TTL Input. A 77.76 MHz or 19.44 MHz nominally 50% duty cycle input clock, to which PIN[7:0] is aligned. PICLK is used to transfer the data on the PIN inputs into a holding register in the parallel to serial converter. The rising edge of PICLK samples PIN[7:0].

Diagnostic Line Code Violation [DLCV]—TTL Input. A rising edge on the DLCV input causes a CMI code violation in the serial output data. DLCV is an asynchronous input, sampled and synchronized by TSCLKI with a minimum pulse width of four TSCLKI periods. DLCV has a integral pull-up resistor.

Phase Alignment Event [PAE]—TTL/CMOS Output. This signal pulses high during each PCLK cycle for which there is less than one bit period between the internal byte clock and PICLK timing domains. PAE is updated on the falling edge of the PCLK output.

Parallel Clock [PCLK]—TTL/CMOS Output. This output is a reference byte clock generated by dividing TSCLKI by eight in normal mode, or by sixteen when in CMI mode. It is normally used to coordinate byte wide transfers between upstream logic and the STPC device. PAE is updated on the falling edge of PCLK.

Internal Loopback Enable [ILEB]—TTL Input. Selects internal line loopback. When high, the STPC device sources the loopback's clock and data from the external loopback pins (RDLCLK, RDLD). When low, the STPC device uses the internal loopback's clock and data inputs. ILEB has an integral pull-up resistor.

ECL to TTL [ECLIP/N]—Differential ECL Input. Used to convert a differential ECL signal to a single-ended TTL output signal (TTLO).

TTL [TTLO]—TTL Output. The TTL output pin is the converted ECL signal coming from the ECLI differential input pins.

TTL to ECL [TTLI]—TTL Input. The TTL to ECL pin is a TTL input that is used to convert a single-ended TTL signal to a differential ECL output signal (ECLO).

ECL [ECLOP/N]—Differential ECL Output. The ECL output pins are the converted TTL input signal coming from the TTLI input pin.

Absolute Maximum Ratings

Parameter	Min	Typ	Max	Unit
Case Temperature under Bias	-55		125	°C
Junction Temperature under Bias	-55		150	°C
Storage Temperature	-65		150	°C
Voltage on VCC with Respect to GND	-0.5		7.0	V
Voltage on VEE with Respect to GND	0.5		-8.0	V
Voltage on any TTL Input Pin	-0.5		5.5	V
Voltage on any ECL Input Pin	0		-3.0	V
TTL/CMOS Output Sink Current			20	mA
TTL/CMOS Output Source Current			10	mA
High Speed ECL Output Source or sink current			50	mA
Static Discharge Voltage		500		V

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Case Temperature under Bias	-40		85	°C
Junction Temperature under Bias	-10		125	°C
Voltage on VCC with Respect to GND	4.75	5.0	5.25	V
Voltage on VEE with Respect to GND[1]	-4.2	-4.5/-4.8	-5.46	V
Voltage on any TTL Input Pin	0		Vcc	V
Voltage on any ECL Input Pin	0		-2.0	V
TTL/CMOS Output Sink Current			8	mA
TTL/CMOS Output Source Current			1	mA
ECL Output Source Current			25	mA

1. VEE (min) = -4.2V for Ambient Temperature ≥ 0°C, -4.5V for Ambient Temperature < 0°C.

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TTL INPUT/OUTPUT DC CHARACTERISTICS[1]

(T_A = -40°C to +85°C, V_{CC} = 5 V ±5%, V_{EE} = -4.5 V ±7% or -5.2 ± 5%)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IL}[2]	Input LOW Voltage	Guaranteed Input LOW Voltage for all inputs		0.8	Volts
V_{IH}[2]	Input HIGH Voltage	Guaranteed Input HIGH Voltage for all inputs	2.0		Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V	-400.0		uA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V		50.0	uA
I_I	Input HIGH Current at Max VCC	V_{CC} = MAX, V_{IN} = 5.25V		1.0	mA
I_{OS}	Output Short Circuit Current	V_{CC} = MAX, V_{OUT} = 0.5V	-100.0	-25.0	mA
I_{OZL}	Output Three-State Current LOW	V_{CC} = MAX, V_{OL} = 0.4V	-50.0	50.0	uA
I_{OZH}	Output Three-State Current HIGH	V_{CC} = MAX, V_{OH} = 2.4V	-50.0	50.0	uA
V_{IK}	Input Clamp Diode Voltage	V_{CC} = MIN, I_{IN} = -18mA	-1.2		Volts
V_{OL}	TTL Output LOW Voltage	V_{CC} = MIN, I_{OL} = 8mA		0.5	Volts
V_{OH}	TTL Output HIGH Voltage	V_{CC} = MIN, I_{OH} = -20mA	2.4		Volts

1. These conditions will be met with an airflow of 400 LFPM.
2. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.

ECL INPUT/OUTPUT DC CHARACTERISTICS[1]

(T_A = -40°C to +85°C, V_{CC} = 5 V ±5%, V_{EE} = -4.5 V ±7% or -5.2 ± 5%)

Symbol	Parameter	Conditions	Signal Name	Min	Max	Unit
V_{IL}	Input LOW Voltage	Guaranteed Input LOW Voltage for all differential inputs		-2.00	-0.70	Volts
V_{IH}	Input HIGH Voltage	Guaranteed Input HIGH Voltage for all differential inputs		-1.75	-0.45	Volts
V_{ID}	Input DIFF Voltage	Guaranteed Input DIFF Voltage for all differential inputs		0.25	1.40	Volts
I_{IL}	Input LOW Current	V_{EE} = MAX, V_{DIFF} = 0.5V		-1.00	20.00	uA
I_{IH}	Input HIGH Current	V_{EE} = MAX, V_{DIFF} = 0.5V		-1.00	20.00	uA
V_{OL}	Output LOW Voltage	50Ω to -2V termination		-2.00	-1.50	Volts
V_{OH}	Output HIGH Voltage	50Ω to -2V termination		-1.11	-0.62	Volts

1. These conditions will be met with an airflow of 400 LFPM.

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STPC INPUT TIMING

(T_c = -40°C to T_c +85°C, V_{cc} = 5 V ±5%, V_{EE} = -4.5 V ±7% or -5.2V ± 5%)

Symbol	Parameter	Min	Max	Unit
	RSCLK Freq. (Normally 622, 311, or 155 MHz)		640	MHz
	RSCLK Duty Cycle	33	67	%
tS_{RSD}	RSD to RSCLK Set-up Time	400		ps
tH_{RSD}	RSCLK to RSD Hold Time	200		ps
	RDLCLK Freq. (Normally 622, 311, or 155 MHz)		640	MHz
	RDLCLK Duty Cycle	33	67	%
tS_{RDLD}	RDLD to RDLCLK Set-up Time	400		ps
tH_{RDLD}	RDLCLK to RDLD Hold Time	200		ps
tWOOF	OOF High Pulse Width	6		ns
tW_{RSTB}	RRSTB Low Pulse Width	6		ns
	TSCLKI Freq. (Normally 622, 311, or 155 MHz)		640	MHz
	TSCLKI Duty Cycle	33	67	%
	PICLK Freq. (Normally 77.76 or 19.44 MHz, must be divided down version of TSCLKI)	33	67	%
	PICLK Duty Cycle	33	67	%
tS_{PIN}	PIN[7:0] Set-up Time w.r.t. PICLK	1		ns
tH_{PIN}	PIN[7:0] Hold Time w.r.t. PICLK	1		ns
	TLLCLK Freq. (Normally 622, 311, or 155 MHz)		640	MHz
	TTLCLKI Duty Cycle	33	67	%
tS_{TLLD}	TLLDI to TLLCLK Set-up Time	400		ps
tH_{TLLD}	TLLCLKI to TLLD Hold Time	200		ps
tW_{SYNC}	SYNC High Pulse Width	2 TSCLKI		periods
tW_{DLCV}	DLCV High Pulse Width	4 TSCLKI		periods
tW_{RSTB}	TRSTB Low Pulse Width	6		ns

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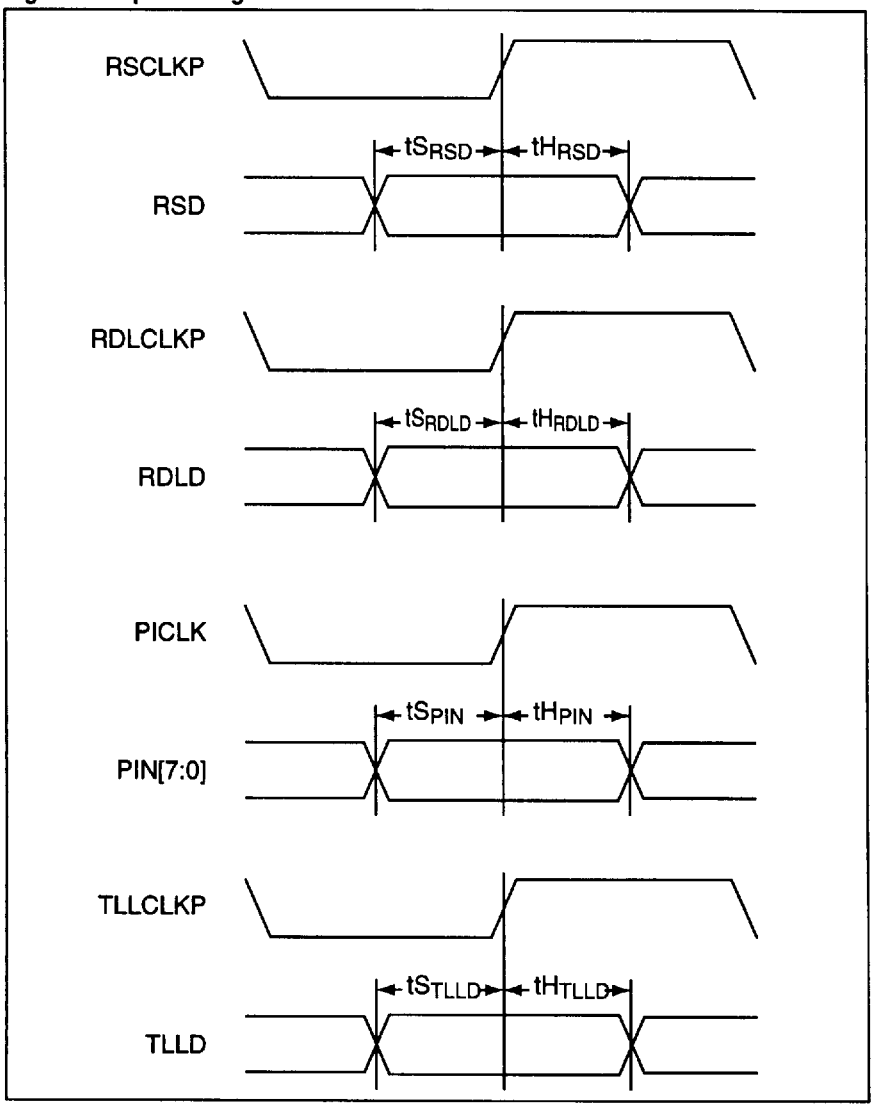
Figure 13. Input Timing



Notes on Input Timing:

1. When a set-up time is specified between an ECL data input and an ECL clock input, the set-up time is the time in picoseconds from the crossover point of the differential data input to the crossover point of the differential clock input.
2. When a hold time is specified between an ECL data input and an ECL clock input, the hold time is the time in picoseconds from the crossover point of the differential clock input to the crossover point of the differential data input.
3. When a set-up time is specified between a TTL data input and a TTL clock input, the set-up time is the time in picoseconds from the 1.4V point of the data input to the 1.4V point of the clock input.
4. When a hold time is specified between a TTL data input and a TTL clock input, the hold time is the time in picoseconds from the 1.4V point of the clock input to the 1.4V point of the data input.

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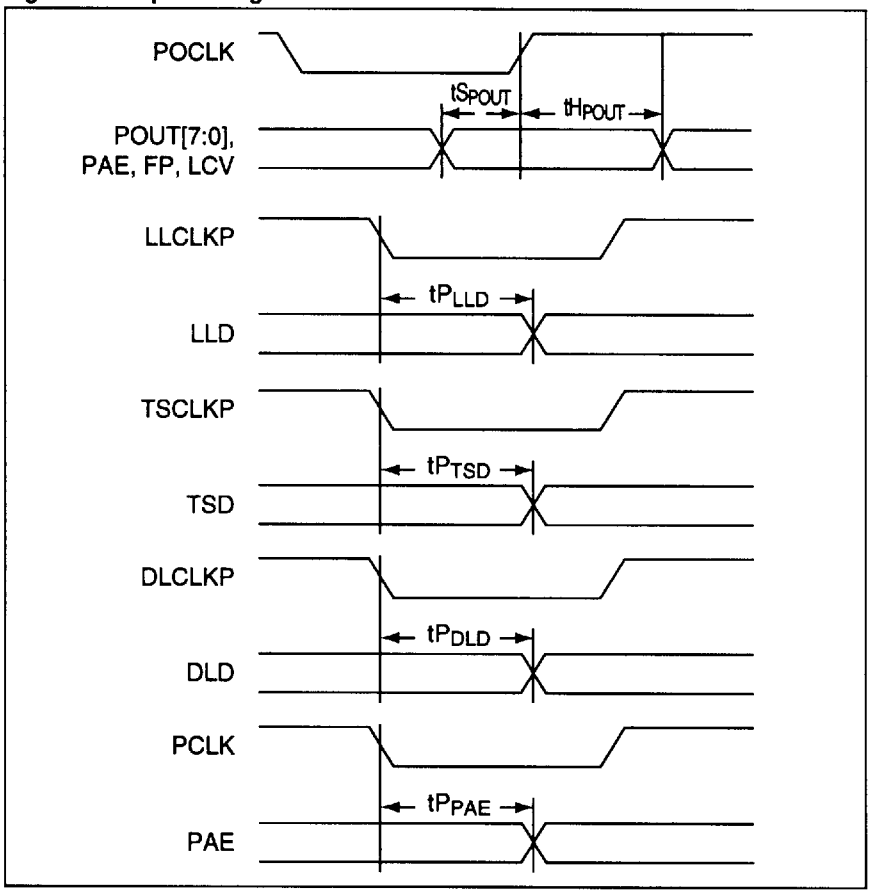
STPC OUTPUT TIMING

Symbol	Parameter	Min	Max	Unit
	POCLK Freq. (Normally 77 or 19 MHz)		80	MHz
	POCLK Duty Cycle	40	60	%
tS_{POUT}	POUT[7:0], FP, LCV and PAE Set-up Time w.r.t. POCLK	3		ns
tH_{POUT}	POUT[7:0], FP, LCV and PAE Hold Time w.r.t. POCLK	2		ns
	LLCLK Frequency (Follows RSCLK or DLCLK)		640	MHz
	LLCLK Duty Cycle (up to 5% additive distortion)	28	72	%
tP_{LLD}	LLCLK Low to LLD Valid Propagation Delay	-350	350	ps
	TSCLK Freq. (Normally 622, 311, or 155 MHz)		640	MHz
	TSCLK Duty Cycle (up to 5% additive distortion	28	72	%
tP_{TSD}	TSCLK Low to TSD Valid Propagation Delay	-350	350	ps
	DLCLK Freq. (Normally 622, 311, or 155 MHz)		640	MHz
	DLCLK Duty Cycle	33	67	%
tP_{DLD}	DLCLK Low to DLD Valid Propagation Delay	-350	350	ps
	PCLK Freq. (Normally 77.76 or 19.44 MHz)		80	MHz
	PCLK Duty Cycle	40	60	%

Figure 14. Output Timing



Notes on Output Timing:

1. Output propagation delay time of TTL outputs is the time in picoseconds from the 1.4 V point of the reference signal to the 1.4V point of the output.
2. Maximum output propagation delays of TTL outputs are measured with a 50 pF load on the outputs.
3. Output propagation delay time of ECL outputs is the time in picoseconds from the cross-over point of the reference signal to the cross-over point of the output.
4. Maximum output propagation delays of ECL outputs are measured with a 50Ω load to -2V in parallel with a 10 pF load.
5. When a set-up time is specified between a TTL data input and a TTL clock input, the set-up time is the time in picoseconds from the 1.4V point of the data input to the 1.4V point of the clock input.
6. When a hold time is specified between a TTL data input and a TTL clock input, the hold time is the time in picoseconds from the 1.4V point of the clock input to the 1.4V point of the data input.

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Pin Assignment

Pin No.	Name	Pin No.	Name	Pin No.	Name	Pin No.	Name
1	NC	31	NC	61	NC	91	NC
2	NC	32	TTLVCC	62	TTLGND	92	TTLVCC
3	TTLGND	33	ECLIOVCC	63	ECLIOVCC	93	ECLIOVCC
4	ECLIOVCC	34	TTLI	64	ILEB	94	TVBB2
5	ECLIP	35	PAE	65	TLLCLKN	95	POUT6
6	ECLIN	36	PCLK	66	TLLCLKP	96	POUT5
7	RVBB	37	ECLVCC	67	ECLVCC	97	ECLVCC
8	ECLVCC	38	ECLVEE	68	VE	98	ECLVEE
9	VE	39	TRSTB	69	TLLDN	99	POUT4
10	LOSN	40	TCMI	70	TLLDP	100	POUT3
11	LOSP	41	TDLEB	71	RDLDP	101	POUT2
12	RSCLKN	42	TLLEB	72	RDLDN	102	RVBB2
13	RSCLKP	43	DLCV	73	RDLCLKP	103	POUT1
14	RSDN	44	SYNC	74	RDLCLKN	104	POUT0
15	RSDP	45	ECLIOVCC	75	ECLIOVCC	105	POCLK
16	ECLIOVCC	46	PICLK	76	DLCLKN	106	ECLIOVCC
17	TSCLKIP	47	PIN7	77	DLCLKP	107	OOF
18	TSCLKIN	48	PIN6	78	DLDN	108	ATMFENB
19	TSDP	49	PIN5	79	DLDP	109	RCMI
20	TSDN	50	PIN4	80	LLDP	110	RRSTB
21	TSCLKP	51	PIN3	81	LLDN	111	RDLEB
22	TSCLKN	52	DNC	82	VE	112	RLLEB
23	VE	53	ECLVEE	83	ECLVCC	113	ECLVEE
24	ECLVCC	54	ECLVCC	84	LLCLKP	114	ECLVCC
25	ECLOP	55	PIN2	85	LLCLKN	115	FP
26	ECLON	56	PIN1	86	POUT7	116	LCV
27	TVBB	57	PIN0	87	ECLIOVCC	117	TTLO
28	ECLIOVCC	58	ECLIOVCC	88	TTLGND	118	ECLIOVCC
29	TTLGND	59	TTLVCC	89	NC	119	TTLVCC
30	NC	60	NC	90	NC	120	NC

Power Supply Connections:

TTLVCC = +5V
ECLVEE = -5.2V
VE = -5.2V
TTLGND = 0V
ECLVCC = 0V
ECLIOVCC = 0V
NC = No Connect
DNC = Do Not Connect (leave floating)

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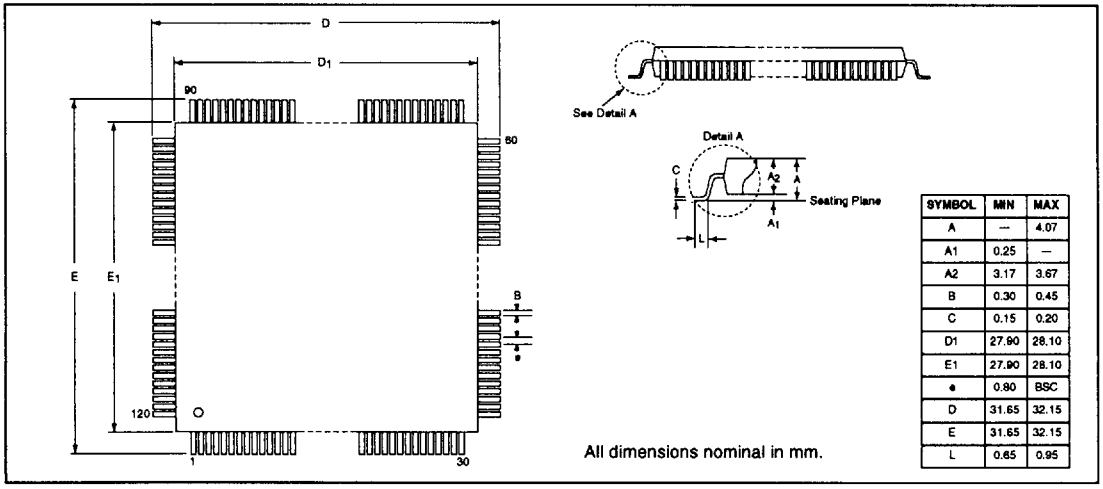
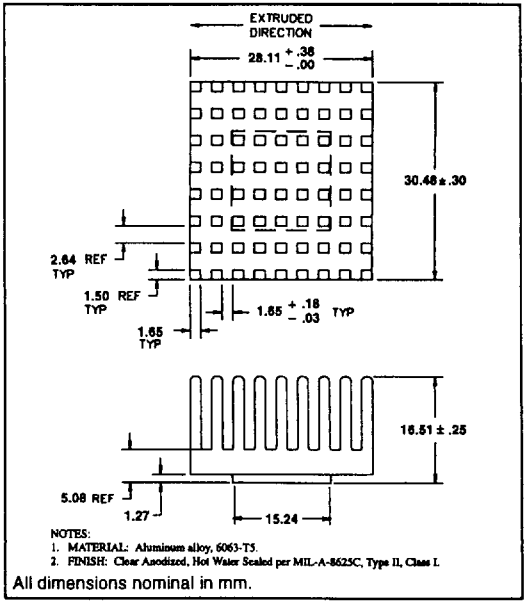
Figure 15. 120-Pin TEP Package



SYMBOL	MIN	MAX
A	—	4.07
A1	0.25	—
A2	3.17	3.67
B	0.30	0.45
C	0.15	0.20
D1	27.90	28.10
E1	27.90	28.10
e	0.80	BSC
D	31.65	32.15
E	31.65	32.15
L	0.65	0.95

All dimensions nominal in mm.

Figure 16. DW0045-17 Heatsink



All dimensions nominal in mm.

Thermal Management

Maximum VEE Supply	Power	Θja Still Air w/DW0045-17 Heatsink	Max Still Air[1] w/DW0045-17 Heatsink	Required Air[2] w/DW0045-17 Heatsink
-4.8V	3.78W	11.9°C/W	85°C	N/A
-5.46V	4.53W	11.9°C/W	76°C	100 LFPM

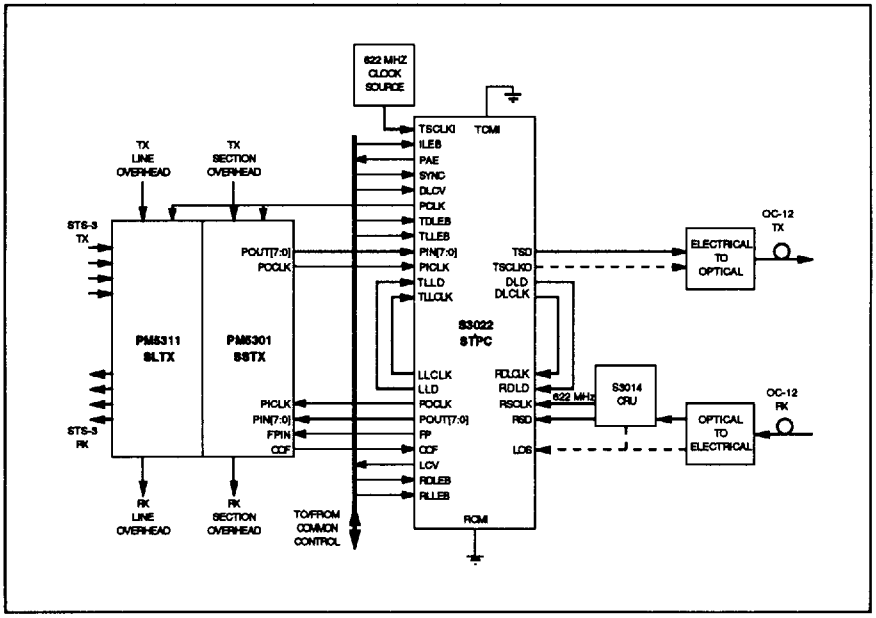
Notes:
1. Max ambient temperature permitted in still air to maintain $T_j \leq 130°C$.
2. Airflow required in 85°C ambient conditions to maintain $T_j \leq 130°C$.

APPLICATION EXAMPLES

622 Mbit/s Interface

The PM5318 STPC device is designed to interface seamlessly with the PM5301 SSTX or PM5312 STTX devices to make a 622 Mbit/s transport interface. Figure 17 shows an STPC connected to an STTX on the equipment side and electrical to optical converters on the line side to realize the core of a typical OC-12 or STM-4 transmission system. Similar connections are used to implement an ATM interface using the PM5355 SUNI-622 device.

Figure 17. OC-12/STM-4 Application



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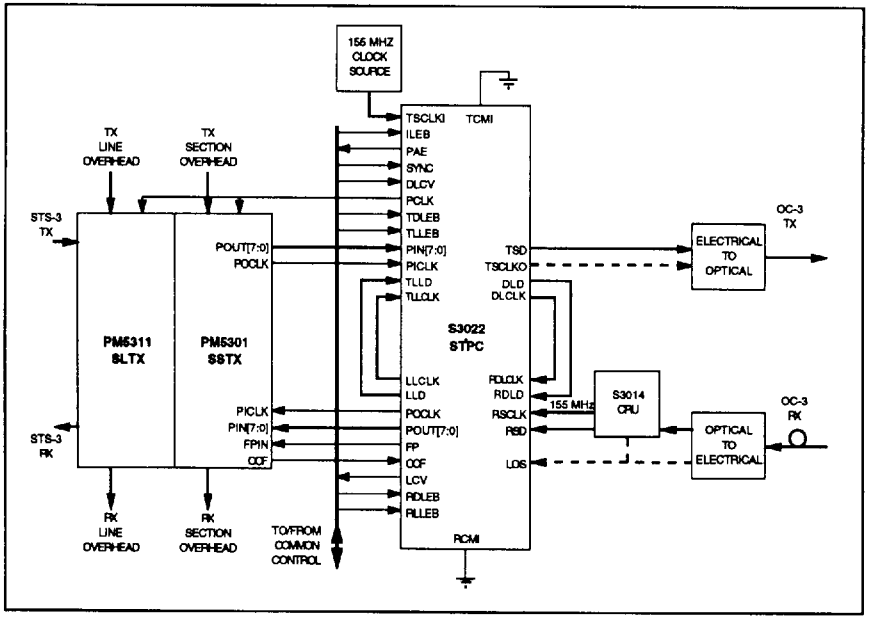
155 Mbit/s Interface

The PM5318 STPC device is designed to interface seamlessly with the PM5301 SSTX or PM5312 STTX devices to make a 155 Mbit/s transport interface. Figure 18 shows the STPC connected to an STTX on the equipment side and electrical to optical converters on the line side to realize the core of a typical OC-3 or STM-1 transmission system.

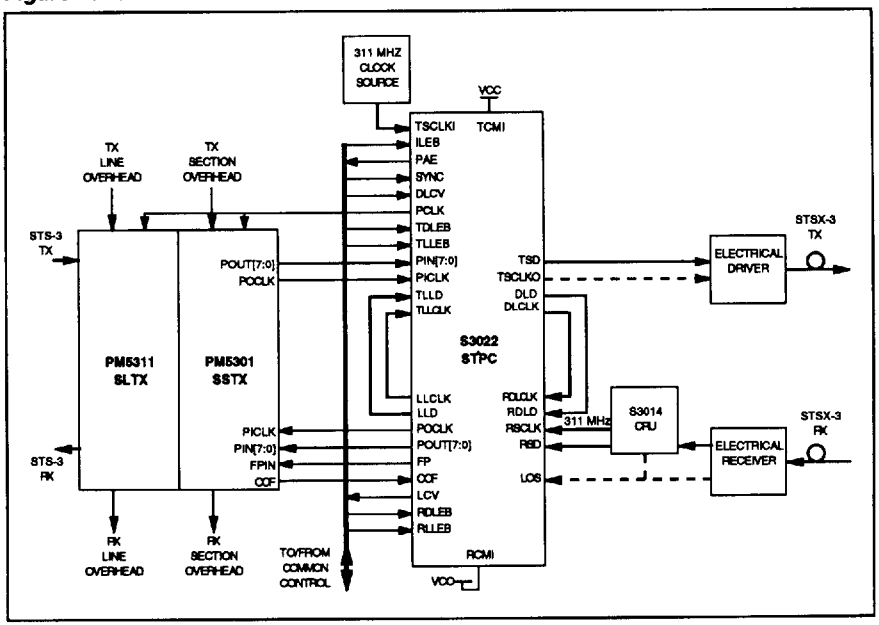
Figure 18. OC-3/STM-3 Application



155 Mbit/s CMI Electrical Interface

With the STPC device optioned for CMI coded STS-3/STM-1, an electrical transmission system using co-axial cable can be implemented as shown in Figure 19. In this case, the interface operates from a 311 MHz clock. TSD would be coupled through a line driver and transformer to a co-axial cable through a transformer and comparators that would slice the incoming signal based on peak detection.

Figure 19. CMI Electrical Interface



Ordering Information

S–Commercial/Industrial	3022	A–120 TEP w/ Heatsink unattached
X	X	X
Grade	Part Number	Package