# PWR-INT301

## High-side Driver IC

### Floating Inputs
### Floating High-side Drive

POWER INTEGRATIONS, INC.®

## Product Highlights

**Floating Control Inputs**
- Connects directly to PWR-INT300 HSD outputs
- No external level translators or transformers required

**Gate Drive Output for an External MOSFET or IGBT**
- Provides 1 A sink/500 mA source current
- Can drive MOSFET or IGBT gate at up to 20 V
- Floating source for driving high-side N-channel MOSFET or IGBT
- External MOSFET or IGBT allows flexibility in design

**Built-in Protection Circuits**
- Logic inputs include noise immunity circuitry
- Undervoltage lockout

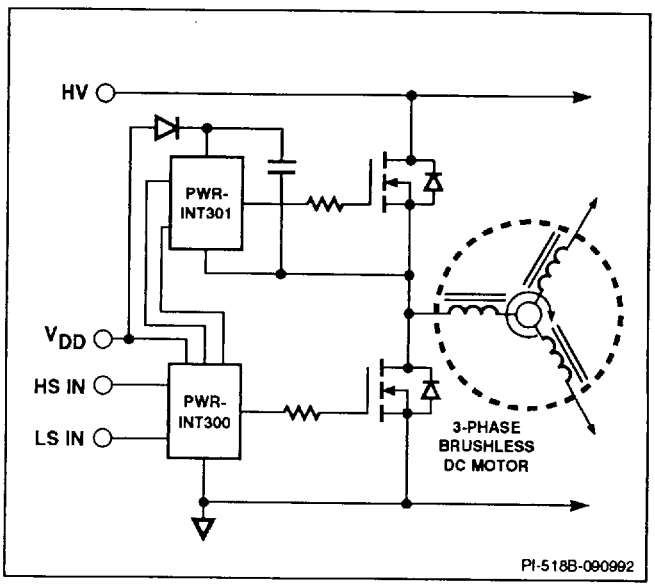


*Figure 1. Typical Application.*

## Description

The PWR-INT301 high-side driver IC provides gate drive for an external high-side MOSFET or IGBT switch. When used in conjunction with the PWR-INT300 low-side drivers, the PWR-INT301 provides a simple, cost-effective interface between low-voltage control logic and high-voltage MOSFET or IGBT switches.

Built-in circuitry shared between the PWR-INT301 and the PWR-INT300 provides noise immunity. The PWR-INT301 is powered from a ground-referenced low-voltage supply. It derives a floating supply from this rail by using a simple bootstrap technique to provide adequate gate drive for the external MOSFET or IGBT.

Applications include motor drives and half and full bridge power supplies.

The PWR-INT301 is available in an 8-pin plastic DIP package.

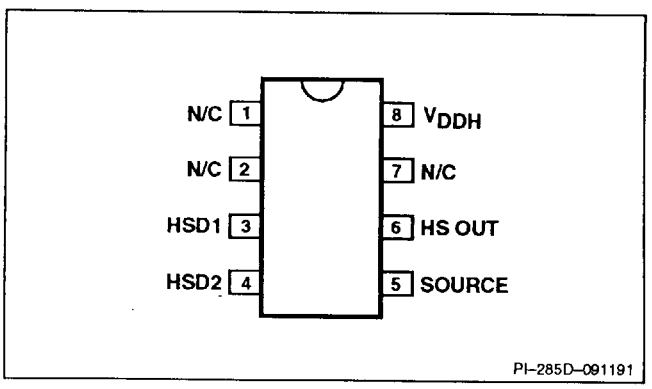


*Figure 2. Pin Configuration.*

| ORDERING INFORMATION | | |
|---|---|---|
| PART NUMBER | PACKAGE | TEMP RANGE |
| PWR-INT301PFI | 8-pin PDIP | -40 to 85°C |

411 Clyde Avenue
Mountain View, California, 94043
Business Phone: (415) 960-3572
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**PRELIMINARY**

November 1993

7289229 0000645 181 PIN

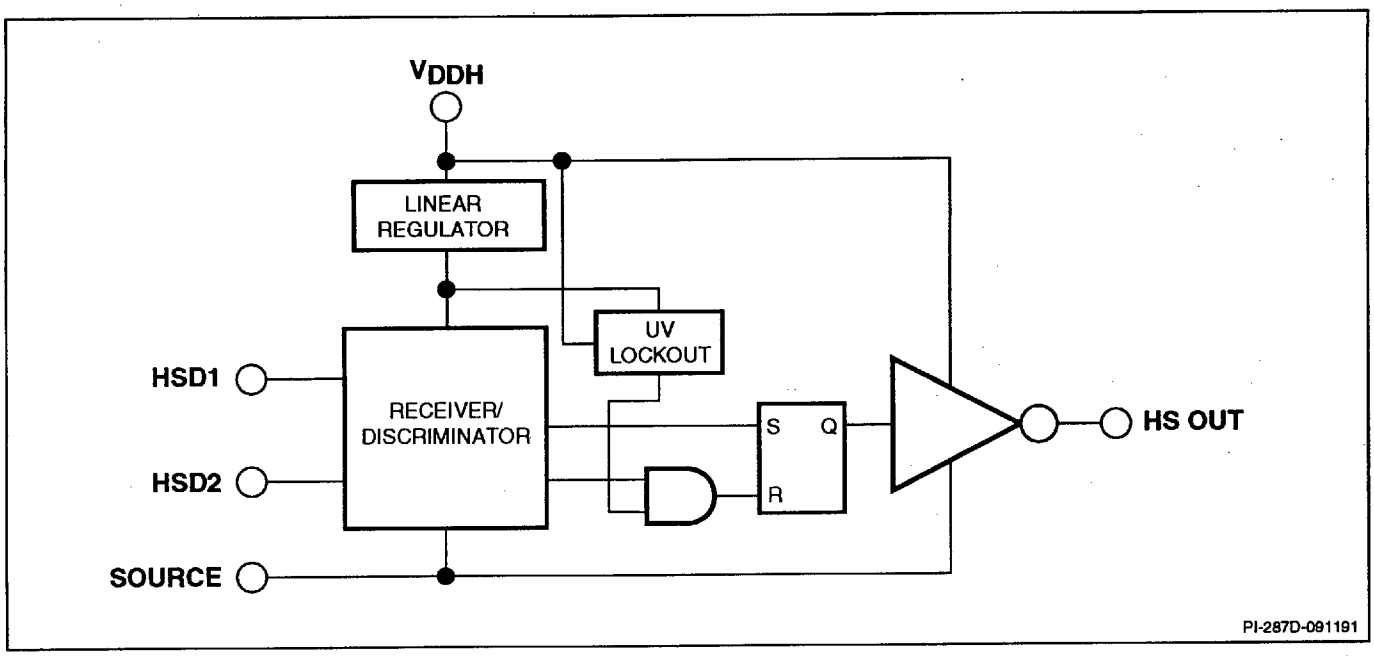



*Figure 3. Functional Block Diagram of the PWR-INT301.*

## PWR-INT301 Functional Description

**5 V Regulator**
The 5 V linear regulator circuit provides the supply voltage for the receiver/ discriminator circuit and control logic. This allows the logic section and the driver circuitry to utilize separate supply voltages without the need of two external supplies.

**Undervoltage Lockout**
The undervoltage lockout circuit disables the HS OUT pin until the $V_{DDH}$ power supply has exceeded 9.25 V (typical), guaranteeing that the high side MOSFET or IGBT will be off during power-up.

**Receiver/Discriminator Circuit**
This circuit provides noise immunity by rejecting common-mode noise on the HSD inputs.

**Driver**
The CMOS driver circuit provides drive power to the gate of the MOSFET or IGBT. The driver consists of a CMOS buffer capable of driving external transistors at up to 20 V. The SOURCE pin is connected to the source of the external MOSFET or IGBT to establish a reference for the gate voltage.



7289229 0000646 018 PIN

## Pin Functional Description

**Pin 1, 2:**
No connection.

**Pin 3:**
Level shift input **HSD1** works in conjunction with HSD2 to provide interface from the low side control logic and to give noise immunity.

**Pin 4:**
Level shift input **HSD2** works in conjunction with HSD1 to provide interface from the low side control logic and to give noise immunity.

**Pin 5:**
**SOURCE** connection. Analog reference point for the circuit, normally connected to the source of the high side MOSFET or IGBT.

**Pin 6:**
**HS OUT** is the output of the MOSFET or IGBT driver for the high side.

**Pin 7:**
No connection.

**Pin 8:**
$V_{DDH}$ supplies power to the control logic and output driver.

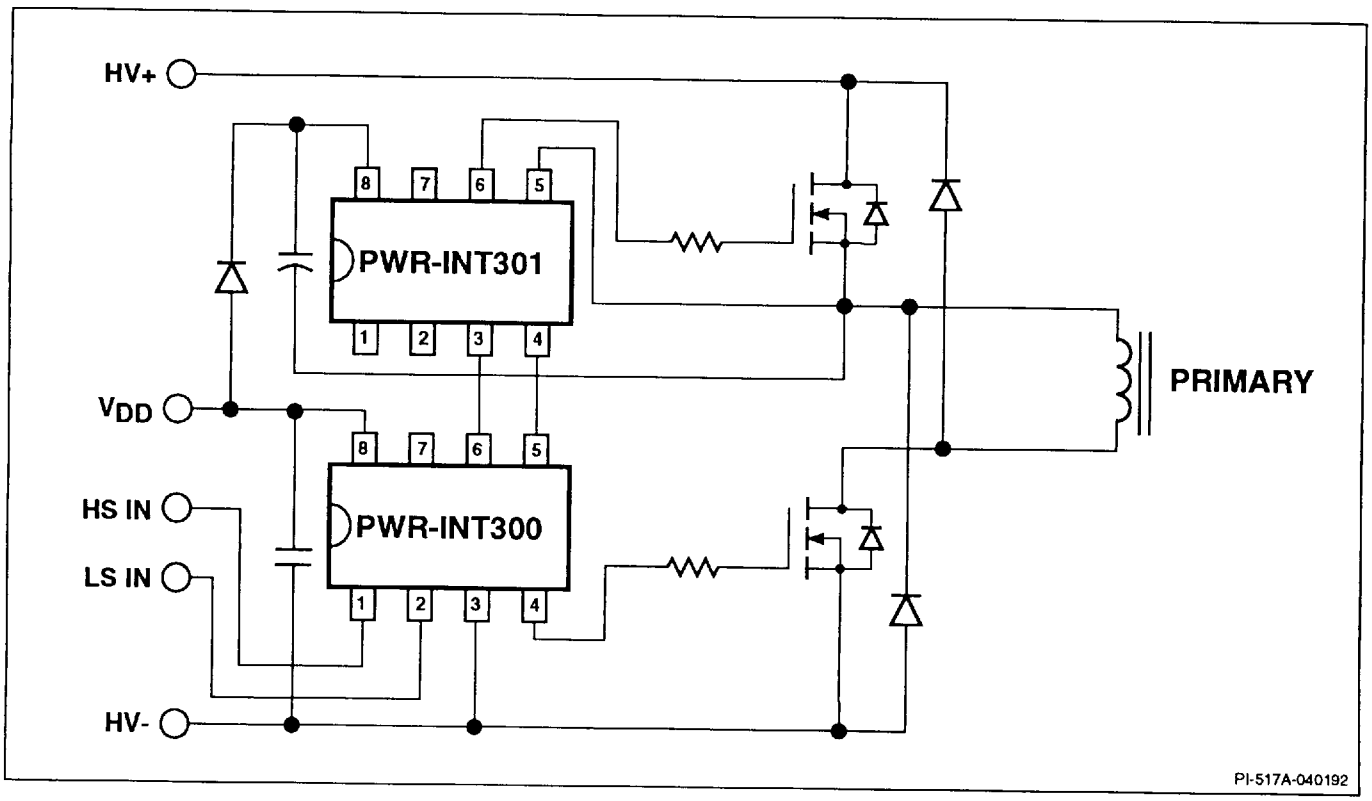



*Figure 4. The PWR-INT300 and PWR-INT301 Driving a Two Transistor Forward Converter.*

## ABSOLUTE MAXIMUM RATINGS[1]

| | |
|---|---|
| $V_{DD}$ Voltage | 22 V |
| Storage Temperature | -65 to 165°C |
| Ambient Temperature | -40 to 85°C |
| Junction Temperature | 150°C |
| Lead Temperature[2] | 260°C |
| Power Dissipation | 1.0 W |
| Thermal Impedance ($\theta_{JA}$) | 100°C/W |

1. Unless noted, all voltages referenced to COM, $T_A$ = 25°C
2. 1/16" from case for 5 seconds.



7289229 0000647 T54 PIN

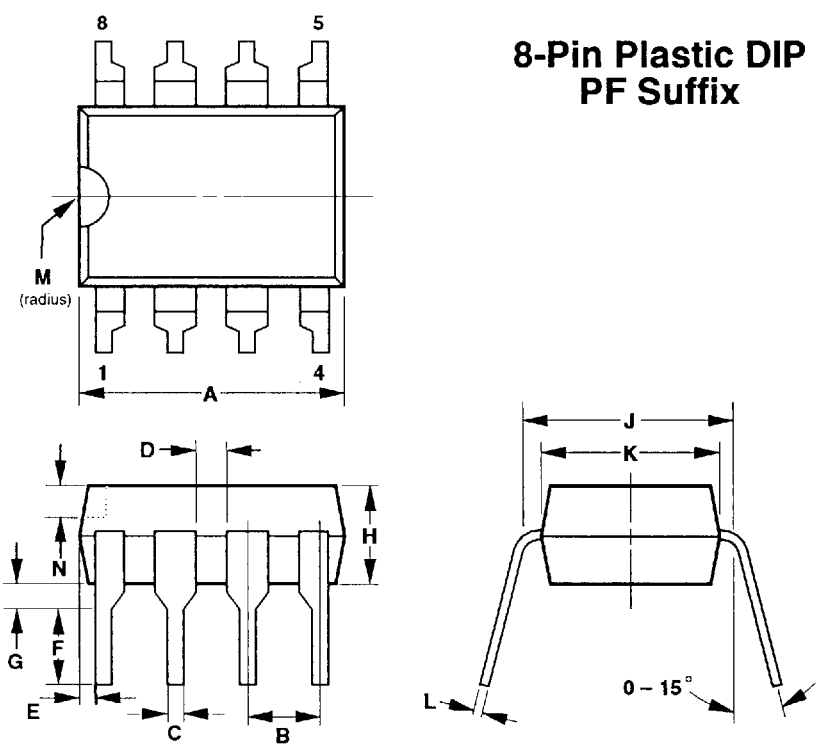
| Specification | Symbol | Test Conditions, Unless Otherwise Specified: $V_{DD}$ = 20 V, COM = 0V, $T_A$ = -40 to 85°C | Limits | | | Units |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| **HSD INPUTS** | | | | | | |
| Input Current Threshold | $I_{IN}$ | | | 2.5 | 5 | mA |
| **HS OUT** | | | | | | |
| Output Voltage, High | $V_{OH}$ | $I_o$= -65 mA | $V_{DD}$-1.0 | | | V |
| Output Voltage, Low | $V_{OL}$ | $I_o$= 130 mA | | | 1.0 | V |
| Output Short Circuit Current | $I_{OS}$ | $V_O$= 0 V | -0.5 | | | A |
| | | $V_O$= $V_{DD}$ | 1 | | | |
| Propagation Delay | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 1000 pF | | | 200 | ns |
| Rise Time | $t_r$ | $C_L$ = 1000 pF | | 50 | | ns |
| Fall Time | $t_f$ | $C_L$ = 1000 pF | | 25 | | ns |
| **SYSTEM RESPONSE** | | | | | | |
| Matching (Low On to High On) | $Mt_{P+}$ | High $t_{PLH}$ - Low $t_{PLH}$ | | | 50 | ns |
| Matching (Low Off to High Off) | $Mt_{P-}$ | High $t_{PHL}$ - Low $t_{PHL}$ | | | 50 | ns |
| **UNDERVOLTAGE LOCKOUT** | | | | | | |
| Undervoltage Threshold | $V_{UV}$ | | 8.5 | 9.25 | 10 | V |
| Undervoltage Hysterisis | $V_{UH}$ | | 0.75 | | 1.55 | V |



7289229 0000648 990 PIN

| Specification | Symbol | Test Conditions, Unless Otherwise Specified: $V_{DD}$ = 20 V, COM = 0V, $T_A$ = -40 to 85°C | Limits | | | Units |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| **SUPPLY** | | | | | | |
| Supply Current | $I_{DD}$ | | | 1.1 | 2.0 | mA |
| Supply Voltage | $V_{DD}$ | | 10 | | 20 | V |

| DIM | inches | mm |
|---|---|---|
| A | .395 MAX | 10.033 MAX |
| B | .090-.110 | 2.286-2.794 |
| C | .015-.021 | .381-.533 |
| D | .040 TYP | 1.016 TYP |
| E | .010-.040 | .254-1.016 |
| F | .125 MIN | 3.175 MIN |
| G | .020 MIN | .508 MIN |
| H | .125-.135 | 3.175-3.429 |
| J | .300-.320 | 7.620-8.128 |
| K | .245-.255 | 6.223-6.477 |
| L | .009-.015 | .229-.381 |
| M | .030-.110 | .762-2.794 |
| N | .020 TYP | .508 TYP |




## 8-Pin Plastic DIP
## PF Suffix

PO-001-071289



7289229 0000649 827 PIN