

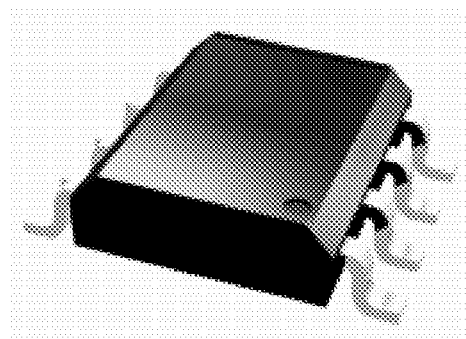
FEATURES

- High Linearity (IP3 55 dBm @ 1.9 GHz)
- High Isolation (30 dB @ 1.9 GHz)
- Low Insertion Loss (0.55 dB @ 1.9 GHz)
- Positive 3V to 5V Control Voltage
- Low DC Power Consumption

DESCRIPTION

The AWS5501 is a Single Pole Double Throw (SPDT) GaAs MMIC switch assembled in a SOIC-8 plastic package. The AWS5501 is designed for analog and digital applications that require low insertion loss and high linearity. State selection is achieved with positive voltage.

Typical Applications include: transmit/receive switch, diversity switching, and antenna selection.



S13
SOIC-8
8 Pin Plastic Package

ELECTRICAL SPECIFICATIONS AT 25 °C (0, +5V)

Parameter ¹	Frequency ²	Min	Typ	Max	Unit
Insertion Loss ³	DC - 1.0 GHz		0.45	0.55	dB
	1.0 - 2.0 GHz	-	0.6	0.75	
	2.0 - 3.0 GHz		0.9	1.2	
Isolation	DC - 1.0 GHz	20	23		dB
	1.0 - 1.8 GHz	22	25		
	1.8 - 2.1 GHz	27	31	-	
	2.1 - 3.0 GHz	10	12		
VSWR ⁴	DC - 1.0 GHz		1.2:1	1.3:1	-
	DC - 2.0 GHz	-	1.3:1	1.4:1	
	DC - 3.0 GHz		1.7:1	1.8:1	

OPERATING CHARACTERISTICS AT 25° C (0, +5V)

Parameter	Condition	Frequency	Min	Typ	Max	Unit
Switching Characteritics ⁵	Rise, Fall (10/90% or 90/10% RF)	-	-	60	-	ns
	On, Off (50% CTL to 90%/10% RF)			100		ns
	Video Feedthru			50		mV
Intermodulation Intercept Point (IP3)	For Two-tone Input Power +10 dBm	1.9 GHz	-	+55	-	dBm
Input Power for 1dB Compression	@ +3V	1.9 GHz	-	+28.5	-	dBm
	@ +5V	1.9 GHz		+35		
Control Voltage	V _{LOW} = 0 to 0.2 V @ 20 uA Max V _{HIGH} = +3 V @ 100 uA Max to +5 V @ 20 uA Max V _S = V _{HIGH} + 0.2V					

1. All measurements made in a 50 ohm system, unless otherwise specified.
2. DC = 300 kHz.
3. Insertion loss changes by 0.003 dB/°C.
4. Insertion loss state.
5. Video feedthru measured with 1 ns rise time pulse and 500 MHz bandwidth.

ABSOLUTE MAXIMUM RATINGS

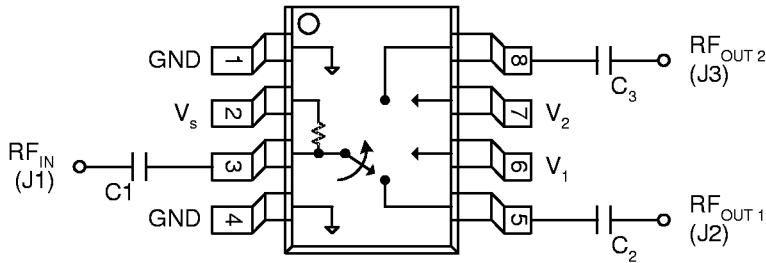
Characteristics	Value
RF Input Power	6W Max. > 900 MHz, 0/+5 Control
Supply Voltage	+8V
Control Voltage	-0.2V, +8V
Operating Temperature	-40° C to +85° C
Storage Temperature	-65° C to +150° C
Θ_{JC}	25° C/W

TRUTH TABLE

V_1	V_2	$J_1 - J_2$	$J_1 - J_3$
V_{High}	0	Isolation	Insertion Loss
0	V_{High}	Insertion Loss	Isolation

$V_{High} = +3 \text{ to } +5 \text{ V}$ ($V_S = V_{HIGH} \pm 0.2 \text{ V}$)

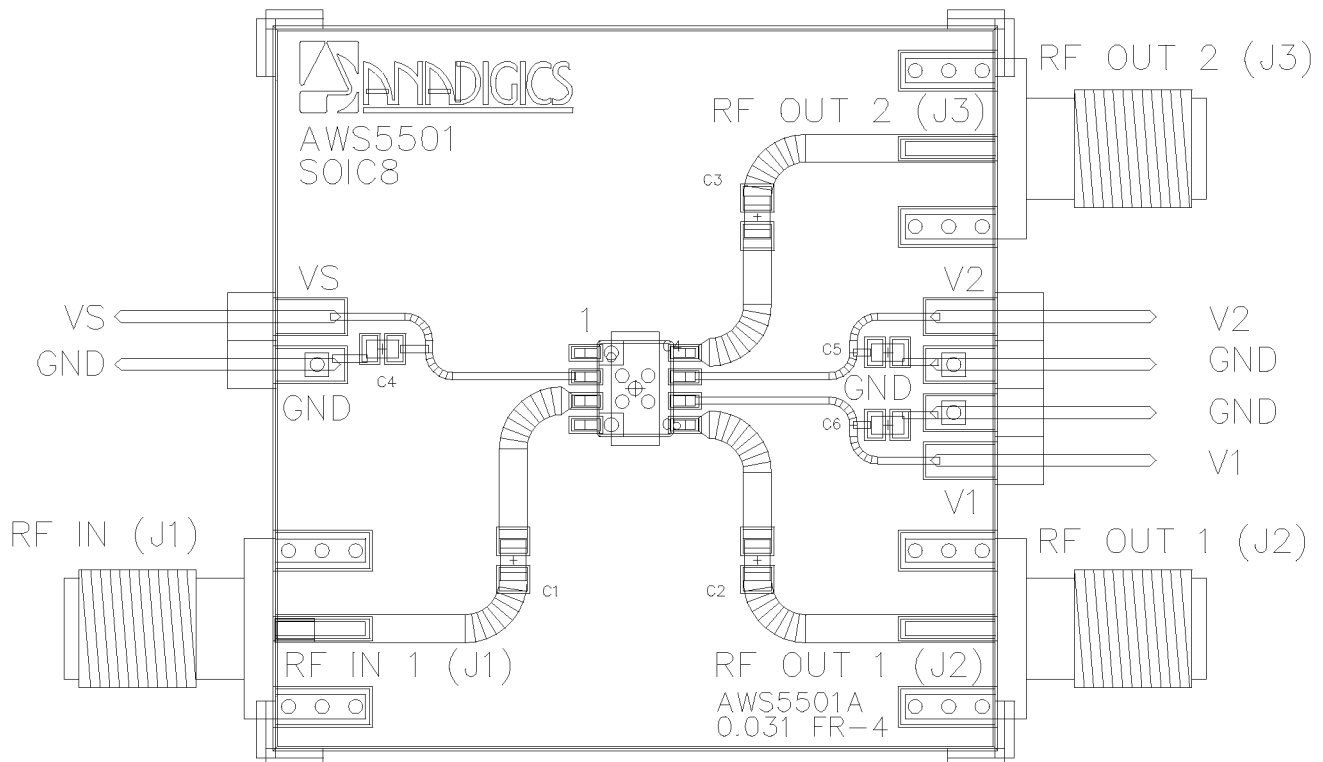
PIN OUT



DC block capacitors $C_{1,2,3}$ must be supplied externally.
 $C_{1,2,3} = 100 \text{ pF}$ for operation >500 MHz

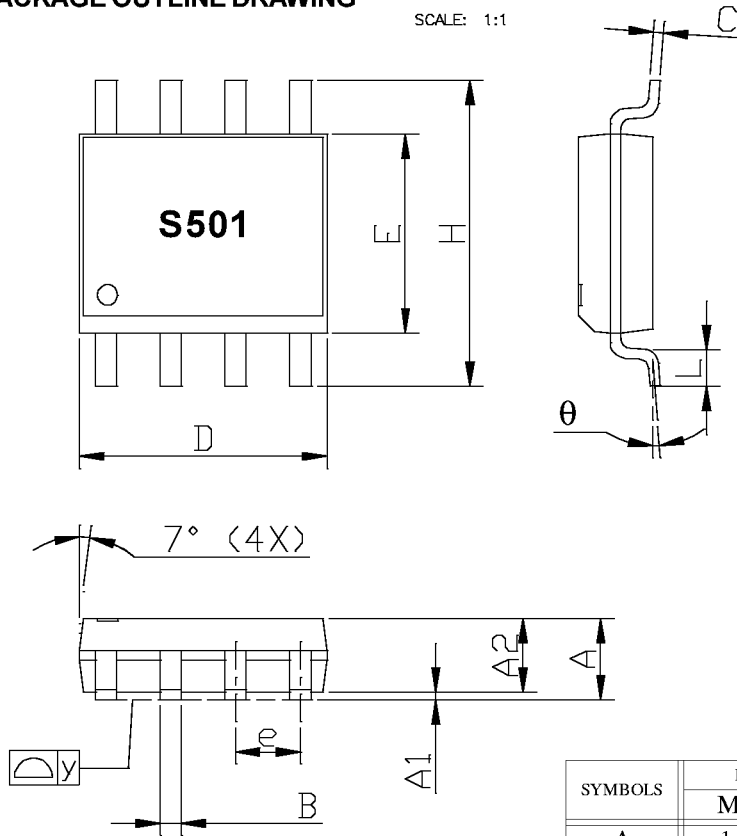
Pin	Function	Description
1	GND	Ground connection (keep as short as possible)
2	V_s	Bias voltage for positive control (3V to 5V)
3	RF_{IN} (J1)	RF common port
4	GND	Ground connection (keep as short as possible)
5	RF_{OUT} (J2)	RF port (can be used as an input or as an output)
6	V1	Control voltage (low 0V, High 3V to 5V)
7	V2	Control voltage (low 0V, High 3V to 5V)
8	RF_{OUT} (J3)	RF port (can be used as an input or as an output)

TEST CIRCUIT LAYOUT



PACKAGE OUTLINE DRAWING

SCALE: 1:1

**NOTES:**

1. Package body sizes exclude mold flash and gate burrs.
2. Dimension L is measured in gage plane.
3. Tolerance 0.10 mm unless otherwise specified.
4. Controlling dimension are metric. Converted inch dimensions are not necessarily exact.
5. Followed from JEDEC MS-012.

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	1.60	1.75	0.053	0.063	0.069
A1	0.10	—	0.25	0.004	—	0.010
A2	—	1.45	—	—	0.057	—
B	0.33	—	0.51	0.013	—	0.020
C	0.19	—	0.25	0.007	—	0.010
D	4.80	—	5.00	0.189	—	0.197
E	3.80	—	4.00	0.150	—	0.157
e	—	1.27	—	—	0.050	—
H	5.80	—	6.20	0.228	—	0.244
L	0.40	—	1.27	0.016	—	0.050
y	—	—	0.10	—	—	0.004
θ	0°	—	8°	0°	—	8°

ANADIGICS, Inc.

35 Technology Drive

Warren, New Jersey 07059

Tel: (908) 668-5000 / Fax: (908) 668-5132

Email: Mktg@anadigics.comwww.anadigics.com**IMPORTANT NOTICE**

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