PAGING DECODER IC(POCSAG)

The S-7037AF decoder IC is for use in the CCIR* Radio Paging Code Number 1 (POCSAG** code). It processes internally the POCSAG signals for the Tone-only pager. Furthermore, decoded data is transferred to an external microprocessor, so the S-7037AF can also be used for a Display pager. Five kinds of call-tone cadences generated for valid calls and messages received let user know which information is received. The S-7037A has a battery saving function that drives the signal receiving circuit intermittently.

* CCIR: International Radio Consultative Committee

** POCSAG: Post Office Code Standardization Advisory Group

■ Features

- Operating voltage : 1.7 to 5.5 V (3.0 V typ.)
- Current consumption : 110 μA max.
- Data rate : 1200 bps
- User address : 2
- Five cadences receivable:
  One for address 1, four for address 2
- External elements:
  Crystal oscillators (76 kHz), C_G, R_F
- Direct interface to IDROM (S-2100)
- CPU direct interface
  CPU controlling output pin

■ Functions

- Power-on clearing
- BCH correction up to 2 bits
- Battery saving
- Battery low alert
- Extension

■ Mask Options

Table 1

Item	Standard	Option
Corrected BCH errors	Random errors of up to 2 bits	Successive errors of up to 4 bits

Block Diagram

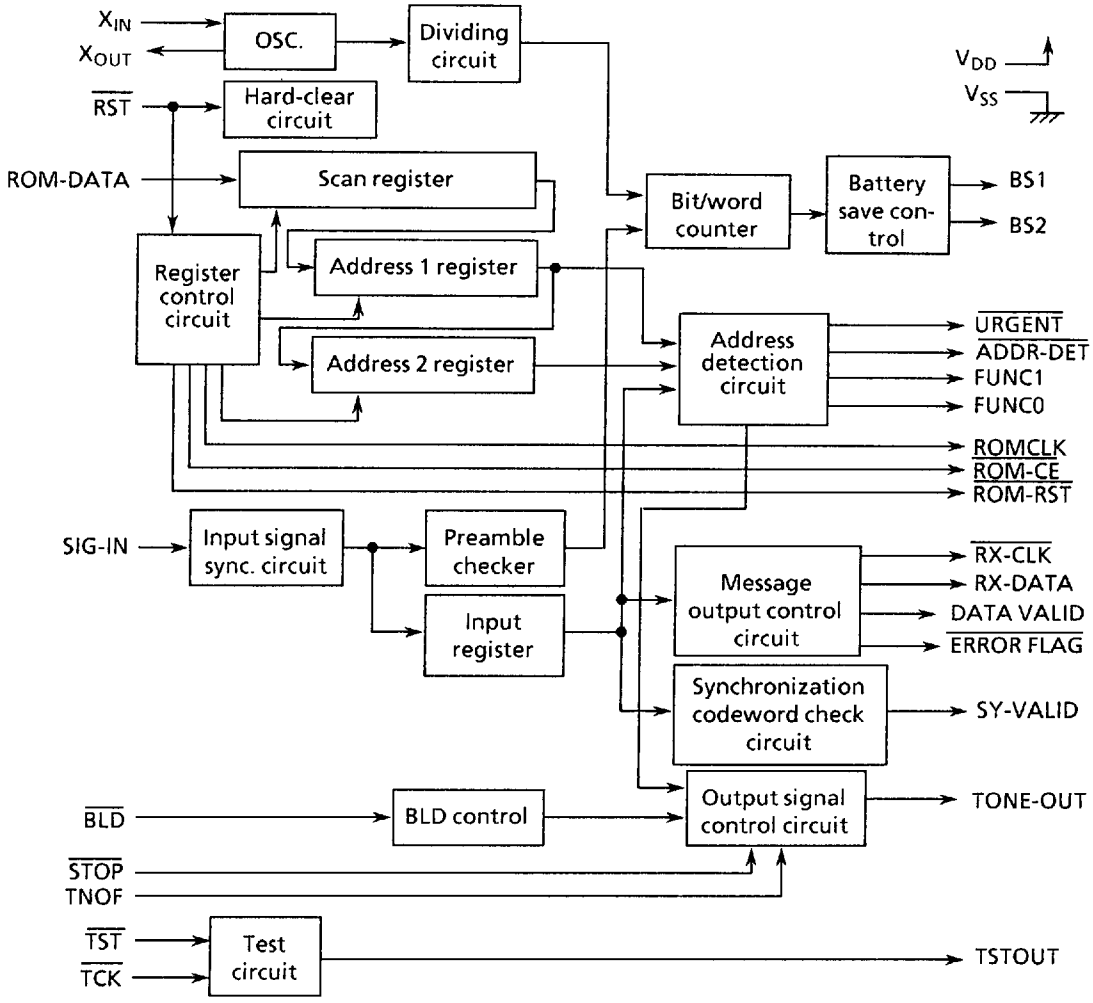


Figure 1

Pin Arrangement

TOP VIEW

28-pin SOP

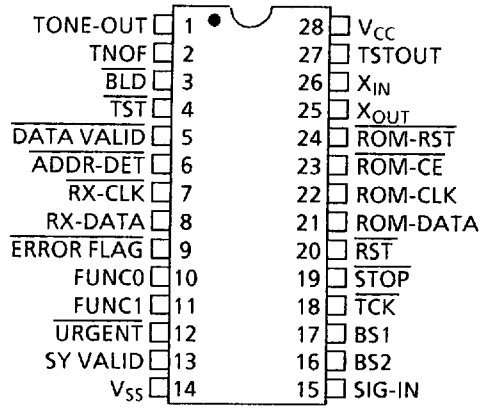


Figure 2

Table 2

Name	I/O	Functions
V_{SS}	—	Negative power supply terminal
V_{DD}	—	Positive power supply terminal
X_{IN}	Input	Crystal connection terminal
X_{OUT}	Output	Crystal connection terminal
BS1	Output	Battery save signal, indicates RF circuit power turns on
BS2	Output	Battery save signal, determines comparator reference voltage
$\overline{BLD}$	Input	Battery low detection signal input terminal: Samples the signals from a voltage detector, and battery is regarded as low when low is detected twice successively
$\overline{RST}$	Input	Hardware reset terminal
$\overline{TST}$	Input	Extension mode setting terminal
$\overline{TCK}$	Input	Extension clock
TSTOUT	Output	Extension mode output terminal
TNOF	Input	Tone frequency selection input terminal Open: 4800 Hz Low: 2400 Hz
$\overline{ADDR\text{-}DET}$	Output	Low continues until message output is completed when input signal address matches with that of ID-ROM
$\overline{RX\text{-}CLK}$	Output	RX-DATA (reception message) sample timing clock
RX-DATA	Output	Reception message (sequential output)
TONE-OUT	Output	Tone output signal
$\overline{STOP}$	Input	Turns off tone when $\overline{STOP}$ is low
SIG-IN	Input	Inputs serial data reception signal from RF circuit
$\overline{ROM\text{-}CE}$	Output	Enables ID-ROM chip
ROMCLK	Output	ID-ROM synchronous clock
ROM-DATA	Input	ID-ROM data
$\overline{ROM\text{-}RST}$	Output	ID-ROM reset
FUNC1	Output	Selected tone (F1) output terminal for received call
FUNC0	Output	Selected tone (F0) output terminal for received call
$\overline{URGENT}$	Output	Outputs low when a call is received to address 1
DATA VALID	Output	Outputs high when a received message is valid
$\overline{ERROR\ FLAG}$	Output	Outputs low when a received message has an error

■ Dimensions

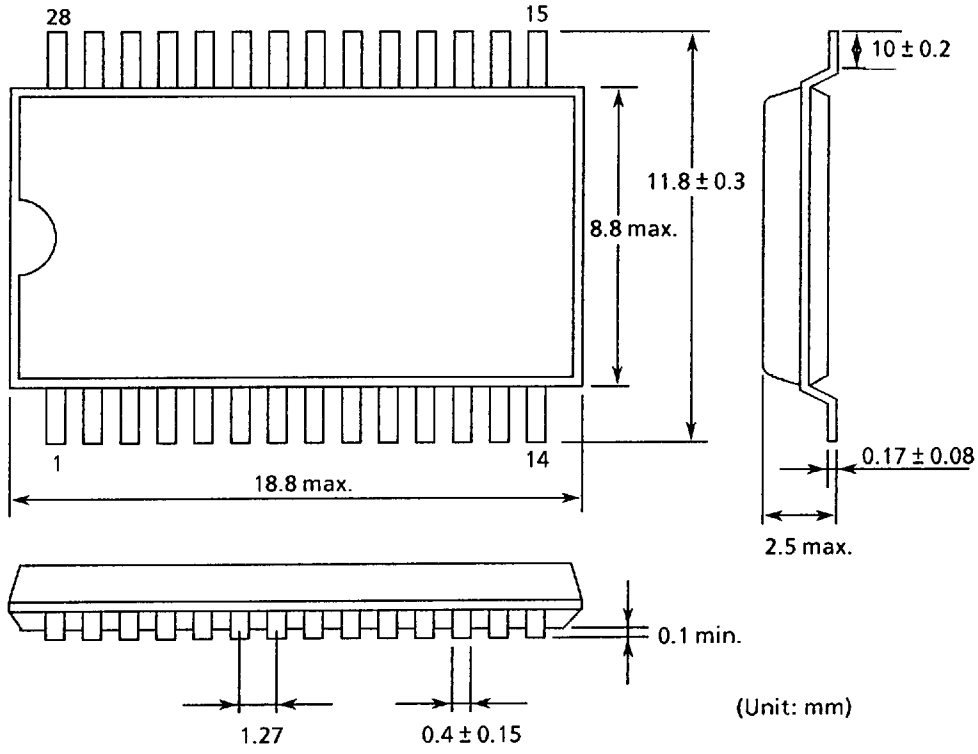


Figure 3

■ Absolute Maximum Ratings

Table 3

Item	Symbol	Ratings	Unit
Power supply voltage	V_{DD}	-0.3 to 7.0	V
Input voltage	V_{IN}	V_{SS}-0.3 to V_{DD} + 0.3	V
Output voltage	V_{OUT}	V_{SS} to V_{DD}	V
Storage temperature	T_{stg}	-40 to + 125	°C
Operating temperature	T_{opr}	-10 to + 70	°C

■ Electrical Characteristics

Table 4

(Unless otherwise specified: V_{DD} = 3.0 V, V_{SS} = 0 V, Ta = 25°C)

Item	Symbol	Conditions (applicable terminals)		Min.	Typ.	Max.	Unit	Test cir	Note
Operating power supply voltage	V_{DD}	Ta = -10°C to + 70°C		1.7	3 0	5 0	V	①	1
		Ta = + 10°C to + 70°C		1.7	3.0	5.5	V		
Oscillating start voltage	V_{DOB}	Ta = -10°C to + 70°C		2.0	—	5.0	V	①	2
		Ta = + 10°C to + 70°C		2 0	—	5.5	V		
Total average standby current consumption	I_N	f_0 = 76800 Hz	V_{DD} = 1.7 V	—	15	30	µA	①	3
			V_{DD} = 3.0 V	—	35	50	µA		
TONE-OUT output current	I_{BOH}	V_{DD} = 1 9 V, V_{OH} = 1 6 V		—	—	-500	µA	②	4
	I_{BOL}	V_{DD} = 1.9 V, V_{OL} = 0 3 V		500	—	—	µA		
Output voltage	V_{OH}	I_{OH} = -50 µA (*)		2 90	—	—	V	③	—
	V_{OL}	I_{OL} = 50 µA (*)		—	—	0.10	V		
Input voltage	V_{IH}	V_{DD} = 1.7 V to 5.5 V		0 8 × V_{DD}	—	—	V	④	—
	V_{IL}	V_{DD} = 1.7 V to 5 5 V		—	—	0.2 × V_{DD}	V		
Input current	I_{IN}	V_{IN} = V_{DD} or V_{SS}		—	—	± 0.1	µA	⑤	4
Pull-up current	I_{R1}	V_{IL} = 0 V (**)		-20	-10	-5	µA	⑥	—
	I_{R2}	V_{IH} = 2 8 V ($\overline{STOP}$)		-120	-60	-30	µA		
	I_{R3}	V_{IL} = 0 V ($\overline{STOP}$)		-20	-10	-5	µA		
	I_{R4}	V_{IH} = 2 8 V ($\overline{RST}$)		-120	-60	-30	µA		
	I_{R5}	V_{IL} = 0 V ($\overline{RST}$)		-3.75	-2	-1	µA		
	I_{R6}	V_{IL} = 0 V ($\overline{TST}$, $\overline{TCK}$)		-200	-100	-50	µA		
$\overline{RST}$ pulse width	t_{RST1}	Ex capacitor = 20 pF	At power on	10	—	—	µs	—	—
	t_{RST2}		At forcible input	1	—	—	ms		
$\overline{STOP}$ pulse width	t_{STOP}			10	—	—	ms	—	—
Frequency IC deviation	△f/△IC			—	—	± 50	ppm	—	5
Frequency voltage deviation	△f/△V			—	—	± 8	ppm	—	6
Recommended equivalent resistance	CI			—	—	45	kΩ	—	—

* $\overline{ADDR\text{-}DET}$, $\overline{RX\text{-}CLK}$, RX-DATA, SY-VALID, BS1, BS2, ROMCLK, $\overline{ROM\text{-}CE}$, TSTOUT, $\overline{URGENT}$, FUNC1, FUNC0, $\overline{ERROR\ FLAG}$

** $\overline{BLD}$, $\overline{TST}$, $\overline{TCK}$, SIG-IN, TNOF

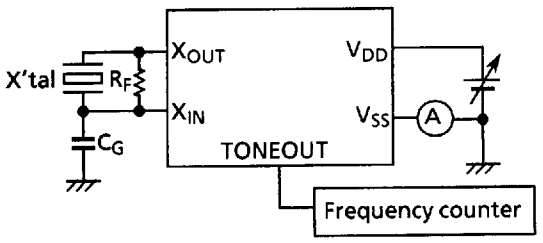
\# For only $\overline{RST}$ pin, latch-up strength is -90mA.

Notes:

1. Power supply voltage while frequency output from TONE-OUT is stable at $\overline{TCK}$ = low. It is recommended that 0 2 µF or more of capacitor is inserted between V_{SS} and V_{DD}.
2. Voltage value where 2.7 kHz is output from TONE-OUT pin within 10 s after oscillation starts
3. Excluding a current flowing into the pull-up resistors Measured under the condition that SIG-IN and ROM-DATA are connected to V_{SS}, other pins are open and the oscillation circuit operates.
4. Suppose that a current flowing into the IC is positive.
5. $$\triangle f/\triangle IC = \frac{f(V_{DD} = 3\ 0\ V) - f_0}{f_0} \times 10^6 \text{ (ppm)}$$ f_0: Average frequency when V_{DD} is 3.0 V
6. $$\triangle f/\triangle V = \frac{f_1(V_{DD} = 3\ 0\ V) - f_2(V_{DD} = 2\ 9\ V)}{f_1(V_{DD} = 3.0\ V)} \times 10^6 \text{ (ppm)}$$

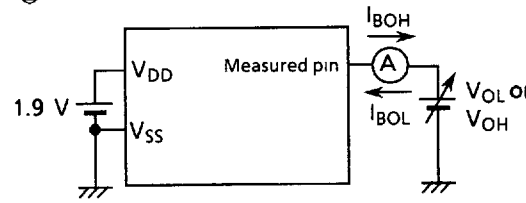
■ Test Circuits

①



R_F = 20 MΩ, C_G = 10 pF
X'tal = 76800 Hz
An ammeter is connected only when a current consumption is measured.

②



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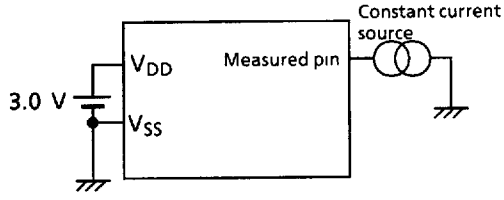

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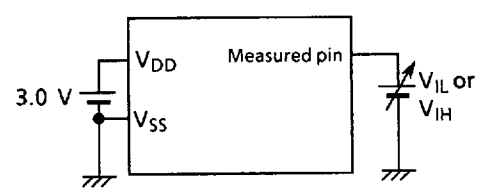

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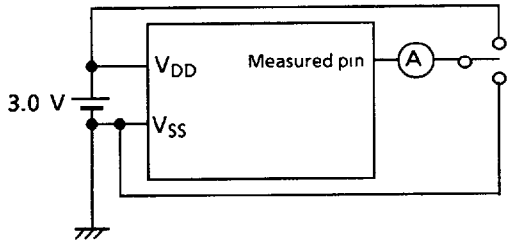

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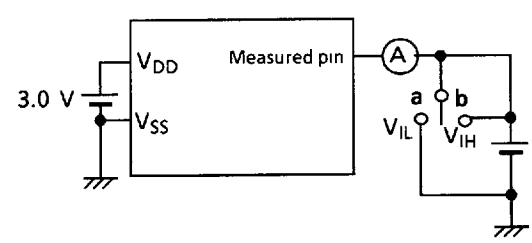


When I_{R1}, I_{R3}, I_{R5} or I_{R6} is measured: switch a
When I_{R2} or I_{R4} is measured: switch b

Figure 4

■ POCSAG Signal Code Format

The POCSAG signal code format of the S-7037AF conforms with CCIR recommendation 584 (see Figure 5).
The transmission unit of a POCSAG signal is called a *block*. This block comprises a preamble and one or more batches following the preamble.

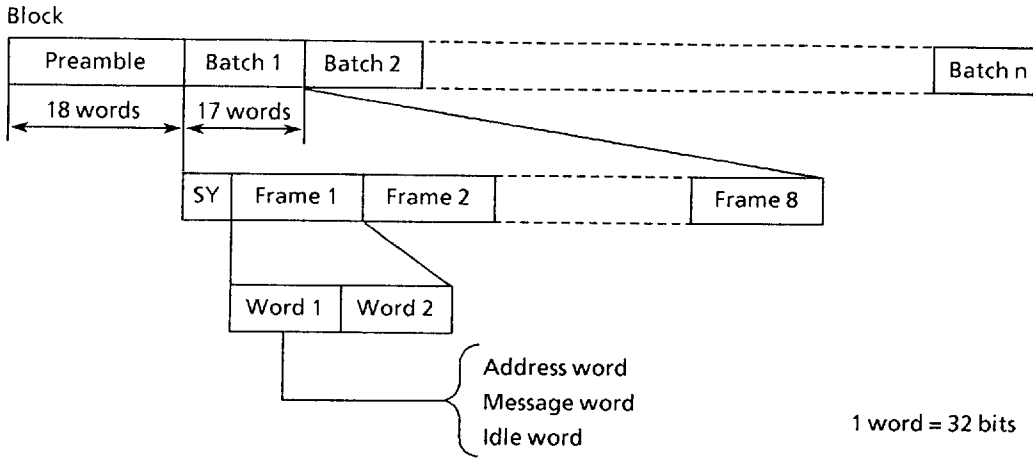
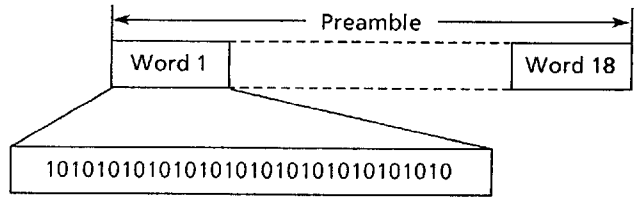


Figure 5 POCSAG code format

1. Preamble
   The preamble at the beginning of a block gives notice of a POCSAG signal sent to the S-7037AF. A preamble consists of at least 576 bits (18 words) alternate signals of 1 and 0. The S-7037AF starts to get the internal circuit and the POCSAG signal synchronized once it receives a preamble.



1/0 alternate pattern signal of 32 bits

32 bits x 18 words = 576 bits

Figure 6 Preamble configuration

2. Batch
The batch contains information on the POCSAG signal, sent following a preamble. Each batch carries a synchronization codeword (SY) and eight frames.
When the S-7037AF recognizes preamble and SY as being those of POCSAG signal, it considers the following signal as a POCSAG frame data and receives it. The S-7037AF identifies the receiving frame set by ID-ROM and receives only the selected frame of one batch and BS1 pin turns high (on) only with a selected frame.

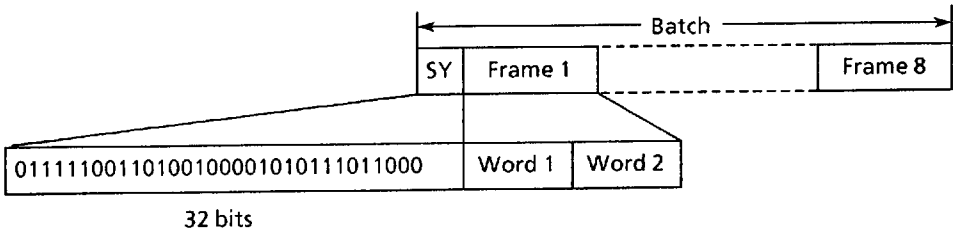


Figure 7 Batch configuration

Synchronization codeword (SY): 32-bit signal shown in Figure 7. When the SY is received after a preamble, it is considered a POCSAG code.

Frame: One frame consists of two words, each of which is 32 bits. There are three types of words: address word, message word and idle word.

3. Kinds of word
There are three types of word information, as shown in Figure 8.

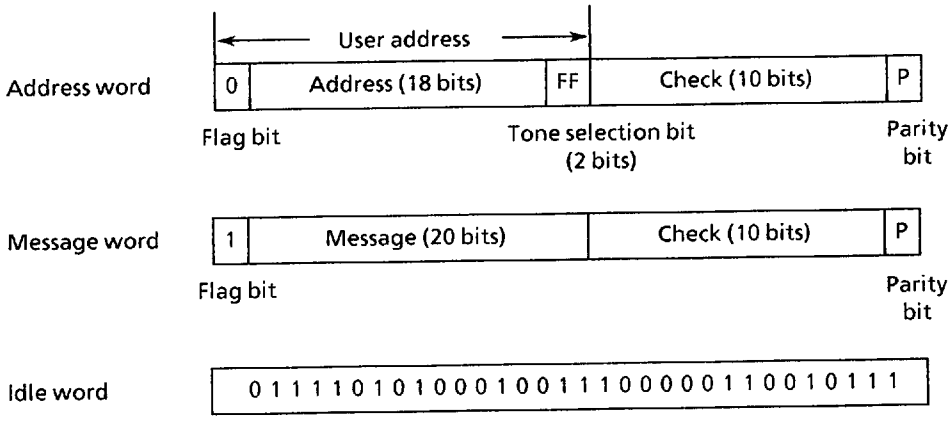


Figure 8 Kinds of words

The address word is sent first, followed by sending the message word to the address (for display pager only). Two or more message words are sent continuously. (Tone-only pagers need no messages; idle words can be used instead.) A flag bit determines whether the word is an address word or a message word. 0 means an address word, and 1 means a message word. The actual information is the address and tone selection bits (FF) in an address word, and the message in a message word.

Address word: This data indicates that the pager is called. An address is always sent with any information. Of the 21 bits in a user address, only 18 bits are used for the actual address. Two tone selection bits select the calling tone (see p5-161 "Tone"). Check bits perform BCH checks (see p5-165 "BCH decode function").

Message word: Of the 32 bits in a message word, only 20 bits are used for the actual message. If a message exceeds 16 words, subsequent message words are received in the next frame until an address word is detected (a flag bit becomes 0). Multiple message words can be continuously sent. A synchronization codeword (SY) must be inserted to continue message from frame 8 (last frame of a batch) to the next batch. The S-7037AF outputs these message words to the CPU.

Idle word: If a batch does not have any information to send, idle words fill the blank portion of the batch. Idle word cannot be assigned as ID codes.

■ Flow Charts

Figures 9 and 10 show flow charts of POCSAG signal reception. These flow charts indicate the operations from turning on the power to sending output signals, for tone-only pager and for display pager.

1. Tone-only pager

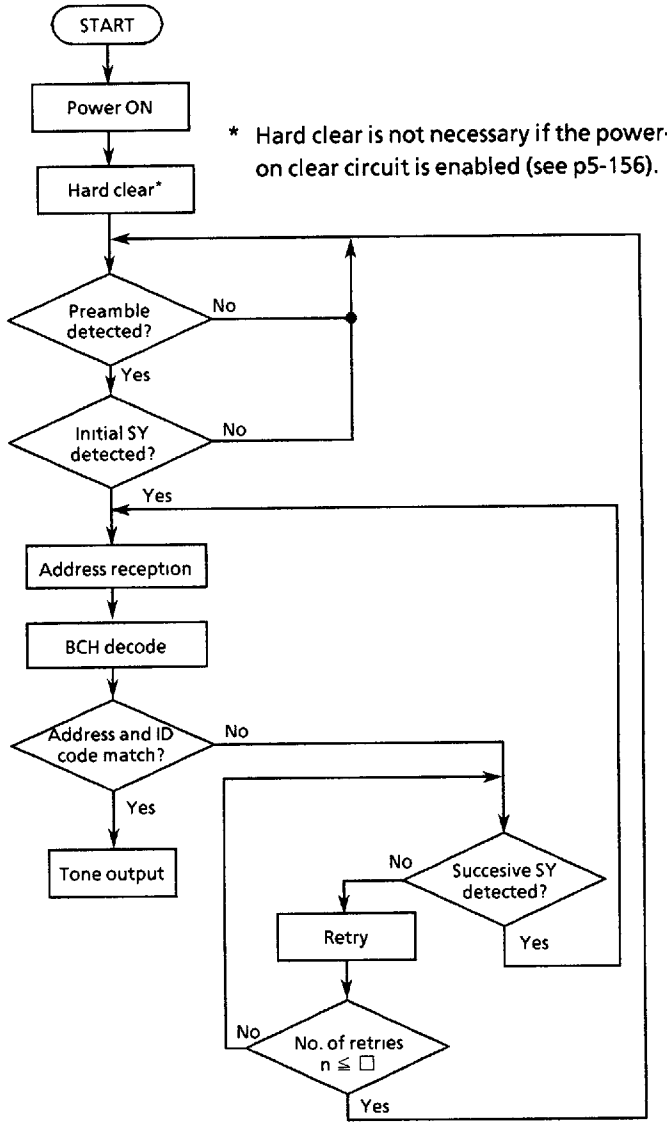
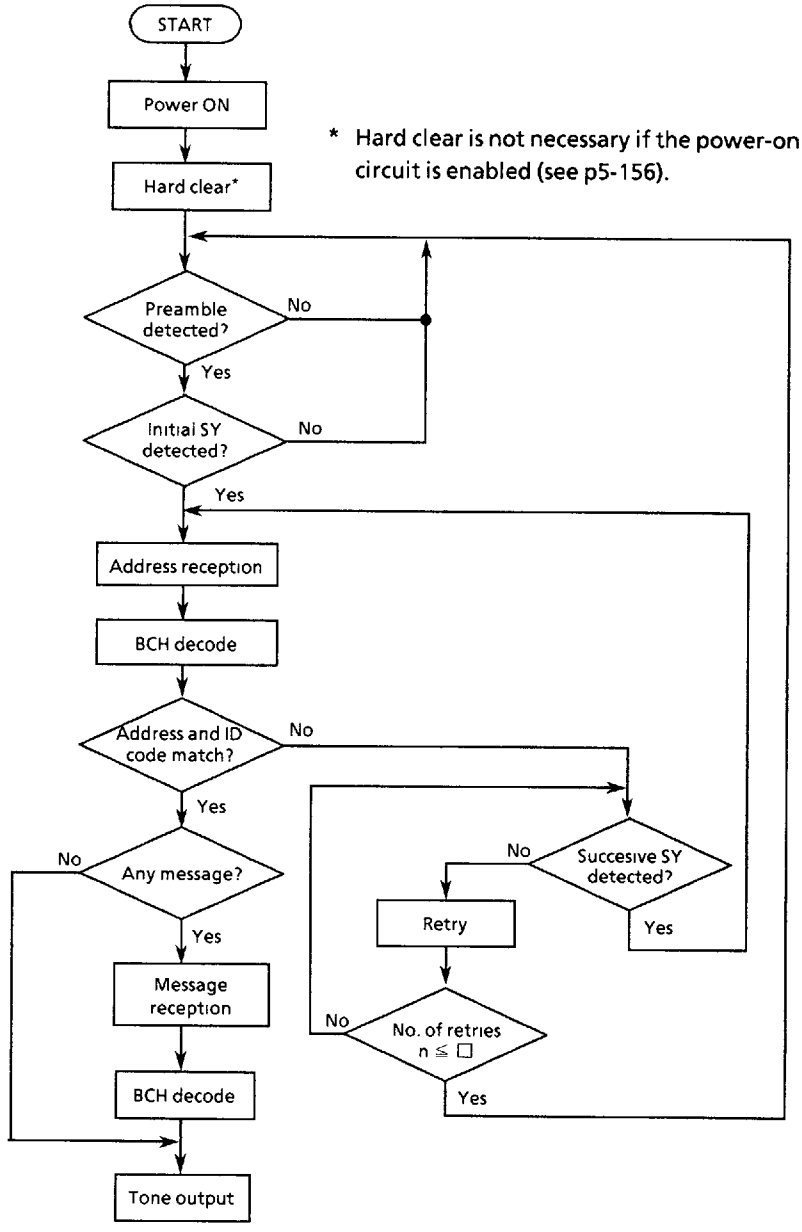


Figure 9

2. Display pager



* Hard clear is not necessary if the power-on clear circuit is enabled (see p5-156).

Figure 10

■ Basic Operation

1. Hard clear
   The internal circuit is initialized by setting the $\overline{RST}$ pin to low. The initial tone is output immediately after hard clear (see p5-161 for waveform). POCSAG signal cannot be received during this time. The initial tone automatically stops when the $\overline{STOP}$ pin is set to low or two minutes have passed. After the completion of initial tone, ID-ROM data is fetched in the S-7037AF.
   The internal circuit will function as a power-on clear circuit by connecting 20 pF capacitor between $\overline{RST}$ and V_{SS} pins. That is, the internal circuit is automatically initialized at power on.

2. Detecting preamble
   Preamble detection mode starts when hard clear is completed or when synchronization codeword is not detected even if detection is repeated over number of retries. During this mode, an alternate pattern of 1, 0, 1, 0 of 12 consecutive bits is regarded as a preamble.
   The S-7037AF drives the reception frequency (RF) circuit intermittently to save power consumption. When BS1 pin is high, the radio part is turned on to detect preambles. When the BS1 pin is low, preamble signals are not detected. Once a preamble is detected, the BS1 pin is set to high until a SY is detected. Figure 11 shows the timing of BS1 pin and preambles.

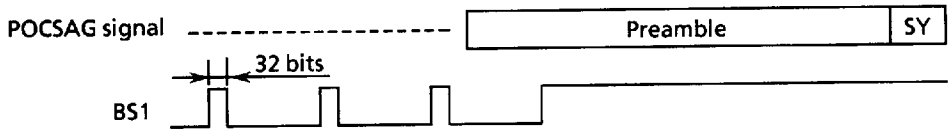


Figure 11 Timing of BS1 pin and preambles

Simultaneous detection mode of preamble and SY
In this mode, either a preamble or a synchronization codeword (SY) is detected simultaneously to receive POCSAG signals. This mode becomes valid when the PR bit of the ID-ROM is set to high. SY can be detected, even if no preamble is detected.

3. Detecting synchronization codeword (SY)
After detecting a preamble, the S-7037AF enters SY detection mode. The SY, first after preamble detection, is the initial SY. New SYs, sent after a batch is received, are called succesive SY.

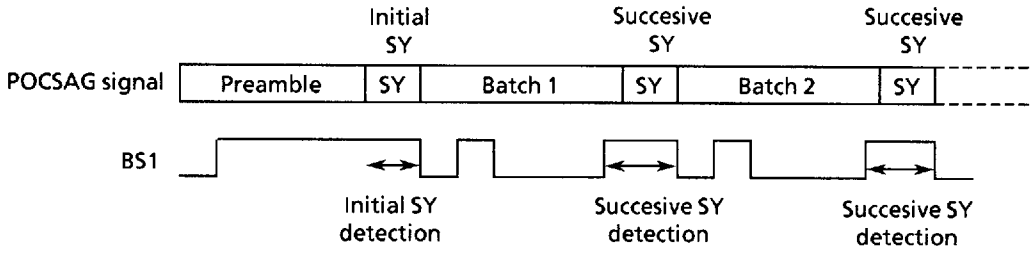


Figure 12 Initial SY and succesive SY

3.1 Initial SY detection mode
The operation which detects the initial SY following a preamble is called the initial SY detection mode. The S-7037AF compares the sent data with the SY data set in the S-7037AF (see Figure 7). After receiving one bit of data, the S-7037AF compares the 32-bit data, including that bit and those before it, with the SY. If 30 or more bits match, the SY is considered to be detected. Even if radio wave are affected by noise, SY is detected as long as there are no more than two faulty bits.

If SY is not detected after comparing 32 words (about 1K bits) in initial SY detection mode, the S-7037AF returns to preamble detection mode.

3.2 Succesive SY detection mode
After initial SY is detected, SY is sent for each batch. After receiving 8-frame (16-word) data, the S-7037AF enters automatically succesive SY detection mode. Since the signal is already synchronized, BS1 goes high and the S-7037AF compares SY, synchronized with the timing when 32 bits of succesive SYs are output. In the same way as in initial SY detection mode, SY is detected even when there are up to two bits of unmatching data. If SY is detected, the bit/word counter is reset, followed by proccesing a batch of data.

If SY is not detected, the S-7037AF retries SY detection for the number of times specified in ID-ROM plus two. If the S-7037AF fails to detect SY during these retires, it returns to preamble detection mode.

Example of setting number of retries

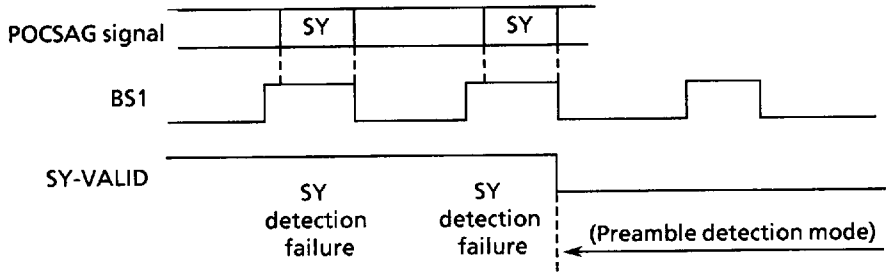
Specifies with bits R3 to R0 of the S-2100 ID-ROM (see p5-168 "Interface to ID-ROM" for the bit configuration).

Table 5 Setup of number of retries

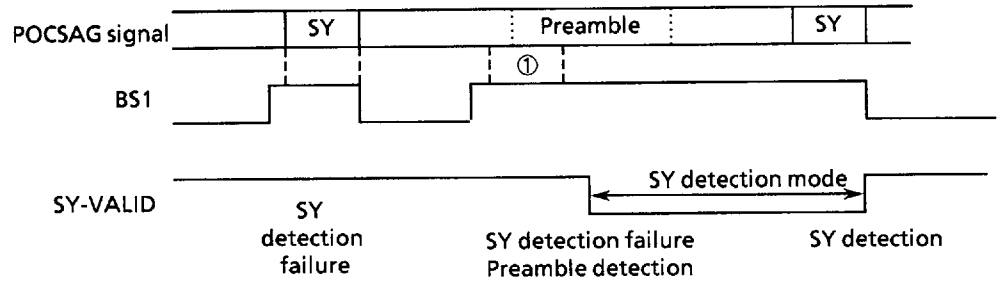
R3	R2	R1	R0	Number of retries
0	0	0	0	2
1	0	0	0	10
1	1	1	1	17

If 12 bits consecutive alternate data such as 1, 0, 1, 0 is detected during the final retry, the S-7037AF regards it as a preamble and enters the initial SY detection mode (see Figure 13).

(1) When the S-7037AF detects no SY and returns to the preamble detection mode



(2) When the S-7037AF detects a preamble in the final retry



① : Period of final retry

Figure 13 Failure to detect succesive SY

4. Detecting address
After detecting SY, the S-7037AF receives eight frames. An address word is placed at the top of a frame. As shown in Figure 14, the last 11 bits of the address word are check bits, and are used for error detection with BCH decode (see p5-165 "BCH decode function"). The S-7037AF compares the non-erroneous address words with the two addresses written in ID-ROM, and receives a message word if they match. Erroneous address words are ignored. If addresses 1 and 2 are received at the same time, address 1 is given priority. Address 2 is regarded as not being received.

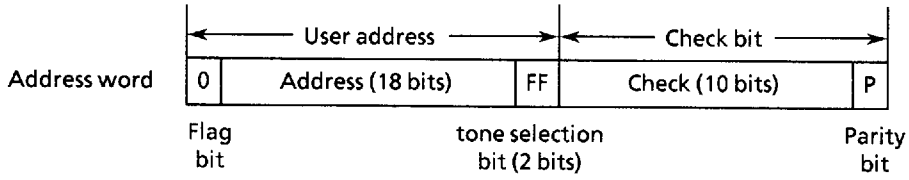


Figure 14 Address word configuration

5. Detecting message (for display pager only)

When an address word is detected, a message word is subsequently received. The S-7037AF sends the message word to CPU, and the message is then sent to the pager display. Message words are continued to detect until an address or idle word is detected.

As shown in Figure 14, the last 11 bits of the message word are also check bits, and are used for error detection with BCH decode (see p5-165 "BCH decode function"). If an error is found, the message word is sent to CPU with $\overline{\text{ERROR FLAG}}$ made low.

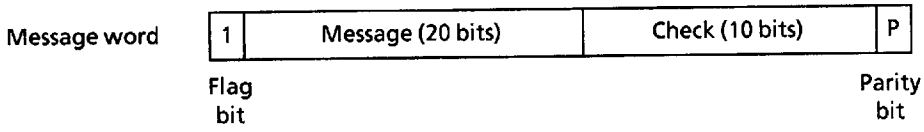


Figure 15 Message word configuration

When the S-7037AF detects SY between message words, the following message is sent to the CPU again after SY is detected. If synchronization is out of step at SY detection, message detection is terminated.

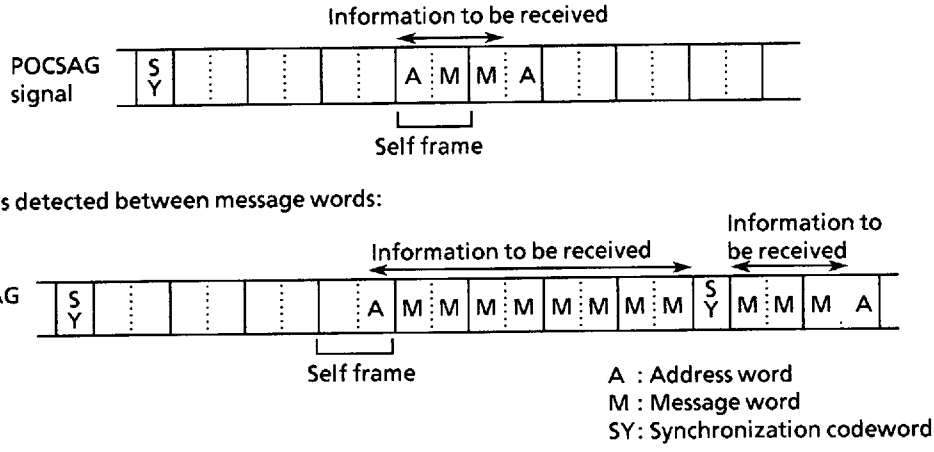


Figure 16 Information to be received

6. Tone

When detecting an address (receiving a call), the S-7037AF sends a message and notifies the operator of the reception by means of tones. Tone is output from TONE OUT pin, upon completion of pager initialization, address reception and power supply voltage drop (see p5-164 "Battery low alert function"). Tone frequency at TNOF open is 4.8 kHz, and can be changed into 2.4 kHz by setting TNOF pin to low.

Upon completion of initialization: A 4.8-kHz single-tone signal is output for two seconds just after hard clear. This is called the initial tone. Setting the $\overline{\text{STOP}}$ pin to low for 2.3 s prevent the initial tone sounding.

Upon address reception: When address reception is completed, a tone is output for 20 seconds. The waveform varies with the contents of the tone selection bits. The tone stops by setting $\overline{\text{STOP}}$ pin to low for 2.3 s. Five types of tones are specified: one for address 1 and four for address 2.
Upon address reception, a quiet sound is emitted for the first two seconds, it then increases in volume.

Upon power supply voltage drop: If $\overline{\text{BLD}}$ pin goes low, due to a power supply voltage drop, two 4.8-kHz single-tones are output every 32 seconds. This is called "BLD tone". This continues until $\overline{\text{STOP}}$ pin is set to low for 2.3 s.

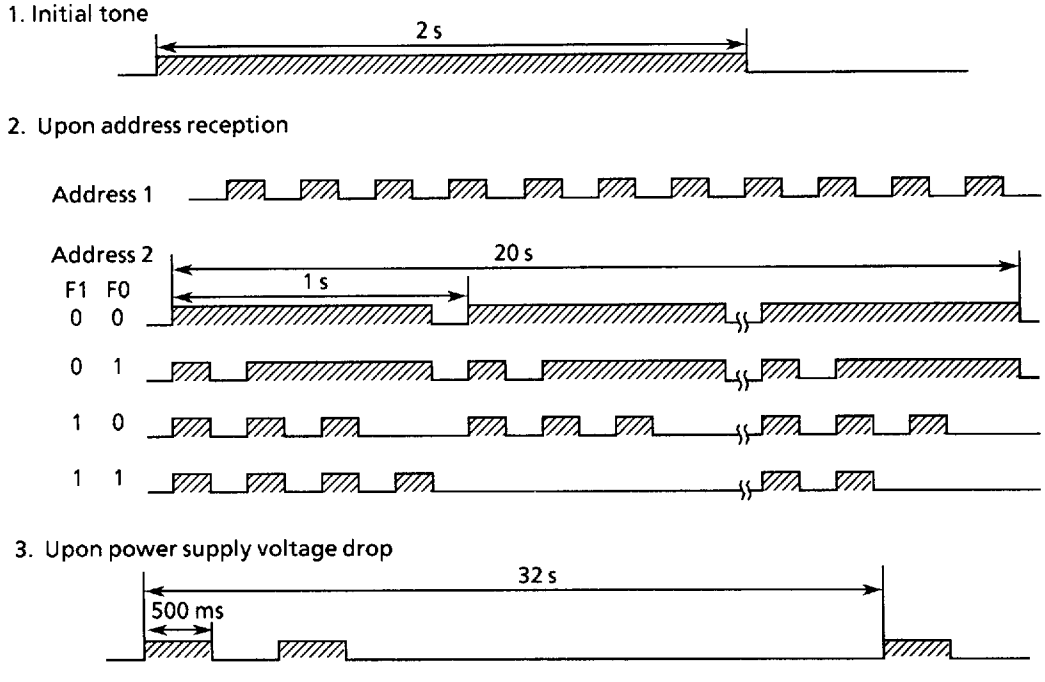


Figure 17 Output waveform of TONE-OUT

■ Internal Functions

The S-7037AF has the following functions to support its basic operations:

- Battery save function to reduce power consumption
- Battery low alert function to notify power supply voltage drop
- BCH decode function to automatically correct address and message errors
- Extension function to enable forcible output of tone

These functions are explained below:

1. Battery save function
   The battery save function turns the RF circuit on and off intermittently to reduce the power consumption of the pager. Two signals are used: BS1 and BS2. BS1 enables the RF circuit. When the BS1 signal is set to high, the RF circuit is turned on. BS2 is the timing pulse to detect preambles and synchronization codes. If BS2 is set to low, SIG-IN does not receive data and does not compensate synchronization.

1.1 BS1

Upon preamble detection: High and low are repeated for each word (32 bits). When BS1 is high, the RF circuit is turned on and preamble detection is enabled.

Upon SY detection: BS1 is set to high to receive POCSAG codes until the initial SY is detected up to 32 words, after preamble signal is detected. If no SY is detected after a period of 64 words, the S-7037AF returns to preamble detection mode. BS1 is also set to high when a consecutive SY is detected. If the S-7037AF fails to detect a consecutive SY more than a number of retries, it returns to preamble detection mode.

After SY detection: The BS1 signal is controlled by the value of the bit/word counter.
BS1 is set to high synchronized with the timing of the frame specified in ID-ROM, and is kept as high until all messages (address only for tone-only pagers) are received. BS1 is set to high 16.5 bits earlier than the specified frame. This supplied power to the RF circuit early enough to allow the RF circuit to be activated (offset time).

For the simultaneous detection mode of preambles and SYs, set the PR bit of ID-ROM to high.

1.2 BS2

Upon preamble detection: BS2 is set to high by eight bits, synchronized with BS1 being set to high.

Upon SY detection: BS2 is set to high by eight or 16 bits (selected by the OF bit of ID-ROM), synchronized with BS1 being set to high.

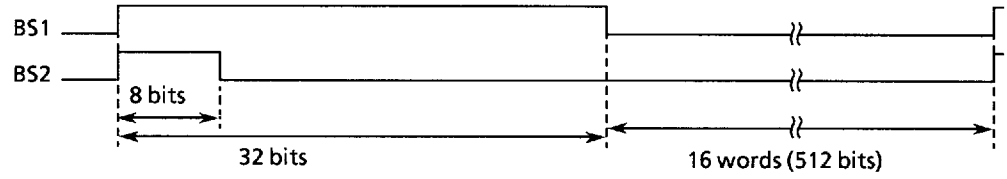
For the simultaneous detection mode of preambles and SYs, set the PR bit of ID-ROM to high.

1.3 Switching the offset time

BS1 and BS2 are set to high when the frame specified in ID-ROM and a consecutive SY arrive. They are set to high 16.5 bits earlier than the frame specified as the offset time.

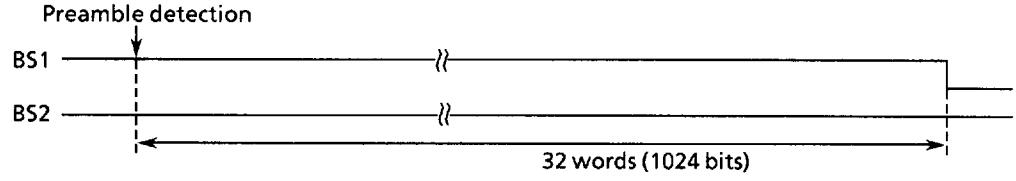
Figure 18 shows the timing of battery save operation.

(A) Preamble detection mode



If a preamble is detected, the mode is terminated and (B) starts.
If no preamble is detected, the operation is repeated until detection.

(B) SY detection following preamble detection



If SY is detected, the mode is terminated and (C) starts.
If no SY is detected, the operation is repeated until detection.

(C) After SY detection

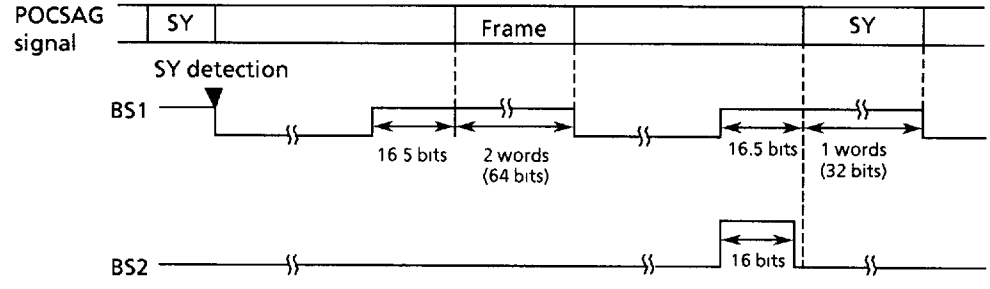


Figure 18 Battery saving

2. Battery low alert

Detection signals of an external voltage detector are input from $\overline{BLD}$ pin, and these levels are sampled. If $\overline{BLD}$ pin is set to low twice consecutively, the tone signal is output. This tone continues until $\overline{STOP}$ pin is set to high for more than 2.3 s.
If the sampling overlaps the tone output, it is not detected at that point but at the next sampling point.

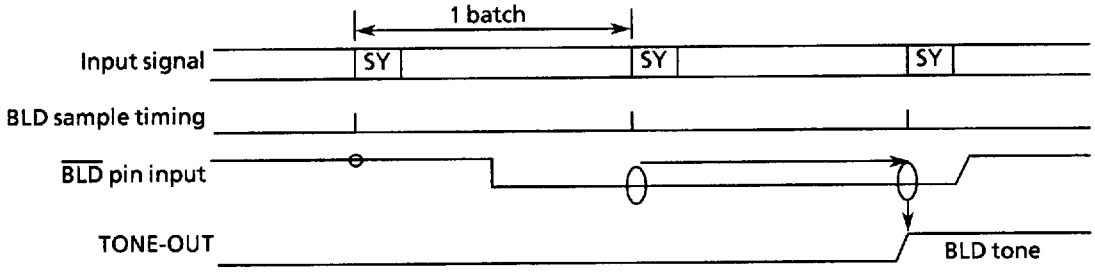


Figure 19 Sampling and detection of power supply voltage

3. BCH decode function
An address or message word consists of 21 valid data bits and 11 check bits. Valid data information is extracted and checked with the check bits. If an error is found, corrections are made according to the number of erroneous bits and 21 valid data bits is extracted. A check bit consists of 10 BCH decode bits and 1 parity bit, as shown in Figure 20.

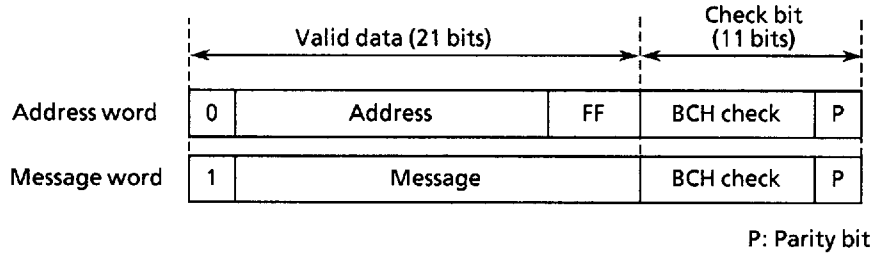


Figure 20 Address and message word configuration

3.1 Error detection based on BCH decode
BCH codes are the result value of the 21 valid data bit divided by the multiple term expression specified by the POCSAG code. By dividing the received address word or message word by the BCH code, the presence and location of error bits are checked. If divisions do not produce any remainder, there are no errors. The remainder value corresponds to the error. The value of the erroneous bits in address words or message words are corrected by the remainder value. The S-7037AF detects three error bits at random. In an address word, up to two error bits are corrected. In a message word, up to 1 error bit is corrected.
The mask option enables correction of four consecutive bits instead of two random bits.

3.2 Error detection based on parity

Parity bits shall be adjusted so that the total sum of the values (number of bits containing 1 as data) at every 32 bits is an even number. If the total sum is an odd number, it is detected as an error. This parity checks are performed after error correction by the BCH decode. A parity error that occurs after error correction by BCH code is processed as an error.
If an address word is erroneous, that address is ignored. If a message word is erroneous, $\overline{\text{ERROR FLAG}}$ goes low, but the message is sent to the CPU.

Table 6 lists the the error processing statuses for received information. In any cases, a message word is sent to CPU.

Table 6 Error processing

BCH error	Correction	Parity error	Address word	$\overline{\text{ERROR FLAG}}$
0 bit		×	Receivable	High
0 bit			Receivable	High
1 bit	×		Receivable	High
1 bit	×	×	Ignored	Low
2 bits	×		Receivable	Low
2 bits	×	×	Ignored	Low
3 bits or more		×	Ignored	Low
3 bits or more			Ignored	Low

4. Expansion function

The S-7037AF performs the functions shown in Table 7, with using two pins such as $\overline{TST}$ and $\overline{TCK}$. These functions are controlled by the CPU, regardless of IC operation.

Table 7

Input		TSTOUT output	Function
$\overline{TST}$	$\overline{TCK}$		
L	L	Sample pulse	Acceleration test (there are four modes)
H	L	Sample pulse	Outputs a tone forcibly

4.1 Acceleration test

If $\overline{TST}$ pin is low during normal status, an acceleration test can be performed. T1 and T0 bits of ID-ROM selects where to enter an acceration input pulse (see Table 8), then input a pulse to $\overline{TCK}$.

Table 8

ID ROM		Pulse input	Acceleration time/ pulse	Note
T1	T0			
0	0	Tone pulse	1/32 s	Substitute for 32 Hz
0	1	Bit counter	1 bit	Input only when BS1 is low
1	0	Wolrd counter	32 bits	
1	1	Batch counter	1 batch	

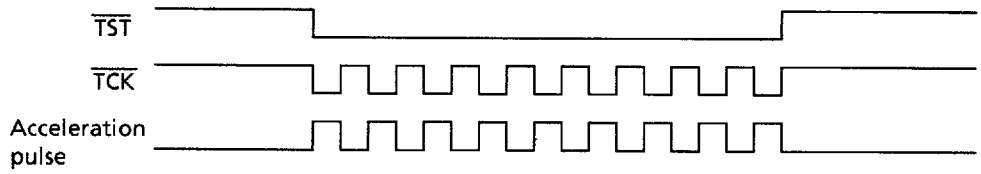


Figure 21 Timing of acceleration input test

4.2 Forcible output of tone

If $\overline{TCK}$ pin becomes low during normal mode, output signals of 2.4 kHz are output from TONEOUT.

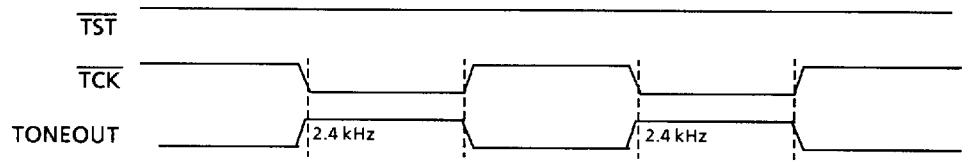


Figure 22 Tone forcible output timing

■ Circuit Design

1. Interface to ID-ROM

1.1 ID-ROM assignment

Using S-2100 as an ID-ROM enables direct connection to the S-7037AF. Table 9 describes the ID-ROM functions, and Table 10 describes bit allocations.

Table 9

Bit name	Functions
$\overline{UE}$*	Address 1 access enable
U17 to U0	Code setting of address 1
$\overline{ME}$*	Address 2 access enable
M17 to M0	Code setting of address 2
F2 to F0	Specify frame in a batch (common to addresses 1 & 2)
R3 to R0	Specify times of retrial when SC is not detected
PR	Preamble detection mode H : Simultaneous detection with SC L: Only preamble detection
T1 to T0	Test mode setting

* When receiving information at address 1, $\overline{UE}$ must be set to low.
Also, when receiving information at address 2, $\overline{ME}$ must be set to low.

Table 10 S-2100 bit allocation

ROM address	0	1	2	3	4	5	6	7
Bit name	0	UE	U17	U16	U15	U14	U13	U12
	8	9	10	11	12	13	14	15
	U11	U10	U9	U8	U7	U6	U5	U4
	16	17	18	19	20	21	22	23
	U3	U2	U1	U0	ME	M17	M16	M15
	24	25	26	27	28	29	30	31
	M14	M13	M12	M11	M10	M9	M8	M7
	32	33	34	35	36	37	38	39
	M6	M5	M4	M3	M2	M1	M0	F2
	40	41	42	43	44	45	46	47
	F1	F0	R3	R2	R1	R0	PR	T1
	48							
	T0							

1.2 interface

The S-7037AF calls and fetches data in ID-ROM. This operation is controlled by the $\overline{\text{ROM-CE}}$, $\overline{\text{ROM-RST}}$, ROMCLK, and ROM-DATA pins.

$\overline{\text{ROM-CE}}$: Chip enable signal of ID-ROM output. If this pin is set to low, the ID-ROM data is fetched.

$\overline{\text{ROM-RST}}$: Reset output.

ROMCLK: Clock signal output for reading ID-ROM data. Outputs 4.8 kHz clock pulses for 48 bits.

ROM-DATA : ID code data input from ID-ROM

Figure 23 shows the interface timing with the S-2100.

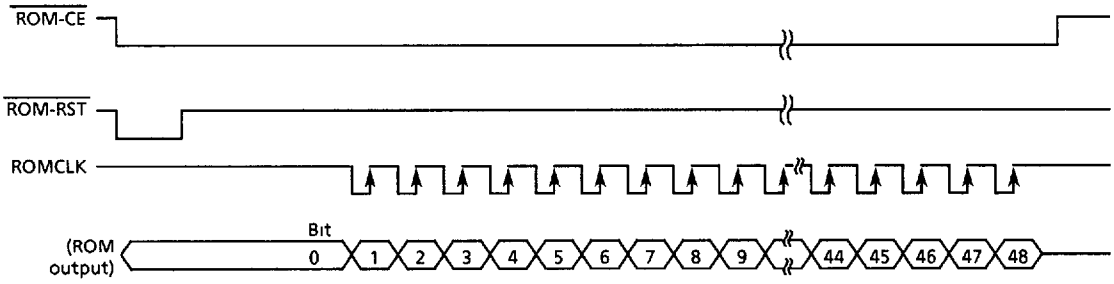


Figure 23 Interface timing with S-2100

2. Interface to CPU (for display pager)
To use the S-7037AF on display pagers, a CPU must be installed between the display unit and the S-7037AF. The received data is decoded and sent to the CPU, and the CPU sends the data to the display. The S-7037AF is provided with nine signal lines for these purposes.

SY-VALID : Indicates that the received POCSAG signal is synchronized (the signal is in the reception area). In preamble detection mode, low is output. Upon SY detection, SY-VALID goes high. When SY-VALID is high, the bit/word counter is synchronized with the received POCSAG signal and can decode it.

$\overline{\text{ADDR-DET}}$: $\overline{\text{ADDR-DET}}$ goes low if address 1 or 2 is detected. When the reception of the message word following the address word is completed, it returns to high.
The message word reception is regarded as being completed in the following cases:
- When the next address word is detected
- When an idle word is detected
- When an SY, inserted between consecutive message words, is not detected

$\overline{\text{RX-CLK}}$, RX-DATA : $\overline{\text{RX-CLK}}$ is a clock signal for sending data. The CPU samples RX-DATA at the falling edge of $\overline{\text{RX-CLK}}$, and fetches data at the rising edge. The RX-DATA pin outputs data to the CPU. Upon message word reception, 20 bits of message data is output per message word.
Figure 24 shows the interface timing of each data item.

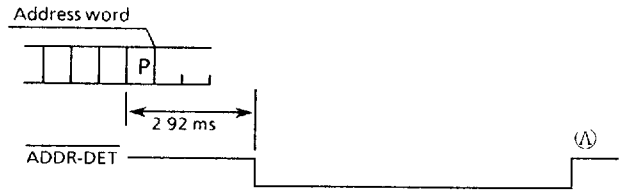
$\overline{\text{URGENT}}$: $\overline{\text{URGENT}}$ goes low when address 1 is received upon address detection.

FUNC1-0 : Kinds of tone, output at calling, is sent to CPU.

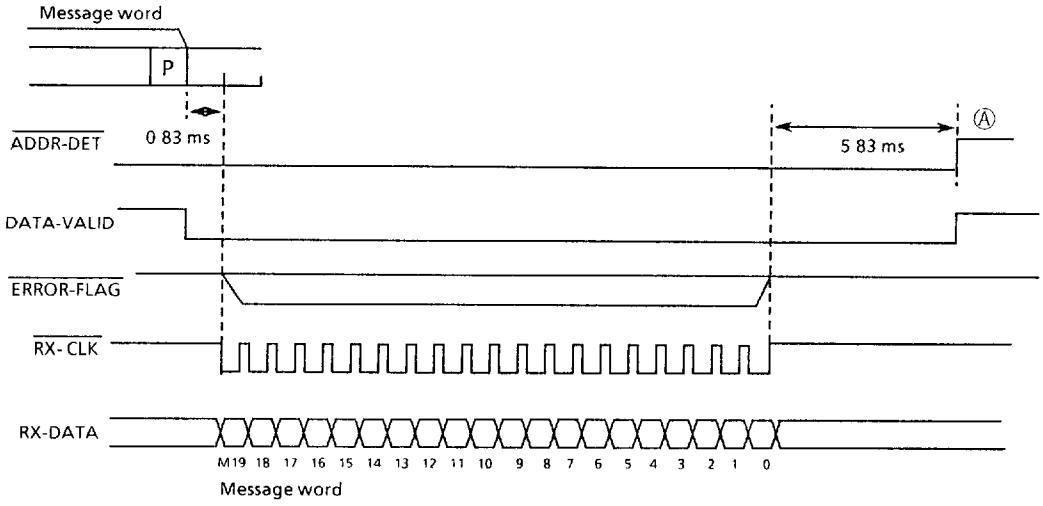
DATA VALID : DATA VALID goes low, synchronized with the ouput timing of valid message.

$\overline{\text{ERROR FLAG}}$: $\overline{\text{ERROR FLAG}}$ is kept to be low while message including an error is sent to CPU.

(1) Address detection



(2) Message detection



Ⓐ $\overline{\text{ADDR-DET}}$ is kept to be low when there is a message word after this.

Figure 24 CPU interface timing

3. Application circuit example

3.1 Tone-only pager

This pager informs the user of reception by tone when a received call signal (address data) is valid. Main peripheral components are ID-ROM, speaker, vibrator, LED, transistor, and crystal oscillator. No CPU is required.

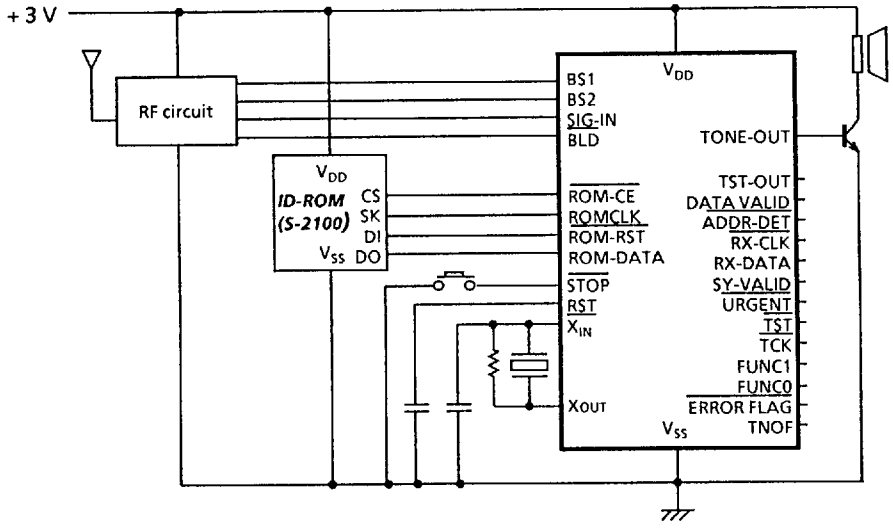


Figure 25 Application circuit example: Tone-only pager

3.2 Display pager

The S-7037AF transmits to the microcomputer only the necessary information, when the received call signal (address data) and the message are valid. The microprocessor, then, informs the user of pager information by displaying the message and tone. A CPU and a display unit are added to a tone-only pager.

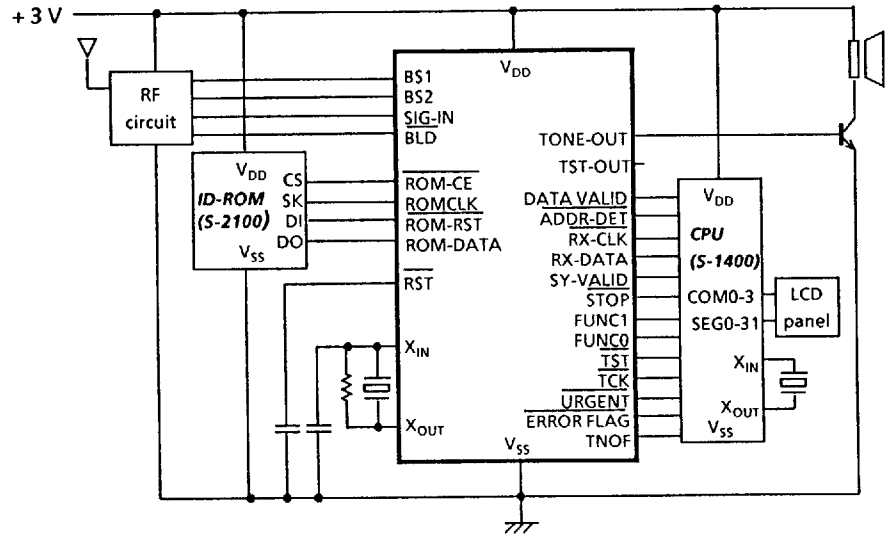


Figure 26 Application circuit example: Display pager