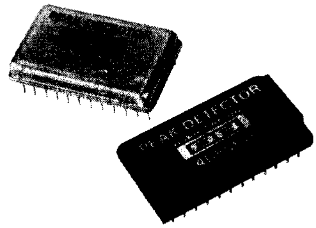
BURR-BROWN®



4085

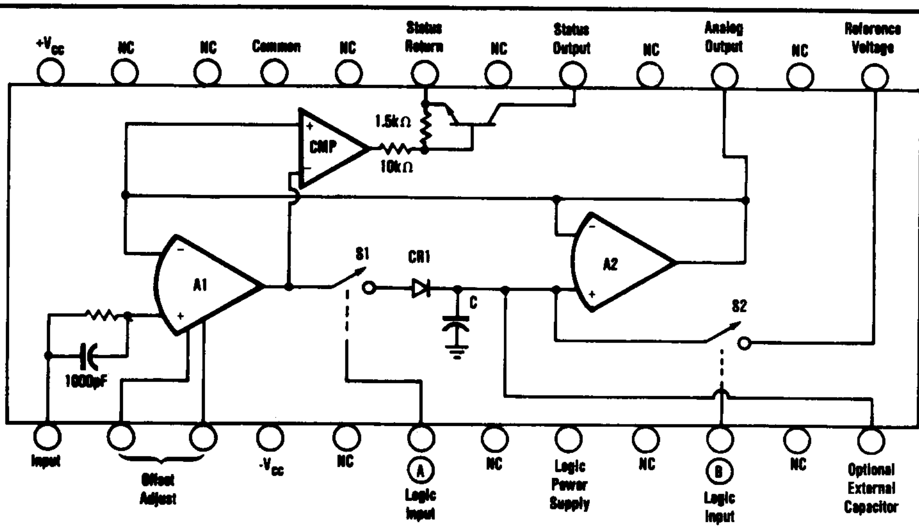
HYBRID MICROCIRCUIT PEAK DETECTOR

FEATURES:

- STORES TRANSIENT VOLTAGES
- COMPLETELY SELF-CONTAINED
- ACCURATE TO ±0.01%
- LOW DROOP ERRORS
- SMALL DIP PACKAGE

DESCRIPTION

The 4085 is a specialized sample/hold amplifier that tracks an input signal until a maximum amplitude is reached. That maximum value is held at the analog output, and the digital Status output indicates that a peak has been detected. The unit can then be commanded to hold that value, ignoring additional peaks, or reset to a user-specified reference voltage. The 4085 detects positive-going peaks from -10V to +10V and is available in a hermetic metal package and a low-cost ceramic package. Three models are available, specified for temperature ranges 0 to +70°C (4085KG), -25°C to +85°C (4085BM), and -55°C to +125°C (4085SM).



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-379A

SPECIFICATIONS

ELECTRICAL

Specification at T_A = +25°C and ±15VDC and +5VDC power supplies unless otherwise noted.

MODEL	4085 MIN	4085 TYP	4085 MAX	UNITS
ANALOG INPUT				
Signal Inputs				
Operating Range	±10	|Vcc|-3		V
Absolute Maximum Range			±Vcc	V
Input Offset Voltage (adjustable to zero)			2	mV
Input Offset Voltage Drift		15	50	μV/°C
Input Bias Current		15	50	pA
Input Resistance		1		GΩ
Input Capacitance		8		pF
DIGITAL INPUT				
Logic Levels				
Logic "1"	+2.4 at 50nA, max			V
Logic "0"			+0.8 at 100μA, max	V
Truth Table	Logic Input A		Logic Input B	
Peak Detect Mode	1		0	
Hold Mode	0		0	
Reset	0		1	
TRANSFER CHARACTERISTICS				
Voltage Gain		1.0		V/V
ACCURACY				
DC Voltage Gain Error			±0.01	% of FSR(1)
Dynamic Accuracy to 300Hz		±0.01	±0.02	% of FSR
Dynamic Accuracy to 100Hz			±0.01	% of FSR
Temperature Coefficient of Gain Error		±3		ppm/°C
Feedthrough			±0.05	% of Step
Droop (all units at T_A = +25°C)(2)			±0.06	mV/msec
T_A = +70°C, 4085KG			±0.5	mV/msec
T_A = +85°C, 4085BM			±1.2	mV/msec
T_A = +125°C, 4085SM			±12.0	mV/msec
Power Supply Sensitivity, ±Vcc			±0.005	%/% Supply Variation
Logic Supply			±0.005	%/% Supply Variation
DYNAMIC PERFORMANCE				
Acquisition Time (BM, SM)			500	μsec
Acquisition Time (KG)			800	μsec
Slew Rate		0.5		V/μsec
Charge Offset(3)		0.5	1	mV
Status Delay at 500Hz		0.7	1	msec
Status Delay at 100Hz		1.2	2	msec

MODEL	4085 MIN	4085 TYP	4085 MAX	UNITS
ANALOG OUTPUT				
Voltage Range	±10	|Vcc|-3		V
Output Current	5			mA
Output Resistance		0.2	0.5	Ω
Output Noise 10Hz to 100kHz		30		μV, rms
Output Load Capacitance	50	100		pF
STATUS OUTPUT				
Collector-emitter Voltage			+30	V
Collector Current			20	mA
DC Current Gain	50	100		mA/mA
V_{BE}		0.65		V
REFERENCE VOLTAGE				
Operating Range	±10	|Vcc|-3		V
Absolute Maximum Range			±Supply	V
Discharge Current(4)	5		30	mA
POWER SUPPLY REQUIREMENTS				
Rated Voltage		±15		V
Operating Range	±8		±18	V
Current Drain (I_{OUT} = 0)			±20	mA
Rated Logic Supply Voltage(5)		+5.0 ±0.5		V
Logic Supply Current				
(Logic A & B high)		3.0 ±0.3		mA
(Logic A & B = 0V)		4.4 ±0.5		mA
TEMPERATURE RANGE				
Specification				
4085KG	0		+70	°C
4085BM	-25		+85	°C
4085SM	-55		+125	°C
Operating				
4085KG	-25		+85	°C
4085BM	-55		+90	°C
4085SM	-55		+125	°C
Storage				
4085KG	-30		+90	°C
4085BM	-60		+100	°C
4085SM	-60		+150	°C

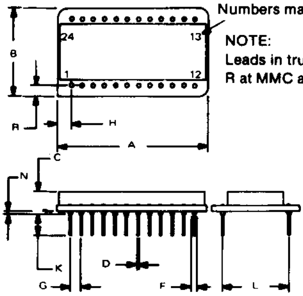
NOTES:

1. FSR = Full Scale Range, 20V for the 4085.
2. Equation for droop: $$\text{Droop (mV/msec)} = \frac{100\text{pA} \times 2^{\left(\frac{T - 25°C}{11}\right)}}{3300\text{pF} + C_{EXT}\text{ (pF)}}$$
3. Charge Offset is the charge transferred from the holding capacitor when the 4085 is switched to the hold mode.
4. Any circuitry connected to the reference pin should be capable of sinking the desired discharge current of the internal 3300pF holding capacitor plus any external capacitor. The discharge current range is the current limit imposed by an internal FET switch. It does not imply that the I_{DSS} of external circuitry must be designed to limit current to this range.
5. Logic Supply, pin 8, may be connected to higher supply voltages for operation with MOS or CMOS logic. Refer to "Operating Instructions".

MECHANICAL

Pin numbers shown for reference only.
Numbers may not be marked on package.

NOTE:
Leads in true position .010" (0.25mm) R at MMC at seating plane.



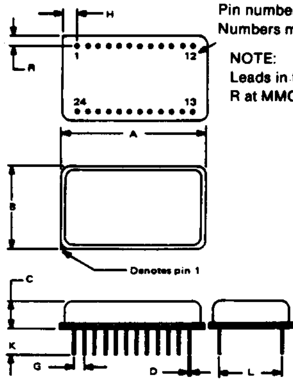
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.310	1.360	33.27	34.54
B	.770	.810	19.56	20.57
C	.150	.210	3.81	5.33
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.110	.130	2.79	3.30
K	.150	.250	3.81	6.35
L	.600 BASIC		15.24 BASIC	
N	.002	.010	0.05	0.25
R	.085	.105	2.16	2.67

ORDER NUMBER:
4085KG

CASE: Black Ceramic (alumina)
MATING CONNECTOR: 245MC
WEIGHT: 8.4 grams (0.3 oz)

Pin numbers shown for reference only.
Numbers may not be marked on package.

NOTE:
Leads in true position .010" (0.25mm) R at MMC at seating plane.



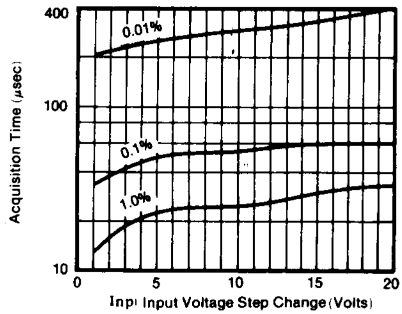
ORDER NUMBER:
4085BM
4085SM

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.365	1.385	34.67	35.18
B	.790	.810	20.07	20.57
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.125	.150	3.18	3.81
K	.150	.300	3.81	7.62
L	.600 BASIC		15.24 BASIC	
R	.080	.110	2.03	2.79

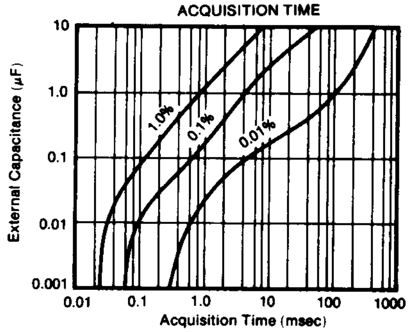
CASE: Kovar, Gold or Nickel plated
MATING CONNECTOR: 245MC
WEIGHT: 8.4 grams (0.3 oz)

TYPICAL PERFORMANCE CURVES

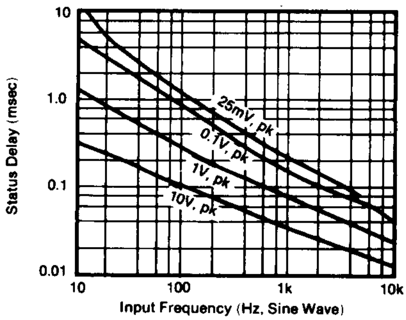
ACQUISITION TIME



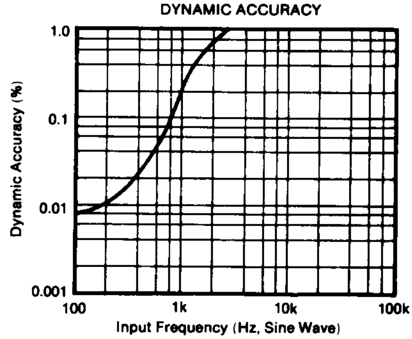
ACQUISITION TIME



STATUS OUTPUT DELAY

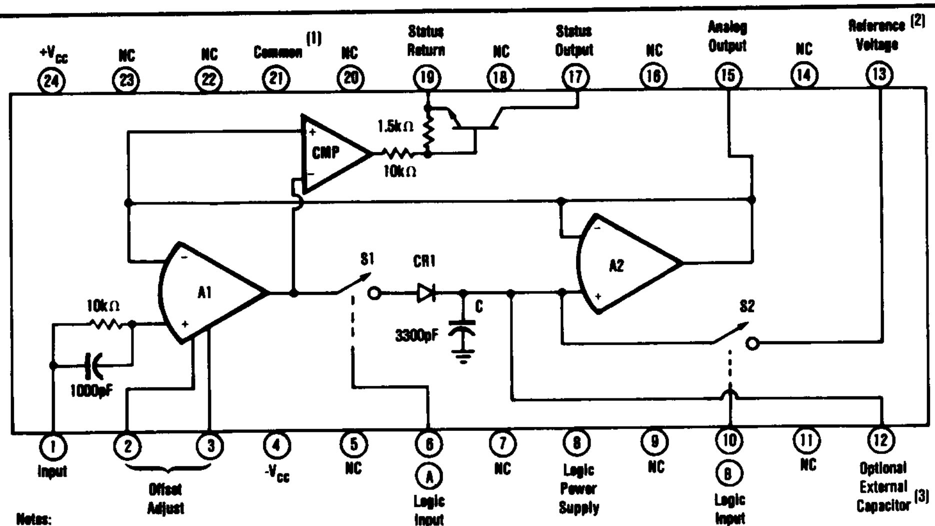


DYNAMIC ACCURACY



THEORY OF OPERATION

In the Peak Detect Mode (S1 closed, S2 open), the analog output tracks the analog input until a peak value is reached. When the input voltage falls below the magnitude of the peak voltage, CR1 becomes reversed biased, and the feedback loop between A1 and A2 is broken. At this point, the status output transistor turns on and the magnitude of the peak voltage is held on the analog output. In the Hold Mode (S1 open, S2 open), the current charging path from the output of A1 to the capacitor is opened. The output voltage is equal to the voltage stored in the capacitor even though the input voltage may become larger than the peak voltage. In the Reset Mode (S1 open, S2 open), the voltage on the capacitor will charge to whatever voltage is applied to the reference voltage input. If both S1 and S2 are closed at the same time, the output of A1 will be connected to the reference voltage input through a low impedance. This represents an illegal mode of operation, but will cause no damage to the unit.



Notes:

1. Pin 21 internally connected to case on 4085BM and 4085SM.
2. Pin 13 must be connected to either power supply common or a user-specified reference voltage. Refer to Application section for details.
3. External capacitor: use polystyrene (up to +85°C), polypropylene, or teflon.

FIGURE 1. 4085 Functional Diagram and Pin Configuration.

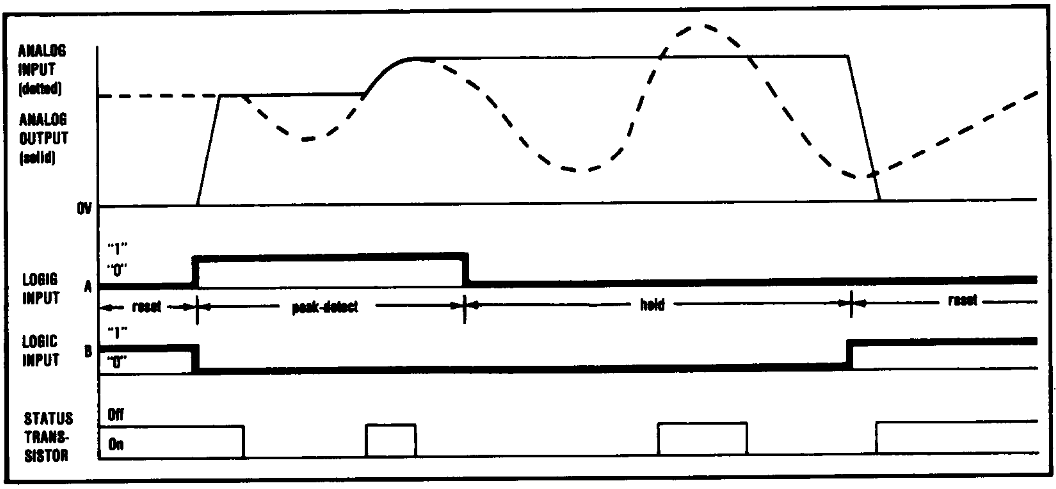


FIGURE 2. Timing Diagram For Peak-Detect Operation.

OPERATING INSTRUCTIONS

OFFSET VOLTAGE ADJUSTMENT

The ±2mV input offset voltage of the 4085 may be nulled to zero by using the circuit shown in Figure 3. With the 4085 in the Peak Detect Mode (logic input A = "1", logic input B = "0") apply zero volts to pin 1. Adjust the potentiometer until the output voltage is zero volts. Disconnect pin 12 after adjustment is made.

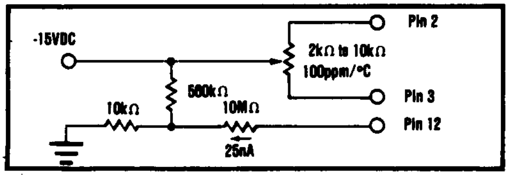


FIGURE 3. Offset Adjust Circuit.

POWER SUPPLY CONSIDERATIONS

The 4085 will operate as specified with power supplies from ±8VDC to ±18VDC. To minimize noise pickup, the supply inputs should be decoupled with 1μF tantalum capacitors located physically close to the unit.

DIGITAL INPUTS AND LOGIC SUPPLY

The digital inputs may be driven with TTL or CMOS logic. Pin 8 should be tied to the logic supply. The logic supply voltage (V_L) may also be provided by connecting pin 8 through a resistor of value R (kΩ) = 1.67 (V_{CC} -V_L)/V_L to the +V_{CC} ($V_{CC} \geqslant V_L$). The logic threshold voltage is equal to 0.4V_L - 0.7V.

INPUT FREQUENCY BANDWIDTH LIMITING

It is recommended that the input bandwidth be limited as much as possible by an RC section such as that shown in Figure 4. This is to limit noise spikes at the input that may cause erroneous readings. If detecting large pulse heights, a 5μsec time constant should be used. This will not degrade acquisition time or tracking accuracy for frequencies up to 500Hz. For input frequencies greater than 500Hz, a smaller time constant may be used.

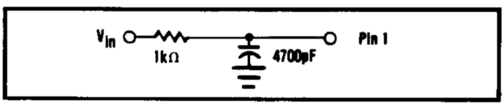


FIGURE 4. Input Bandwidth Limiting.

STATUS OUTPUT CHARACTERISTICS

The open-collector, open-emitter output transistor is a small signal, medium speed switching transistor similar to a 2N2222. To facilitate driving a variety of devices, the configuration of the status output has been left to the user's discretion.

The internal comparator shown in the block diagram (Figure 1) has an output characteristic as follows. Input signal track: $Z_{out} \approx \infty$; peak hold: V_{out} = +V_{CC} - 0.5V.

Several configurations are illustrated in Figures 5, 6, and 7. "Inverting" means logic "0" = peak has been detected. "Noninverting" means logic "1" = peak has been detected.

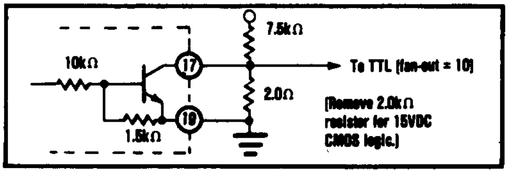


FIGURE 5. Inverting TTL (CMOS) Status Output.

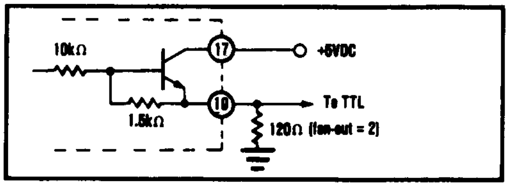


FIGURE 6. Noninverting TTL Status Output.

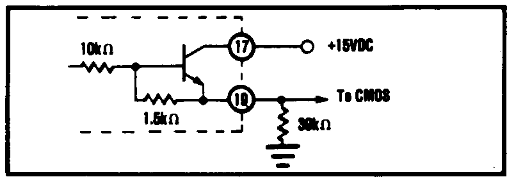


FIGURE 7. Noninverting CMOS Status Output.

DESIGNING IN HYSTERESIS

It may be desirable in some situations to have hysteresis in the circuit such that small peaks will not be detected, eliminating jitter in the Status output. This is possible through external components connected as shown in Figure 8. After a peak is detected, the input voltage must be slightly greater (determined by R1/R2) than the previous peak to cause the output to resume tracking the input. This hysteresis voltage is expressed by:

$$V_H = \frac{(V_{in} - V_E - 0.9V)\,R1}{R1 + R2}$$

The emitter voltage of the status transistor should be tied to a voltage sufficiently lower than the lowest expected peak to allow proper operation.

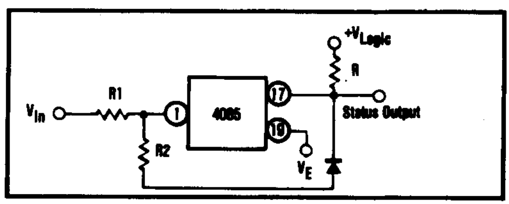


FIGURE 8. Hysteresis.

APPLICATIONS

PEAK CATCHER

This circuit detects and holds the first peak it encounters. After the first peak is detected, it automatically is switched to the Hold Mode. To reset the circuit for catching another peak, a 10μsec or longer positive logic pulse should occur at the Release Input. This will reset the peak detector to the desired voltage and put it in the peak-detect mode.

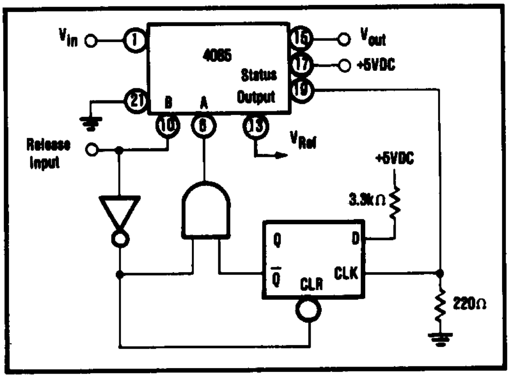


FIGURE 9. Peak Catcher.

NO-RIPPLE, FAST-SETTLING RMS-DC CONVERTER

If a waveform is known, the rms value of the signal may be computed from the peak value. In this circuit, the rms value is computed by the output amplifier from the peak value held by the 4085. The output in the circuit shown is updated manually. It may be updated automatically by replacing the switch circuit with an oscillator plus timing logic.

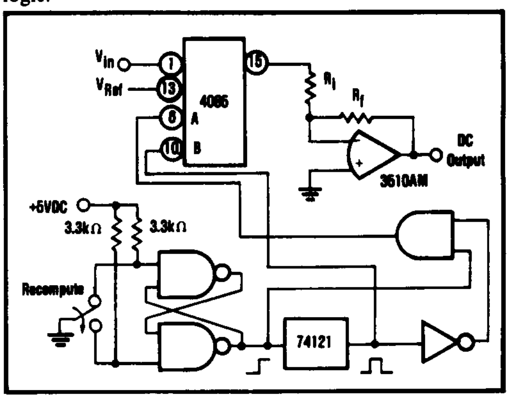


FIGURE 10. RMS-DC Converter.

INTERFACING TO A/D CONVERTER

Interfacing to an A/D converter is straightforward. The gating of the A/D converter command allows a conversion only if a peak has been detected and permits completion of each conversion. If a peak occurs while the A/D is converting, it will not be detected.

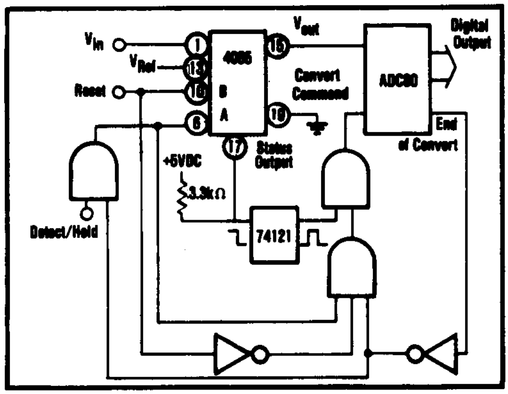


FIGURE 11. A/D Converter Interface.

PEAK-TO-PEAK DETECTOR

Figure 12 shows a circuit that will display the peak-to-peak voltage of an input waveform. The Status Output indicates that both positive and negative peaks have been detected and that the output is valid. The resistors around A3 should be matched to insure good common-mode rejection.

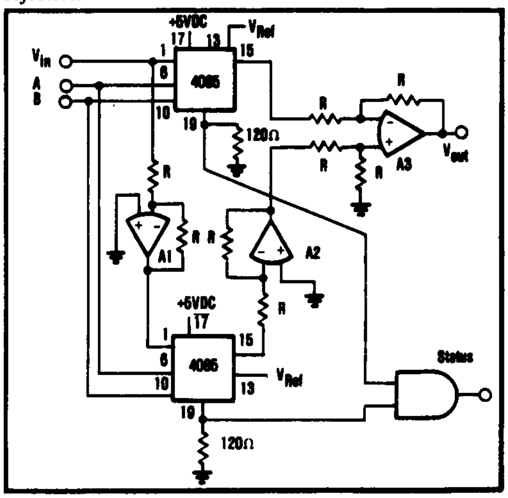


FIGURE 12. Peak-to-Peak Detector.

REFERENCE VOLTAGE

In the Reset Mode the voltage applied to pin 13 places an initial charge on the holding capacitor at the input to A2 (see Figure 1). This threshold voltage may be any value between positive and negative 10 volts. For most applications pin 13 will be tied to power supply common. This sets V_{Ref} to 0 volts. The 4085 will then capture peaks greater than 0 volts.

Pin 13 must be connected to either power supply common or to a user-specified reference voltage. If this connection is not made the 4085 will appear to have excessive droop.