

TM4256EC4 262,144 BY 4-BIT DYNAMIC RAM MODULE

SEPTEMBER 1985—REVISED MAY 1988

- 262,144 × 4 Organization
- Single 5-V Supply (10% Tolerance)
- 22-Pin Single-in-line Package (SIP)
- Utilizes Four 256K Dynamic RAMs in Plastic Chip Carrier
- Long Refresh Period . . . 4 ms (256 Cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance of Unmounted RAMs:

	ACCESS TIME	ACCESS TIME	READ OR WRITE CYCLE
	ROW ADDRESS (MAX)	COLUMN ADDRESS (MAX)	(MIN)
TMS4256-10	100 ns	50 ns	200 ns
TMS4256-12	120 ns	60 ns	230 ns
TMS4256-15	150 ns	75 ns	260 ns

- Common $\overline{\text{CAS}}$ Control with Separate Data Input and Output Lines
- Low Power Dissipation
- Operating Free-Air Temperature . . . 0°C to 70°C

description

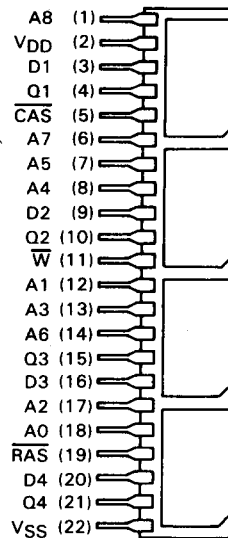
The TM4256EC4 series is a 1024K, dynamic random-access memory module, organized as 262,144 × 4 bits in a 22-pin single-in-line package comprising four TMS4256FML, 262,144 × 1 bit dynamic RAMs in 18-lead plastic chip-carriers mounted on top of a substrate together with decoupling capacitors mounted beneath the chip carriers. The onboard capacitors eliminate the need for bypassing on the motherboard and offer superior performance over equivalent leaded capacitors due to reduced lead inductance. Also, with 0.3 inch board spacing, the TM4256EC4 has a density of ten devices per square inch (approximately 4 × the density of DIPs). With the elimination of bypass capacitors on the motherboard, reduced PC board size, and fewer plated through-holes, a cost savings can be realized.

Each TMS4256FML is described in its data sheet and is fully electrically tested and processed according to TI MIL-STD-883B flows (as amended for commercial applications) prior to assembly. After assembly onto the SIP, a further set of electrical tests is performed.

The TM4256EC4 features $\overline{\text{RAS}}$ access times of 100 ns, 120 ns, and 150 ns maximum.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with $\overline{\text{RAS}}$ in order to retain data. $\overline{\text{CAS}}$ can remain high during the refresh sequence to conserve power.

TM4256EC4 . . . C SINGLE-IN-LINE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE
TM4256EC4

A0-A8	Address Inputs
$\overline{\text{CAS}}$	Column-Address Strobe
D1-D4	Data Inputs
Q1-Q4	Data Outputs
$\overline{\text{RAS}}$	Row-Address Strobe
VDD	5-V Supply
VSS	Ground
$\overline{\text{W}}$	Write Enable

Dynamic RAM Modules

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PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.


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All inputs and outputs, including clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TM4256EC4 is rated for operation from 0°C to 70°C.

operation

The TM4256EC4 operates as four TMS4256FMLs connected as shown in the functional block diagram. Refer to the TMS4256 data sheet for details of operation.

specifications

For TMS4256FML electrical specifications, refer to the TMS4256 data sheet.

single-in-line package and components

PC substrate: 0,79 mm (0.031 inch) minimum thickness

Bypass capacitors: Multilayer ceramic

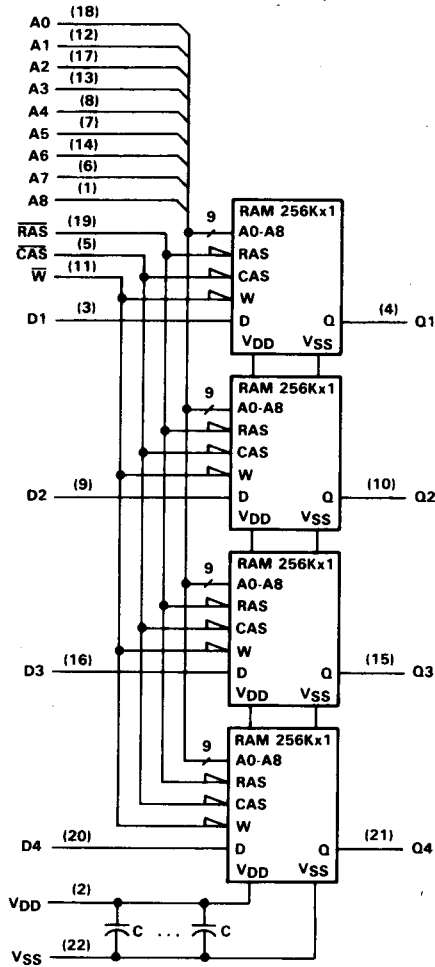
Leads: Tin/lead solder coated over phosphor-bronze

TM4256EC4
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functional block diagram

Dynamic RAM Modules

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TM4256EC4
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Dynamic RAM Modules

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin, including V _{DD} supply (see Note 1)	-1 V to 7 V
Short circuit output current for any output	50 mA
Power dissipation	4 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

	MIN	NOM	MAX	UNIT
V _{DD} Supply voltage	4.5	5	5.5	V
V _{SS} Supply voltage		0		V
V _{IH} High-level input voltage	2.4		6.5	V
V _{IL} Low-level input voltage (see Note 2)	-1		0.8	V
T _A Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TM4256EC4-10		TM4256EC4-12		UNIT
		MIN	MAX	MIN	MAX	
V _{OH} High-level output voltage	I _{OH} = -5 mA	2.4	V _{DD}	2.4	V _{DD}	V
V _{OL} Low-level output voltage	I _{OL} = 4.2 mA	0	0.4	0	0.4	V
I _I Input current (leakage)	V _I = 0 V to 6.5 V, V _{DD} = 5 V, All other pins = 0 V	±10		±10		µA
I _O Output current (leakage)	V _O = 0.4 V to 5.5 V, V _{DD} = 5 V, $\overline{\text{CAS}}$ high	±10		±10		µA
I _{DD1} ‡ Average operating current during read or write cycle	t _c = minimum cycle, All outputs open	280		260		mA
I _{DD2} ‡ Standby current	After 1 memory cycle, RAS and $\overline{\text{CAS}}$ high, All outputs open	18		18		mA
I _{DD3} ‡ Average refresh current	t _c = minimum cycle, $\overline{\text{CAS}}$ high and RAS cycling, All outputs open	232		212		mA
I _{DD4} ‡ Average page-mode current	t _{c(P)} = minimum cycle, RAS low and $\overline{\text{CAS}}$ cycling, All outputs open	200		180		mA

‡I_{DD1}-I_{DD4} are measured with Q1-Q4 in the same mode (i.e., operating, standby, refresh, page mode).

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electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TM4256EC4-15		UNIT
		MIN	MAX	
V _{OH} High-level output voltage	I _{OH} = -5 mA	2.4	V _{DD}	V
V _{OL} Low-level output voltage	I _{OL} = 4.2 mA	0	0.4	V
I _I Input current (leakage)	V _I = 0 V to 6.5 V, V _{DD} = 5 V, All other pins = 0 V		±10	μA
I _O Output current (leakage)	V _O = 0.4 V to 5.5 V, V _{DD} = 5 V, $\overline{\text{CAS}}$ high		±10	μA
I _{DD1} [†] Average operating current during read or write cycle	t _c = minimum cycle, All outputs open		240	mA
I _{DD2} [†] Standby current	After 1 memory cycle, $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ high, All outputs open		18	mA
I _{DD3} [†] Average refresh current	t _c = minimum cycle, $\overline{\text{CAS}}$ high and $\overline{\text{RAS}}$ cycling, All outputs open		192	mA
I _{DD4} [†] Average page-mode current	t _{c(P)} = minimum cycle, $\overline{\text{RAS}}$ low and $\overline{\text{CAS}}$ cycling, All outputs open		160	mA

[†]I_{DD1}-I_{DD4} are measured with Q1-Q4 in the same mode (i.e., operating, standby refresh, page mode).

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER	MIN	MAX	UNIT
C _{i(A)} Input capacitance, address inputs		20	pF
C _{i(D)} Input capacitance, data inputs		5	pF
C _{i(RAS)} Input capacitance, $\overline{\text{RAS}}$ input		20	pF
C _{i(W)} Input capacitance, $\overline{\text{W}}$ input		28	pF
C _{i(CAS)} Input capacitance, $\overline{\text{CAS}}$ input		20	pF
C _{o(Q)} Output capacitance, data outputs		7	pF
C _{o(VDD)} Decoupling capacitance	0.4		μF