DATA SHEET

IP4100 series
9-channel IEEE 1284 filter/termination with 2 kV ESD protection

Preliminary specification
File under Advanced Ceramics and Modules, ACM4

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Philips Components

PHILIPS

9-channel IEEE 1284 filter/termination with 2 kV ESD protection

IP4100 series

FEATURES

- 9-channel RC filter array with pull-up resistors
- ESD protection: >2 kV
- Undershoot protection
- High capacitance range
- Available in 20-pin or 24-pin QSOP and 20-pin SOIC packages.

APPLICATIONS

IEEE 1284 filter/termination for:

- Workstations
- Desktop and portable computers
- PDAs
- PCMICA cards.

DESCRIPTION

The Philips IP4100 series of Application Specific Integrated Products (ASIPs) is a 9-channel solution for termination and filtering for high speed IEEE 1284 parallel interfaces while also providing ESD protection of >2 kV. IP4100 devices are fabricated using thin film-on-silicon technology and integrates 18 resistors, 9 capacitors and 18 diodes in various package configurations.

The IP4100 is configured as low pass filters with high impedance pull-ups. As filters, the IP4100 will pass low frequency digital data and attenuate undesired high frequency signals. As terminations, the IP4100 will reduce reflections caused by transmission line effects of long cable lines.

The integral diodes of the IP4100 provide ESD protection of <2 kV. Furthermore, the diodes help maintain signal integrity on digital transmission lines by reducing logic undershoot conditions.

QUICK REFERENCE DATA

DESCRIPTION	VALUE
Electrical characteristics at 25 °C	
Resistance	±10%; see Table 1
Capacitance	±20%; see Table 1
Operating voltage, V_{CC}	0 to +5.5 V
ESD protection	IEC 61000-4-2, level 1 (2 kV)
Power rating per channel	100 mW, package limited
Package ratings	
Maximum dissipation at:	
T_{amb} = 70 °C	1 W
T_{amb} = 85 °C	0.83 W
Operating temperature	–25 to +85 °C
Storage temperature	–60 to +150 °C

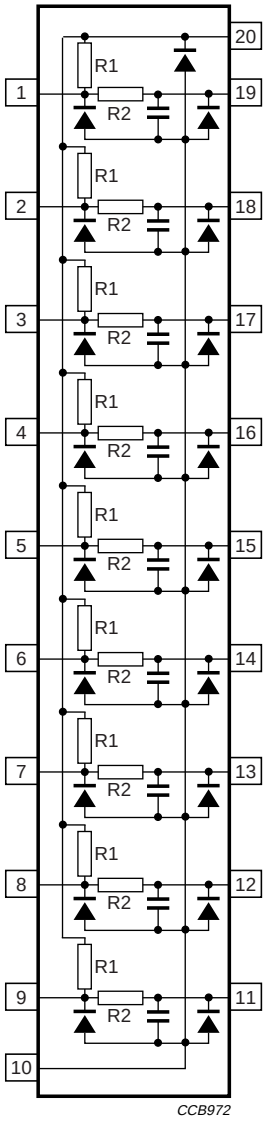


Fig.1 Functional diagram for 20-pin packages.

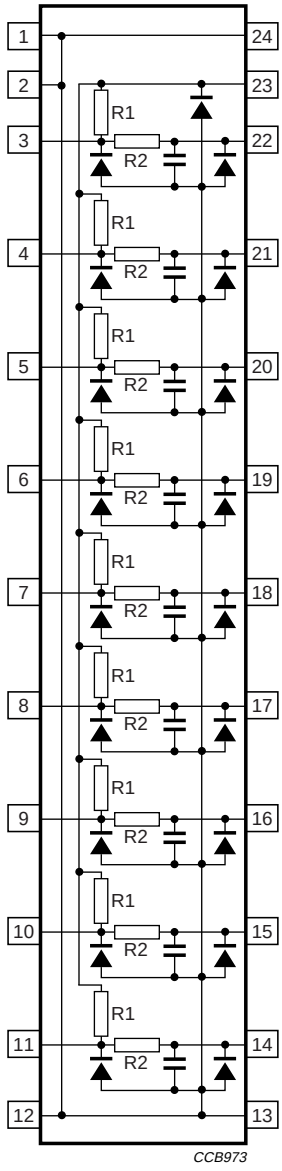
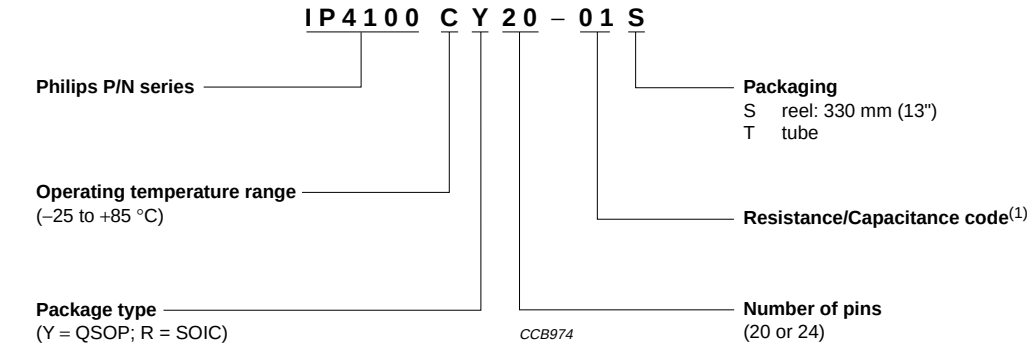


Fig.2 Functional diagram for 24-pin packages.

ORDERING INFORMATION

Ordering code



(1) For R/C codes, see Table 1.

Table 1 Standard R/C values, ordering information and packaging quantities

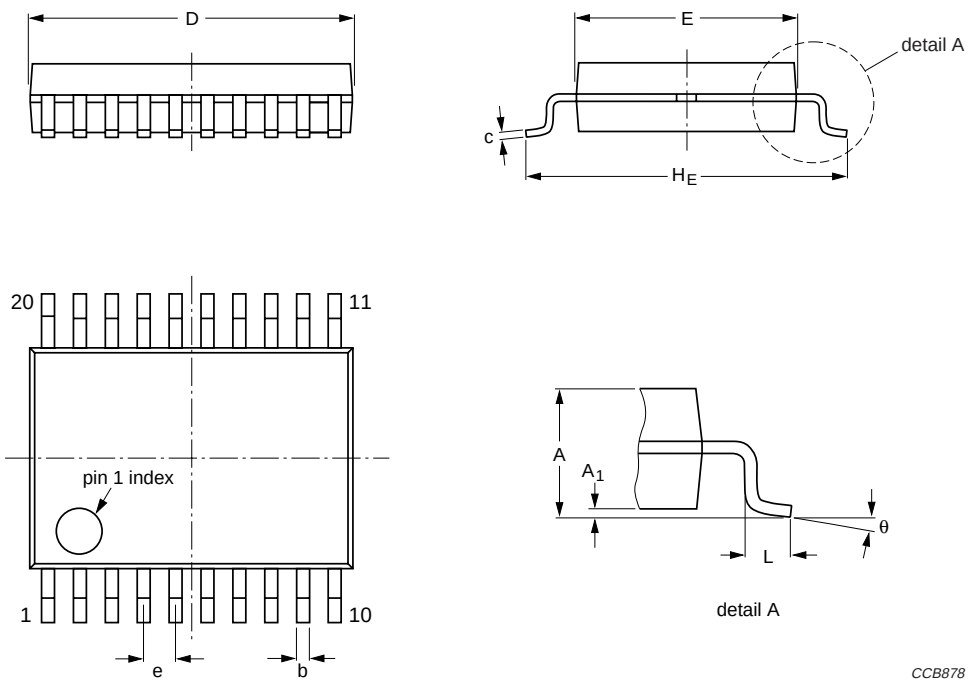
R/C CODES	RESISTANCE VALUE		CAPACITANCE VALUE (pF)	CATALOGUE NUMBER IP4100CY(R)20(24)-...	
	R1 (kΩ)	R2 (Ω)		REEL 330 mm (13") 1000 units	TUBE 55 units(1)
-01	4.7	33	180	01S	01T
-02	2.2	33	220	02S	02T
-03	1.0	33	180	03S	03T

Note

1. The QSOP package has a tube quantity of 56 units.

PACKAGING

SOIC20 Package outline



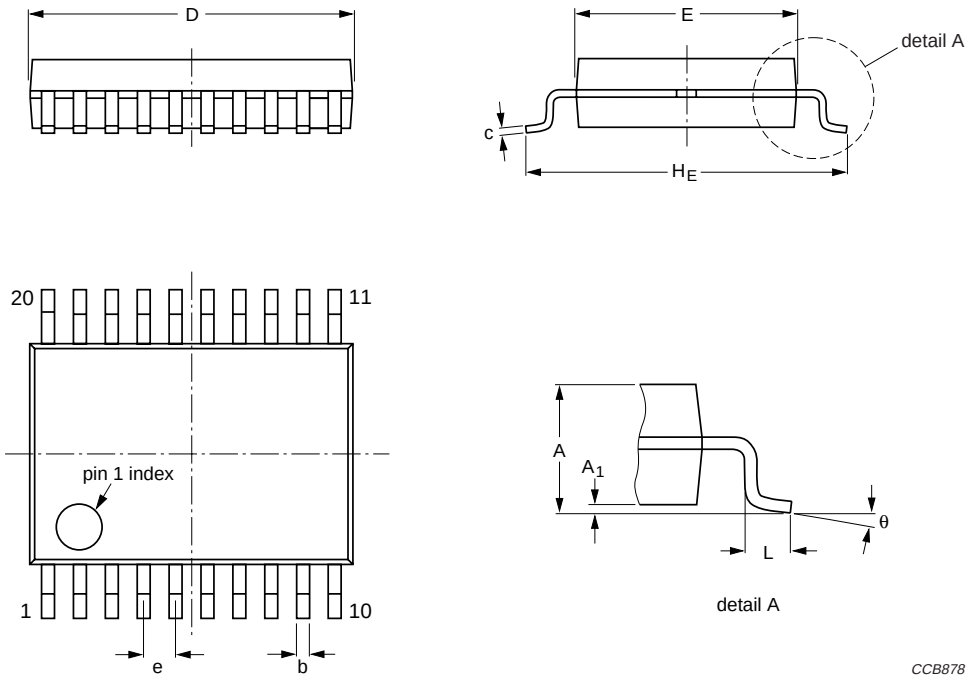
For dimensions see Table 2.

Fig.3 SOIC20 plastic shrink small outline package; 20 leads; wide body 7.39 mm.

Table 2 Package dimensions; see Fig.3

DIMENSION	VALUE		UNIT
	MIN.	MAX.	
A	2.43	2.64	mm
A_1	0.10	0.30	mm
b	0.36	0.46	mm
c	0.23	0.32	mm
D	12.65	12.85	mm
E	7.39	7.60	mm
H_E	10.06	10.52	mm
e	1.27 NOM.		mm
L	0.51	1.02	mm
θ	0	8	deg

QSOP20 Package outline



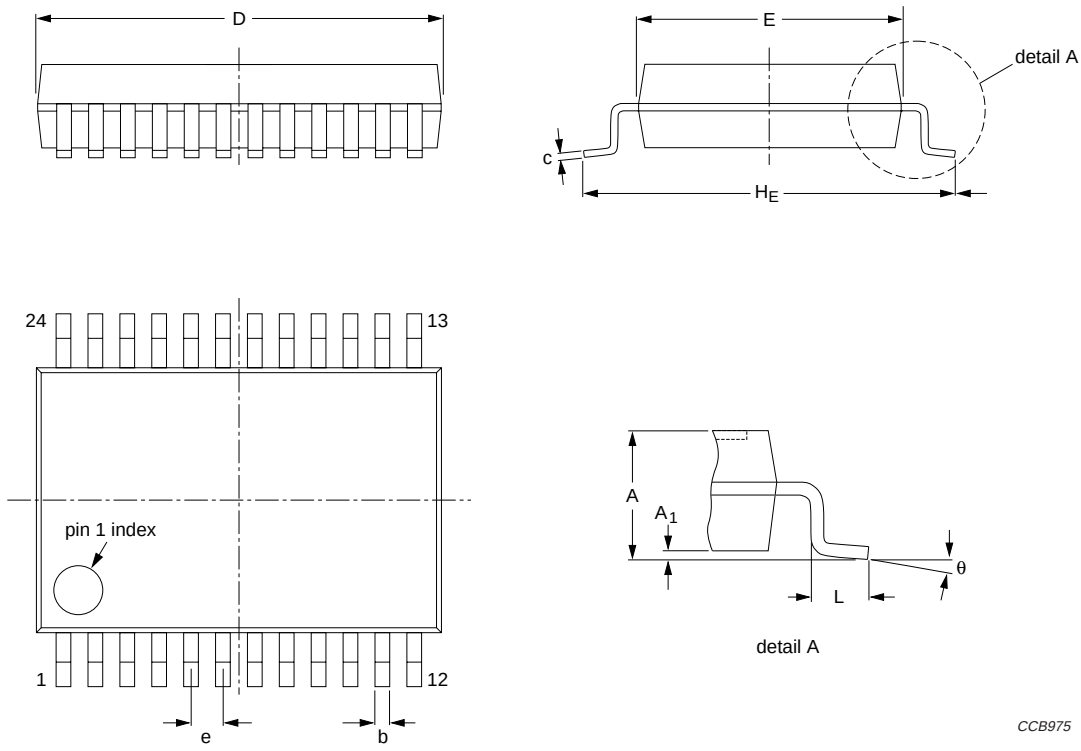
For dimensions see Table 3.

Fig.4 QSOP20 plastic shrink small outline package; 20 leads; narrow body width 3.81 mm.

Table 3 Package dimensions; see Fig.4

DIMENSION	VALUE		UNIT
	MIN.	MAX.	
A	1.35	1.75	mm
A_1	0.10	0.30	mm
b	0.20	0.30	mm
c	0.15	0.25	mm
D	8.55	8.74	mm
E	3.81	3.99	mm
H_E	5.79	6.20	mm
e	0.635 NOM.		mm
L	0.40	1.27	mm
θ	0	8	deg

QSOP24 Package outline



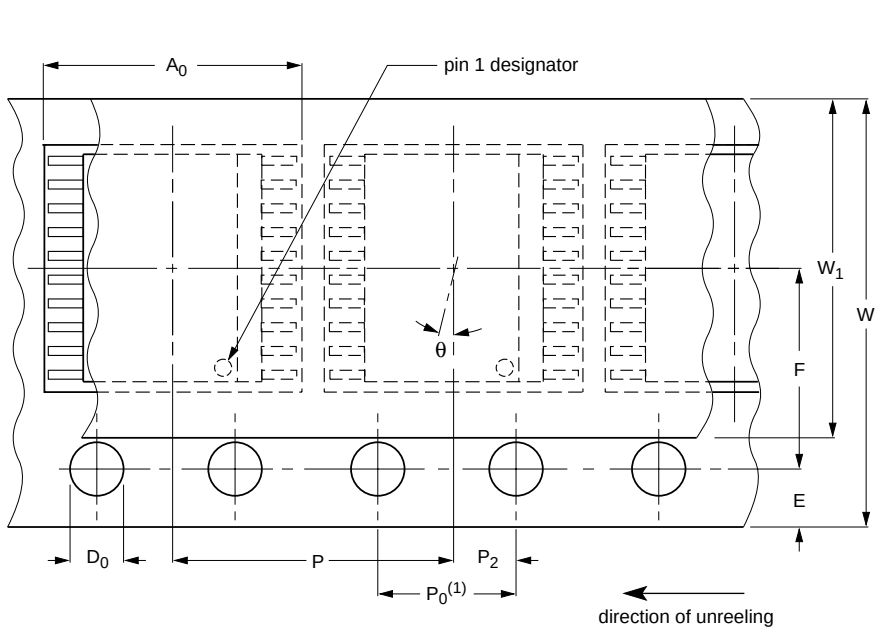
For dimensions see Table 4.

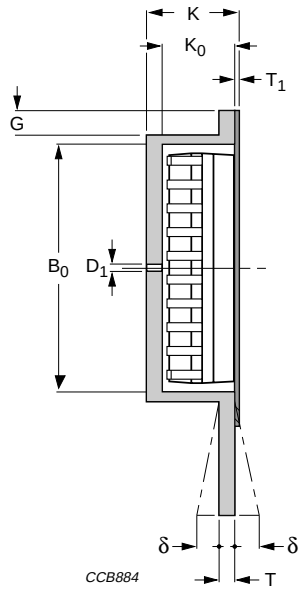
Fig.5 QSOP24 plastic shrink small outline package; 20 leads; narrow body width 3.81 mm.

Table 4 Package dimensions; see Fig.4

DIMENSION	VALUE		UNIT
	MIN.	MAX.	
A	1.35	1.75	mm
A_1	0.10	0.30	mm
b	0.20	0.30	mm
c	0.15	0.25	mm
D	8.55	8.74	mm
E	3.81	3.99	mm
H_E	5.79	6.20	mm
e	0.635 NOM.		mm
L	0.40	1.27	mm
θ	0	8	deg

Blister tape specifications





K_0: so chosen that the orientation of the component cannot change.
For dimensions see Table 5.
(1) Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Fig.6 Blister tape.

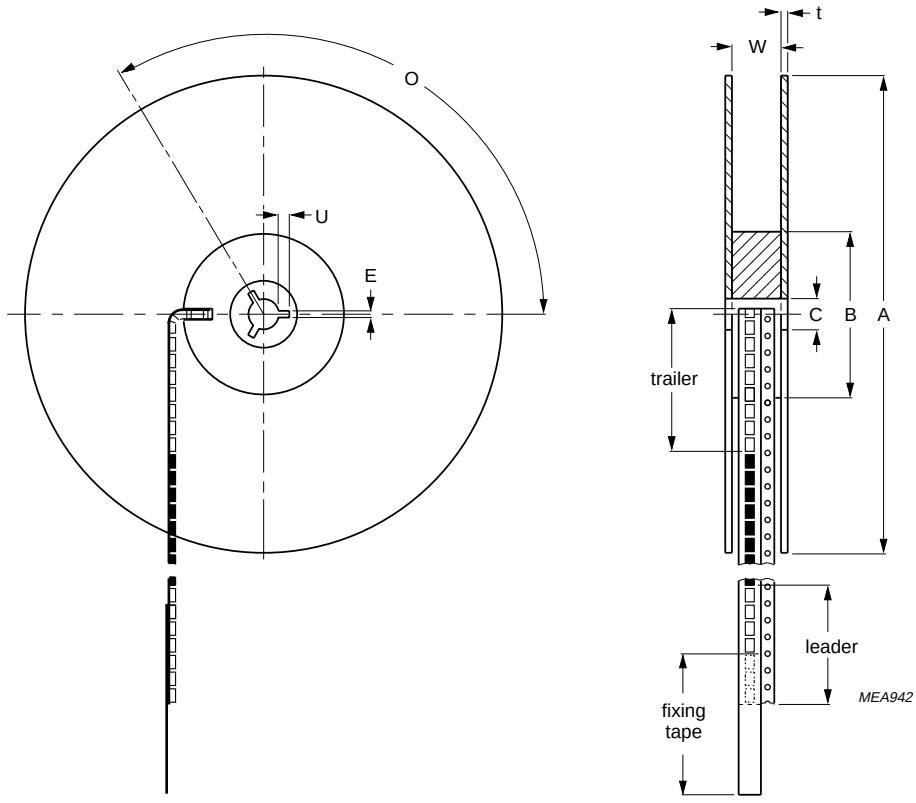
Table 5 Dimensions of blister tape; see Fig.6

PARAMETER	DIMENSION (mm)		TOLERANCE (mm)
	QSOP20/24 PACKAGE	SOIC20 PACKAGE	
A_0 nominal clearance; note 1	6.5	10.9	±0.1
B_0 nominal clearance; note 1	9.0	13.3	±0.1
K_0 minimum clearance; note 1	2.3	3.0	±0.1
K	<2.4	<3.2	–
G	>0.75	>0.75	–
Θ	<15°	<15°	–
δ	<0.3	<0.3	–
W	16.0	24.0	±0.3
E	1.75	1.75	±0.1
F	7.5	7.5	±0.1
D_0	1.5	1.5	+0.1/–0.0
$D_{1\ min}$	1.5	1.5	–
P_0; note 2	4.0	4.0	±0.1
P	8.0	12.0	±0.1
P_2	2.0	2.0	±0.1
T	<0.35	<0.35	–
T_1	<0.1	<0.1	–

Notes

1. Typical displacement in pocket.
2. P_0 pitch tolerance over any 10 pitches is ±0.2 mm.

Reel specifications



For dimensions see Table 6.
Minimum trailer length: 160 mm.
Minimum leader length: 390 mm.

Fig.7 Reel.

Table 6 Reel dimensions; see Fig.7

TAPE WIDTH (mm)	A NOM. (mm)	t (mm)	W (mm)	B (mm)	C (mm)	E MIN. (mm)	U MIN. (mm)	O
16	330	3 +0.0/–1.5	16.4 +2.0/–0.0	101 ±1.5	13 +0.5/–0.2	1.5	3.6	120°
24	330	3 +0.0/–1.5	24.4 +2.0/–0.0	101 ±1.5	13 +0.5/–0.2	1.5	3.6	120°

QUALITY AND RELIABILITY

Wafer fabrication and packaging technology

Philips ASIPs use well-proven semiconductor industry thin film-on-silicon fabrication and packaging technologies. Wafers are processed in a clean room wafer fabrication environment with circuit elements defined using a photolithography process. Metal disposition is performed by precision sputter process. Finished wafers are diced, assembled and tested in a state-of-the-art assembly and packaging facility fully compliant with ISO 9002.

Tests and requirements

The following tests have been conducted on representative samples of Philips ASIPs in QSOP (SSOP), SOIC and similar industry standard plastic packages in accordance with the appropriate IEC, EIA and EIAJ requirements.

Table 7 Test procedures and requirements

EIA/JESD22 TEST METHOD	TEST	PROCEDURE	REQUIREMENTS
B102-A	solderability (after ageing)	8 hours steam; immersed for 5 s in a solder bath at 215 °C	good tinning (≥95% covered); no visible damage
A113-A	SMD sequential stress	preconditioning; 5 cycles: –55 to +125 °C; 24 hours bake; temperature and humidity soak; 3 cycles of IR convection reflow at maximum 220 °C	device functional; no visible damage; SAT inspection
A104-A	temperature cycling	1000 cycles: 10 minutes minimum at –65 °C 10 minutes minimum at +150 °C	no visible damage; ΔR/R max.: ±1%; ΔC/C max.: ±1%
A102-B	autoclave (pressure pot)	336 hours: 121 °C, 100% RH	no visible damage; ΔR/R max.: ±1%; ΔC/C max.: ±1%
A101-B	temperature; humidity; bias	1000 hours: 85 °C; 85% RH; reverse voltage bias	no visible damage; ΔR/R max.: ±1%; ΔC/C max.: ±1%
A108-A	high temperature reverse bias	1000 hours: 125 °C; reverse voltage bias	no visible damage; ΔR/R max.: ±1%; ΔC/C max.: ±1%
A108-A	high temperature operating life	1000 hours: 125 °C; each channel with maximum power per spec.	no visible damage; ΔR/R max.: ±1%; ΔC/C max.: ±1%

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.