FINITION OF TERMS

SCRIPT TERMS:

Forward, applying to LOW inputs.

HIGH, applying to a HIGH logic level or when used with V_{CC} to cate high V_{CC} value.

nput.

LOW, applying to LOW logic level or when used with V_{CC} to cate low V_{CC} value.

Output.

Reverse, applying to HIGH inputs.

ICTIONAL TERMS:

B_1 Inputs The TRUE data inputs for Adder FA1.

$\overline{A}_2$, B_2, $\overline{B}_2$ Inputs The TRUE and FALSE data inputs for Adder

$\overline{C}_2$ Inputs The Carry or 3rd data input for Adders FA1 and

Output The FALSE Carry Output for Adder FA1.

Output The TRUE Carry Output for Adder FA2.

-Out The logic HIGH or LOW output drive capability in terms nput Unit Loads.

t Unit Load One T²L gate input load. In the HIGH state it is al to I_R and in the LOW state it is equal to I_F.

ble Carry Parallel Adder The sum of two binary numbers is ned one bit time after the presence of these data at the adder uts. The bit time is chosen to allow the carry term to propagate n the least significant addition to the most significant addition. ar to Figure

S_2 Output The TRUE Sum Outputs for Adders FA1 and FA2.

$\overline{S}_2$ Output The FALSE Sum Outputs for Adders FA1 and FA2.

ERATIONAL TERMS:

Forward input load current, for unit input load.

Output HIGH current, forced out of output in V_{OH} test.

Output LOW current, forced into the output in V_{OL} test.

Reverse input current with V_R applied to input.

The current drawn by the device under maximum power supply erating voltage and current conditions.

gative Current Current flowing out of the device.

itive Current Current flowing into the device.

Forward LOW input voltage, for forward input current (I_F) test.

Minimum logic HIGH input voltage.

Maximum logic LOW input voltage.

Minimum logic HIGH output voltage with output HIGH current flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} into output.

V_R Input reverse HIGH voltage applied for input leakage current, (I_R) test.

SWITCHING TERMS: (All switching times are measured at the 1.5 V logic level)

$t_{pd+}(CC_0)$ The propagation delay measured from the Carry Input signal transition of either adder to the corresponding LOW-HIGH transition of the Carry Output signal.

$t_{pd-}(CC_0)$ The propagation delay measured from the Carry Input signal transition of either adder to the corresponding HIGH-LOW transition of the Carry Output signal.

$t_{pd+}(A_1\overline{S}_1)$ The propagation delay measured from Adder 1 A or B Data Input signal transition to the LOW-HIGH transition of the FALSE Sum Output signal.

$t_{pd-}(A_1\overline{S}_1)$ The propagation delay measured from Adder 1 A or B Data Input signal transition to the HIGH-LOW transition of the FALSE Sum Output signal.

$t_{pd+}(A_1S_1)$ The propagation delay measured from Adder 1 A or B Data Input signal transition to the LOW-HIGH transition of the TRUE Sum Output signal.

$t_{pd-}(A_1S_1)$ The propagation delay measured from Adder 1 A or B Data Input signal transition to the HIGH-LOW transition of the TRUE Sum Output signal.

$t_{pd+}(\overline{A}_2S_2)$ The propagation delay measured from Adder 2 A or B FALSE Data Input signal transition to the LOW-HIGH transition of the TRUE Sum Output signal.

$t_{pd-}(\overline{A}_2S_2)$ The propagation delay measured from Adder 2 A or B FALSE Data Input signal transition to the HIGH-LOW transition of the TRUE Sum Output signal.

$t_{pd+}(A_2\overline{S}_2)$ The propagation delay measured from Adder 2 A or B Data Input signal transition to the HIGH-LOW transition of the FALSE Sum Output signal.

$t_{pd-}(A_2\overline{S}_2)$ The propagation delay measured from Adder 2 A or B Data Input signal transition to the LOW-HIGH transition of the FALSE Sum Output signal.

$t_{pd+}(A_2S_2)$ The propagation delay measured from Adder 2 A or B Data Input signal transition to the LOW-HIGH transition of the TRUE Sum Output signal.

$t_{pd-}(A_2S_2)$ The propagation delay measured from Adder 2 A or B Data Input signal transition to the HIGH-LOW transition of the TRUE Sum Output signal.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 24 to Pin 12) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current (Note 1)	−30 mA to +5 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am930859X T_A = 0°C to +75°C V_{CC} = 5.0 V ±5%
Am930851X T_A = −55°C to +125°C V_{CC} = 5.0 V ±10%

Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.72 mA V_{IN} = V_{iH} or V_{iL}		2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 14.4 mA V_{IN} = V_{iH} or V_{iL}			0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_{iL} (Note 2)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4 V			−1.0	−1.6	mA
I_{iH} (Note 2)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4 V			6.0	40	μA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V				1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0 V		−20		−70	mA
I_{CC}	Power Supply Current	All other inputs = 4.5 V V_{CC} = MAX.	Am930851X		65	100	mA

Notes: 1) Typical Limits are at V_{CC} = 5.0 V, 25°C Ambient and maximum loading.
2) Actual input currents are obtained by multiplying unit load current by input load factor (See Loading Rules).

SWITCHING CHARACTERISTICS (T_A = 25°C)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{pd+} ($\overline{E}$)	Enable to Output HIGH	V_{CC} = 5.0 V C_L = 15 pF	10	19	30	ns
t_{pd-} ($\overline{E}$)	Enable to Output LOW		6	12	18	
t_{pd+} (D)	Data to Output HIGH		8	16	20	ns
t_{pd-} (D)	Data to Output LOW		6	12	18	
t_s "H"	HIGH Data Set-up Time		−4	0	6	ns
t_s "L"	LOW Data Set-up Time		4	7	10	
t_{pw} ($\overline{E}$)	Min. Enable Pulse Width			8	15	ns
t_{pw} ($\overline{MR}$)	Min. Master Reset Pulse Width			10	15	ns
t_{pd-} ($\overline{MR}$)	Master Reset to Output LOW		7	14	20	
t_{rec} ($\overline{MR}$)	Master Reset Recovery Time			−1	10	ns

DEFINITION OF TERMS

SUBSCRIPT TERMS:

H HIGH, applying to a HIGH logic level or when used with V_{CC} to indicate high V_{CC} value.

I Input.

L LOW, applying to LOW logic level or when used with V_{CC} to indicate low V_{CC} value.

O Output.

FUNCTIONAL TERMS:

D_0, D_1, D_2, D_3 Inputs The four data inputs of each of the 9308 latch blocks.

$\overline{E}_0$, $\overline{E}_1$ Inputs The two Enable inputs. Both of these inputs must be LOW for insertion of data into the latches.

Fan Out The logic HIGH or LOW output drive capability in terms of input unit loads.

Input Unit Load One T^2L gate input load. In the HIGH state it is equal to 40μA at 2.4V and in the LOW state it is equal to 1.6mA at 0.4V.

Latch A storage element which stores one bit of data on receipt of a single transition on an Enable signal.

$\overline{MR}$ Input The master reset input.

Q_0, Q_1, Q_2, Q_3 Outputs The four outputs of each of the 9308 latch blocks.

$Q(t_n)$ The output of a latch at time t_n.

$Q(t_{n+1})$ The output of a latch at time t_{n+1} when input conditions at time t_n have been realized by the output.

OPERATIONAL TERMS:

I_{IL} Forward input load current for unit input load.

I_{OH} Output HIGH current forced out of output in V_{OH} test.

I_{OL} Output LOW current forced into the output in V_{OL} test.

I_{IH} Reverse input load current with V_{OH} applied to input.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

V_{IH} Minimum logic HIGH input voltage. Refer to Figure 6.

V_{IL} Maximum logic LOW input voltage. Refer to Figure 6.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} into output.

SWITCHING TERMS: (All switching times are measured at the 1.5 V logic level.)

t_{pw} ($\overline{E}$) The minimum time that both Enable inputs $\overline{E}_0$ and $\overline{E}$ must be LOW in order for data to be correctly entered into the latches.

t_{pw} ($\overline{MR}$) The minimum pulse width for resetting the latches.

t_{pd+} (DQ) The propagation delay from the D input LOW to HIGH transition to the Q output LOW to HIGH transition. Refer to Figure 1.

t_{pd-} (DQ) The propagation delay from the D input HIGH-LOW transition to the Q output HIGH to LOW transition. Refer to Figure 1.

t_{pd+} ($\overline{E}$Q) The propagation delay from the Enable signal HIGH-LOW transition to the Q output LOW to HIGH transition. Refer to Figure 1.

t_{pd-} ($\overline{E}$Q) The propagation delay from the Enable signal HIGH to LOW transition to the Q output HIGH to LOW transition. Refer to Figure 1.

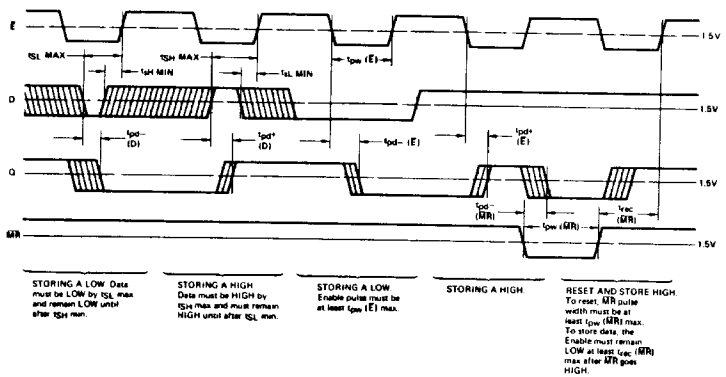
$t_{s\ (H)}$ ($\overline{DE}$) The time required for a HIGH logic level to be present and remain present at a data input prior to the Enable transition from LOW to HIGH in order for the latch to retain a HIGH logic level. Refer to Figure 1. HIGH data must be steady at all times between t_{sH} max and t_h min.

$t_{s\ (L)}$ ($\overline{DE}$) The time required for a LOW logic level to be present and remain present at a data input prior to the Enable transition from LOW to HIGH in order for the latch to retain a LOW logic level. LOW data must be steady at all times between t_{sL} max and t_{sH} min.

t_{rec} ($\overline{MR}$) Recovery time for MR is the minimum time required between the end of the reset pulse and the Enable transition from LOW to HIGH in order for the latches to respond to new data. Refer to Figure 1.

t_{pd-} ($\overline{MR}$) The propagation delay from the master reset signal HIGH-LOW transition to the output HIGH-LOW transition. Refer to Figure 1.

SWITCHING WAVEFORMS



Note: The "set-up Time" is defined as the time required, relative to the enable, for a LOW to HIGH edge (tsH) or a HIGH to LOW edge (tsL) to propagate through internal delays. Logic transitions occurring before ts max are guaranteed to be detected; those occurring after ts min are guaranteed not to be detected. Transitions between ts max and ts min may or may not be detected. The minimum set up time for a LOW is sometimes called the "release time" for a HIGH.

KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN

Figure 1

TRUTH TABLE

Inputs				Output
$\overline{MR}$	$\overline{E}_0$	$\overline{E}_1$	$D_{(n)}$	$Q_{(n+1)}$
L	X	X	X	L
H	L	L	L	L
H	L	L	H	H
H	H	X	X	$Q_{(n)}$ No change
H	X	H	X	$Q_{(n)}$ No change

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Table I

MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

Table II

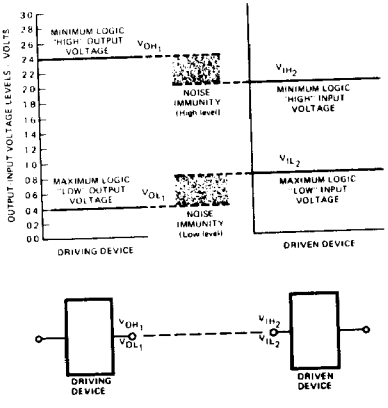
Am9308 LOADING RULES (in unit loads)

Input/Output	Pin No.'s	Input Unit Load	Output Drive HIGH	LOW
Latch 1 $\overline{MR}$	1	1	—	—
$\overline{E}_0$	2	1	—	—
$\overline{E}_1$	3	1	—	—
D_0	4	1.5	—	—
Q_0	5	—	18	9
D_1	6	1.5	—	—
Q_1	7	—	18	9
D_2	8	1.5	—	—
Q_2	9	—	18	9
D_3	10	1.5	—	—
Q_3	11	—	18	9
GND	12	—	—	—
Latch 2 $\overline{MR}$	13	1	—	—
$\overline{E}_0$	14	1	—	—
$\overline{E}_1$	15	1	—	—
D_0	16	1.5	—	—
Q_0	17	—	18	9
D_1	18	1.5	—	—
Q_1	19	—	18	9
D_2	20	1.5	—	—
Q_2	21	—	18	9
D_3	22	1.5	—	—
Q_3	23	—	18	9
V_{CC}	24	—	—	—

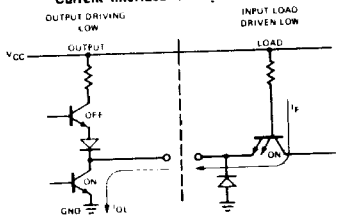
Table III

INPUT/OUTPUT INTERFACE CONDITIONS

Voltage Interface Conditions — LOW & HIGH



Current Interface Conditions — LOW



Current Interface Conditions — HIGH

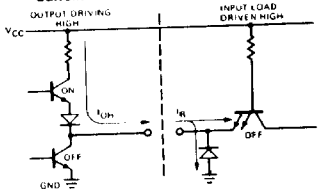


Figure 2

9308 APPLICATIONS

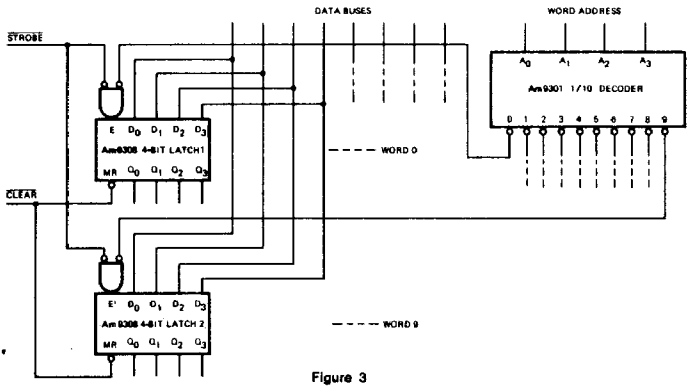


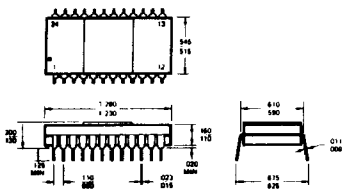
Figure 3

Latch Selection

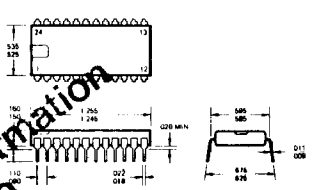
The Am9308 can be selected by using an Am9301 decoder. The active LOW outputs of the Decoder conform with the active LOW input enables of the latch blocks. The diagram shows one 4-bit latch being selected out of ten possible latch blocks.

PHYSICAL DIMENSIONS
Dual-In-Line

Hermetic

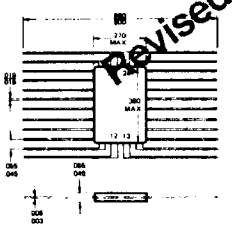


Molded



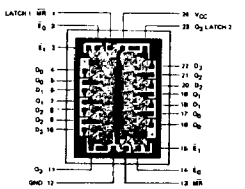
Revised Package Information
See Section 9

Flat Package



Metallization and Pad Layout

73 x 101 Mils



ADVANCED
MICRO
DEVICES INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

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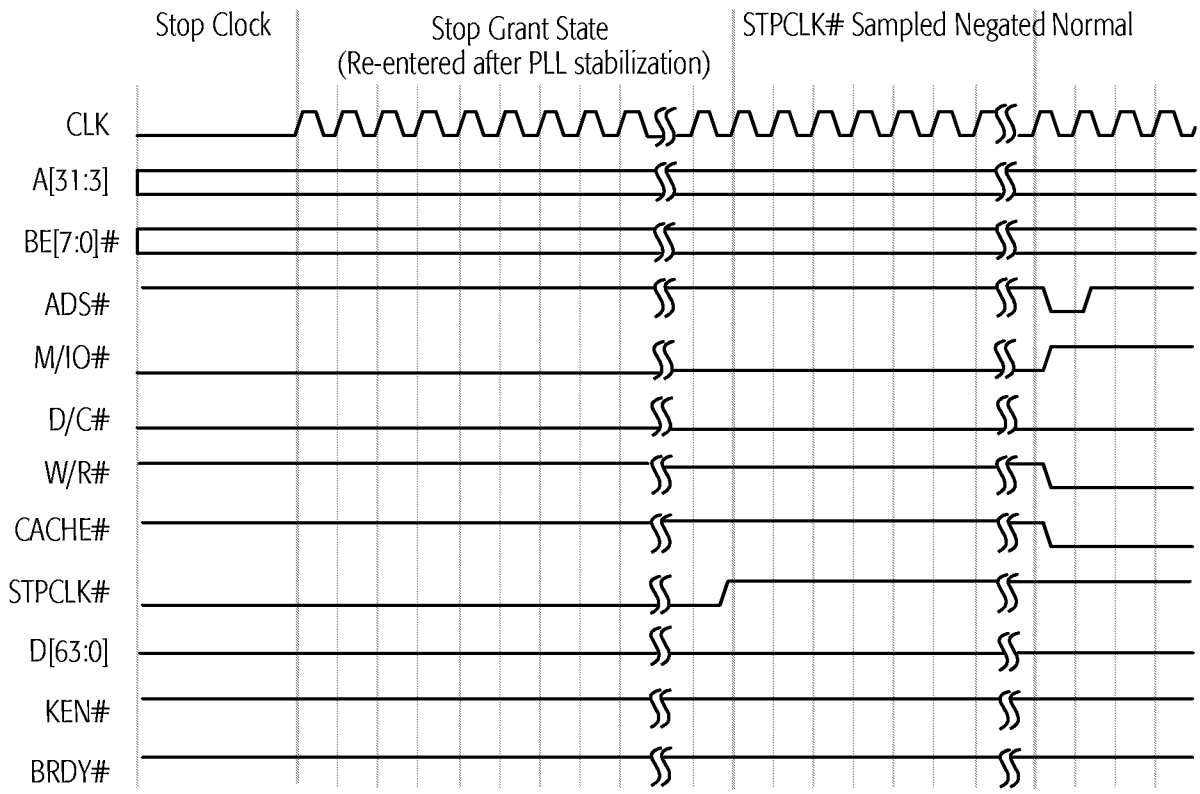

Figure 75. Stop Grant and Stop Clock Modes, Part 2

INIT-Initiated Transition from Protected Mode to Real Mode

INIT is typically asserted in response to a BIOS interrupt that writes to an I/O port. This interrupt is often in response to a Ctrl-Alt-Del keyboard input. The BIOS writes to a port (similar to port 64h in the keyboard controller) that asserts INIT. INIT is also used to support 80286 software that must return to Real mode after accessing extended memory in Protected mode.

The assertion of INIT causes the processor to empty its pipelines, initialize most of its internal state, and branch to address FFFF_FFF0h—the same instruction execution starting point used after RESET. Unlike RESET, the processor preserves the contents of its caches, the floating-point state, the MMX state, Model-Specific Registers (MSRs), the CD and NW bits of the CR0 register, the time stamp counter, and other specific internal resources.

Figure 76 shows an example in which the operating system writes to an I/O port, causing the system logic to assert INIT. The sampling of INIT asserted starts an extended microcode sequence that terminates with a code fetch from FFFF_FFF0h, the reset location. INIT is sampled on every clock edge but is not recognized until the next instruction boundary. During an I/O write cycle, it must be sampled asserted a minimum of three clock edges before BRDY# is sampled asserted if it is to be recognized on the boundary between the I/O write instruction and the following instruction. If INIT is asserted synchronously, it can be asserted for a minimum of one clock. If it is asserted asynchronously, it must have been negated for a minimum of two clocks, followed by an assertion of a minimum of two clocks.

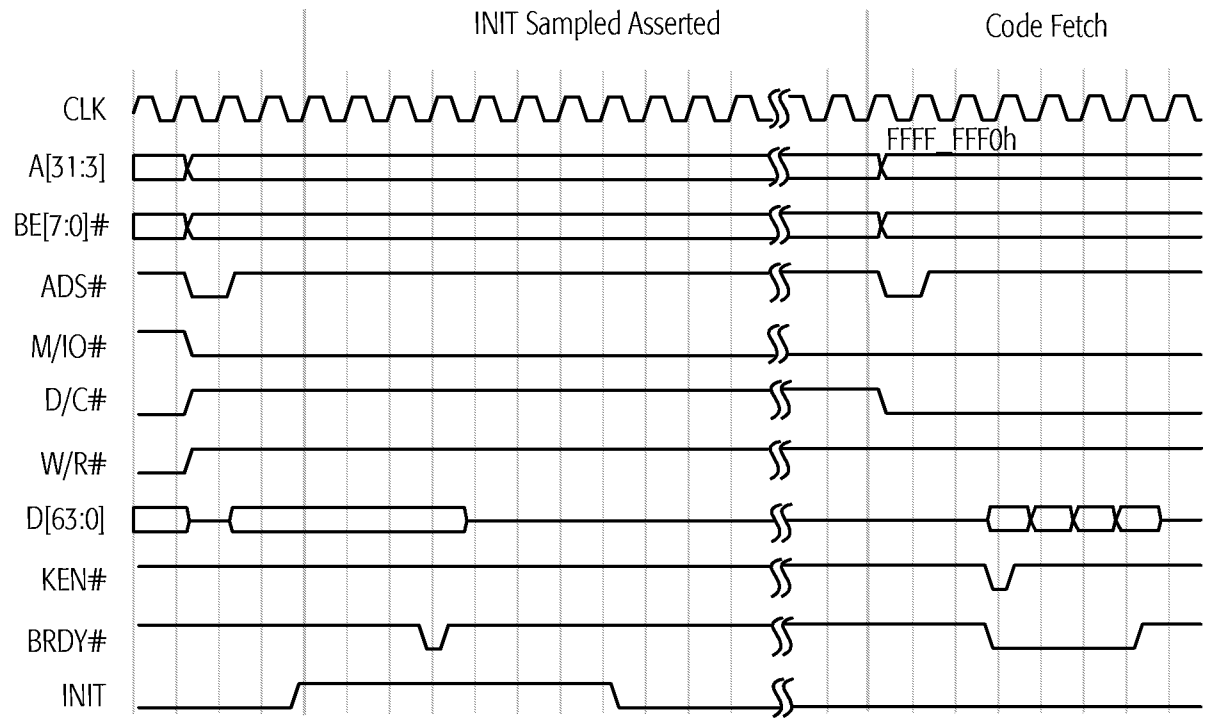

Figure 76. INIT-Initiated Transition from Protected Mode to Real Mode

6 Power-on Configuration and Initialization

On power-on the system logic must reset the AMD-K6-2 processor by asserting the RESET signal. When the processor samples RESET asserted, it immediately flushes and initializes all internal resources and its internal state, including its pipelines and caches, the floating-point state, the MMX and 3DNow! states, and all registers. Then the processor jumps to address FFFF_FFF0h to start instruction execution.

6.1 Signals Sampled During the Falling Transition of RESET

FLUSH# FLUSH# is sampled on the falling transition of RESET to determine if the processor begins normal instruction execution or enters Tri-State Test mode. If FLUSH# is High during the falling transition of RESET, the processor unconditionally runs its Built-In Self Test (BIST), performs the normal reset functions, then jumps to address FFFF_FFF0h to start instruction execution. (See "Built-In Self-Test (BIST)" on page 217 for more details.) If FLUSH# is Low during the falling transition of RESET, the processor enters Tri-State Test mode. (See "Tri-State Test Mode" on page 218 and "FLUSH# (Cache Flush)" on page 103 for more details.)

BF[2:0] The internal operating frequency of the processor is determined by the state of the bus frequency signals BF[2:0] when they are sampled during the falling transition of RESET. The frequency of the CLK input signal is multiplied internally by a ratio defined by BF[2:0]. (See "BF[2:0] (Bus Frequency)" on page 92 for the processor-clock to bus-clock ratios.)

BRDYC# BRDYC# is sampled on the falling transition of RESET to configure the drive strength of A[20:3], ADS#, HITM#, and W/R#. If BRDYC# is Low during the fall of RESET, these outputs are configured using higher drive strengths than the standard strength. If BRDYC# is High during the fall of RESET, the standard strength is selected. (See "BRDYC# (Burst Ready Copy)" on page 95 for more details.)

6.2 RESET Requirements

During the initial power-on reset of the processor, RESET must remain asserted for a minimum of 1.0 ms after CLK and V_{CC} reach specification. (See "CLK Switching Characteristics" on page 255 for clock specifications. See "Electrical Data" on page 247 for V_{CC} specifications.)

During a warm reset while CLK and V_{CC} are within specification, RESET must remain asserted for a minimum of 15 clocks prior to its negation.

6.3 State of Processor After RESET

Output Signals

Table 31 shows the state of all processor outputs and bidirectional signals immediately after RESET is sampled asserted.

Table 31. Output Signal State After RESET

Signal	State	Signal	State
A[31:3], AP	Floating	LOCK#	High
ADS#, ADSC#	High	M/IO#	Low
APCHK#	High	PCD	Low
BE[7:0]#	Floating	PCHK#	High
BREQ	Low	PWT	Low
CACHE#	High	SCYC	Low
D/C#	Low	SMIACT#	High
D[63:0], DP[7:0]	Floating	TDO	Floating
FERR#	High	VCC2DET	Low
HIT#	High	VCC2H/L#	Low
HITM#	High	W/R#	Low
HLDA	Low	–	–

Registers

Table 32 on page 175 shows the state of all architecture registers and Model-Specific Registers (MSRs) after the processor has completed its initialization due to the recognition of the assertion of RESET.