VITESSE

VSC837
Data Sheet

3.2 Gb/s 68x68 Crosspoint Switch

FEATURES

- 68 Input by 68 Output Crosspoint Switch
- 3.2 Gb/s NRZ Data Bandwidth
- 66 MHz Multi-Mode Programming Port
- TTL/2.5 V CMOS Control I/O (3.3V tolerant)
- Programmable On-Chip I/O Termination
- Input Signal Activity (ISA) Monitoring Function
- Integrated Signal Equalization (ISE) for Deterministic Jitter Reduction
- Single 2.5 V Supply
- Differential CML Output Driver
- 11 W typical/14 W maximum (low drive mode) 13 W typical/16W maximum (high drive mode)
- Hard and Soft Power-Down for Unused Channels
- High Performance, 37.5 mm, 480 TBGA Package

GENERAL DESCRIPTION

The VSC837 is a monolithic 68x68 asynchronous crosspoint switch designed to carry broadband data streams. The non-blocking switch core is programmed through a triple-mode port interface that allows random access programming of each input/output port. A high degree of signal integrity is maintained throughout the chip via fully differential signal paths.

The crosspoint function is based on a multiplexer array architecture. Each data output is driven by a 68:1 multiplexer that can be programmed to one and only one of its 68 inputs. The signal path is unregistered and fully asynchronous, so there are no restrictions on the phase, frequency, or signal pattern at each input.

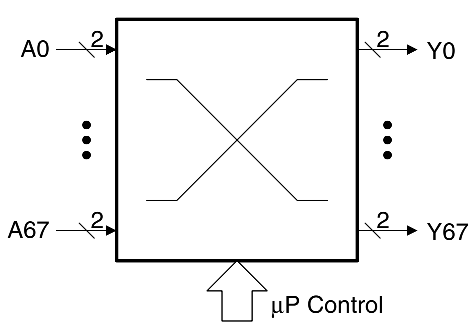
Each high-speed output is a fully differential switched current driver with switchable on-die terminations for maximum signal integrity. Data inputs are terminated on-die through 100 Ω resistors between true and complement inputs (see “Input Termination” on page 9 for further details).

A triple-mode programming interface is provided that allows programming commands to be sent as serial data or one of two forms of parallel data. The input-referred mode (burst mode) allows an input port to be routed to all outputs in only four program cycles. Core programming can be random for each port address, or multiple program assignments can be queued and issued simultaneously. The programming may be initialized to a “straight-through” configuration (A0 to Y0, A1 to Y1, and so on) using the $\overline{\text{INIT}}$ pin.

An activity monitor is provided to allow in-system diagnostics. The activity monitor can observe any high-speed inputs via an internal 69th multiplexer.

Unused channels may be powered down to allow efficient use of the switch in applications that require only a subset of the channels. Power-down can be accomplished in hardware, via dedicated power pins for pairs of input and output channels, or in software by programming individual unused outputs with a disable code.

VSC837 Block Diagram



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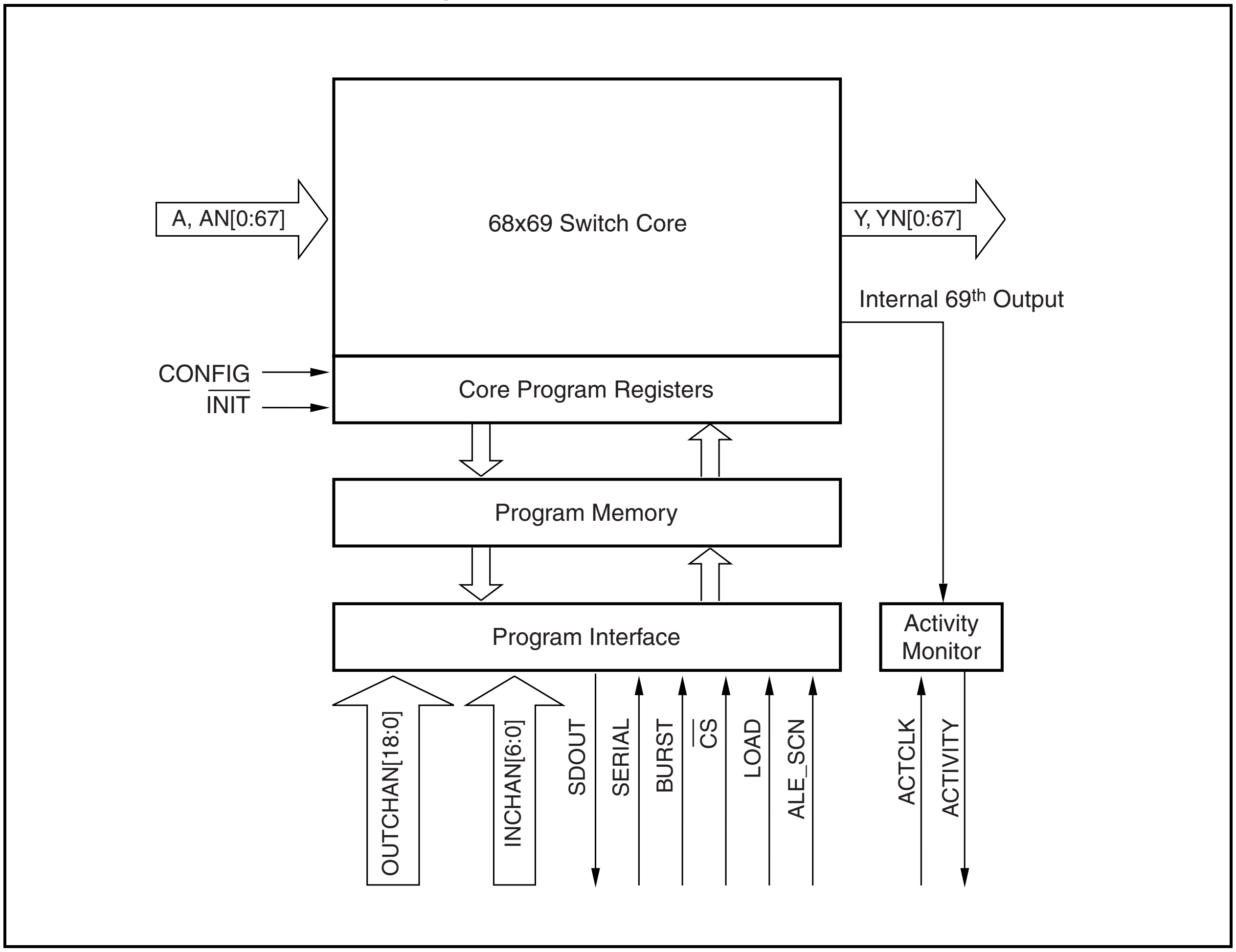
VSC837 Functional Block Diagram



Functional Description

Input/Output Characteristics

All input data must be differential and should be nominally biased to +2.0V or AC-coupled. Other levels are allowed as described under "Input Termination" on page 9. On-chip terminations, with a nominal impedance of 100Ω differential, are provided. All input termination resistors float with an internal bias provided for AC-coupling.

For direct interconnection of multiple VSC837 devices, a CML termination mode is provided by tying the ITC pin to V_{CC}, which ties the center point of the 100Ω termination to V_{CC}, causing the terminations to act as loads for an open-drain or open-collector differential output.

Data outputs are provided through differential current switches with on-chip back-termination. The output circuit is capable of driving external 50Ω far-end termination (recommended). The output back-terminations are electronically switchable to enable a power savings of 2W (max) by reducing the output driver current.

Programming Interface

Parallel Mode

In parallel mode (SERIAL = 0, BURST = 0), the binary word on INCHAN[6:0] is the numerical identifier of the input that will be routed to the specified output. OUTCHAN[6:0] is the numerical identifier of the output being programmed. A rising edge on the LOAD signal will transfer the programming data to the shadow register in the program memory. Raising CONFIG (asynchronously) will transfer the programming data to the main latches in the program memory and cause the internal select signals in the core to reconfigure the multiplexer. Lowering CONFIG will latch the main latches. CONFIG may be tied HIGH to enable programming to take effect instantaneously.

This interface may be used with multiplexed address/data buses by using only INCHAN[6:0] without OUTCHAN[6:0] and dropping ALE when the address of the output to be programmed is present on INCHAN[6:0]. After the address is latched, the input address may be presented on INCHAN[6:0] and programming proceeds as above.

No read-back capability is provided in parallel mode. Read-back for diagnostic purposes is provided in serial mode via the scan function.

Serial Mode

In serial mode (SERIAL = 1, BURST = 0), the INCHAN0 pin becomes the serial data input and the INCHAN1 pin becomes the serial clock (rising edge triggered). A serial word of the form [Output][Input] is shifted into the internal shift register and the LOAD pin is asserted (HIGH), coincident with the last bit of the data word to signal that the word is to be applied. This transfers the input identifier to the shadow register of the addressed output. CONFIG is then applied (asynchronously) to transfer one or more program commands to the main latches of the program memories.

The SDOUT pin follows the data on the INCHAN0_SDIN pin 14 clock cycles later. This enables the user to chain the serial ports of several crosspoints, shift program data for all switches through such a chain, and asserts LOAD on all switches to program all of the connections simultaneously.

The output field is 7 bits long, representing the binary numerical identifier of the output to be programmed. The input field is 7 bits long, representing the numerical identifier of the input that will be routed to the specified output.

Serial Read-Back

Read-back of the program memory contents is accomplished in serial mode by setting the ALE_SCN pin HIGH. This will serially shift out the contents of the main latches in the program memories, slice 68 first and slice 0 last, and MSB-first, LSB-last for each 7-bit word. One rising edge of INCHAN1_SCLK, with ALE_SCN = 0 and SERIAL = 1, must occur to load the entire 483-bit shift register prior to shifting out data. At a clock rate of 66MHz, this operation takes 7.26µs.

Burst Mode

Burst mode programming (BURST = 1, SERIAL = 0) enables an input to be broadcast to any group of 1 to 17 outputs with a single command. In this mode, rising edges on the LOAD pin will trigger program operations. The INCHAN[6:0] pins represent the input to be broadcast. The OUTCHAN[18:17] pins represent the page (quarter) of the program memory to access, and each of the OUTCHAN[16:0] pins represents 1 of the 17 outputs within that page. A '1' on any of those pins will cause that output to be programmed to connect to the input named on INCHAN[6:0].

No read-back capability is provided in burst mode. See “Serial Read-Back” above.

Activity Monitoring

The activity monitor observes the output of the internal 69^{th} output from the core. By programming the 69^{th} output to observe various inputs, the input signals can be scanned for activity or lack thereof. Each rising edge of ACTCLK causes the monitor to read out the activity state from the previous ACTCLK period and clears the internal activity state until a data transition triggers it again. There must be a minimum of one rising and one falling edge on the observed input data pin during the ACTCLK period for activity to be detected. After power-on the output of ACTIVITY after the first ACTCLK rising edge is unknown.

Selective Power-Down

Unused input and output channels can be made to consume little or no power via one of two methods of selective power-down.

Software Power-Down

Using the software power-down feature, unused outputs may be disabled, saving approximately 150mW per output channel for maximum dissipation conditions. This is accomplished by programming each unused output to look at input 63 (3F Hex), which represents a non-existent input channel. The channel may be subsequently activated by programming a valid input address. It is recommended, however, that any changes in power programming only be executed as part of an initialization sequence to guard against the effects of any switching transients that might result from suddenly changing the power supply current. Software mode does not affect the functioning or power of unused input channels.

Hardware Power-Down

Using the hardware power-down feature, the power associated with given input channel pairs may be shut off by tying the corresponding V_{EE} pin to V_{CC} (see Table 11 on page 12). Up to 17 outputs may be powered off in this manner. Approximately 150mW per input channel pairs is saved under the maximum dissipation conditions. The power associated with given output channel pairs, including their contribution to the core power, can be shut off by tying the corresponding V_{EE} pin to V_{CC} (see Table 11 on page 12). Approximately 300mW per two output channels is saved under the maximum dissipation conditions.

Certain V_{EE} pins must always be active. See Figure 7 on page 11 and Table 12 on page 20 for the location of these pins.

SPECIFICATIONS

AC Characteristics

Over Recommended Operating Conditions.

Table 1. Data Path

Symbol	Parameter	Min	Typ	Max	Unit	Condition
f_{RATE}	Maximum data rate			3.2	Gb/s	
t_{SKW}	Channel-to-channel delay skew		300		ps	
t_{PDAY}	Propagation delay from an A input to a Y output		750		ps	
t_R, t_F	High-speed output rise/fall times(1, 2)			150	ps	20% to 80% TERM_CTRL = 1
t_{JR}	Output added delay jitter, rms(1, 2, 3)			10	ps	
t_{JP}	Output added delay jitter, peak-to-peak(1, 2, 3)			40	ps	

1. *Guaranteed, but not tested.*
2. *The high-speed input rise/fall time must be ≤150ps.*
3. *Broadband (unfiltered) deterministic jitter added to a jitter-free input. 2^{23}–1 PRBS data pattern.*

Table 2. Program Interface Timing(1)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{s\overline{WR}}$	Setup time from INCHAN[6:0] or OUTCHAN[6:0] to rising edge of $\overline{WR}$.	3.35			ns
$t_{h\overline{WR}}$	Hold time from rising edge of $\overline{WR}$ to INCHAN[6:0] or OUTCHAN[6:0].	1.45			ns
t_{pwLW}	Pulse width (HIGH or LOW) on LOAD.	15.0			ns
$t_{s\overline{CS}}$	Setup time from $\overline{CS}$ to falling edge of LOAD or ALE_SCN in parallel or burst mode, or rising edge of LOAD in serial mode.	0			ns
$t_{h\overline{CS}}$	Hold time of $\overline{CS}$ rising edge after LOAD or ALE_SCN rising in parallel or burst mode, falling edge of LOAD in serial mode, or falling edge of CONFIG in any mode.	0			ns
t_{pwCFG}	Pulse width (HIGH or LOW) on CONFIG.	6.75			ns
t_{sSDIN}	Setup time from INCHAN0_SDIN to INCHAN1_SCLK rising.	1.65			ns
t_{hSDIN}	Hold time of INCHAN0_SDIN after INCHAN1_SCLK rising.	1.0			ns
$t_{perSCLK}$	Minimum period of SCLK in serial mode.	15			ns
t_{sLOAD}	Setup time from LOAD to INCHAN1_SCLK rising.	1.85			ns
t_{hLOAD}	Hold time of LOAD after INCHAN1_SCLK rising.	0.95			ns
$t_{sSERIAL}$	Setup time from SERIAL rising to INCHAN1_SCLK rising when entering serial mode or SERIAL falling to LOAD falling when entering parallel mode or SERIAL falling to LOAD rising when entering burst mode.	0.90			ns
$t_{hSERIAL}$	Hold time from INCHAN1_SCLK rising to SERIAL falling when exiting serial mode.	0			ns
t_{sBURST}	Setup time from BURST rising to LOAD rising when entering burst mode or BURST falling to LOAD falling when entering parallel mode.	1.85			ns
t_{hBURST}	Hold time from LOAD rising to BURST falling when exiting burst mode.	2.45			ns
t_{dsDOUT}	Delay from INCHAN1_SCLK rising to SDOUT, 20pF load.			6.20	ns
$t_{pw\overline{INIT}}$	Pulse width (HIGH or LOW) on $\overline{INIT}$.	6.75			ns
t_{sSCAN}	Setup time from ALE_SCN to INCHAN1_SCLK rising when starting or completing a serial read-back sequence.	1.65			ns
t_{hSCAN}	Hold time of ALE_SCN after INCHAN1_SCLK rising when starting or completing a serial read-back sequence.	1.0			ns

1. *Program interface timing specifications are guaranteed, but not tested.*

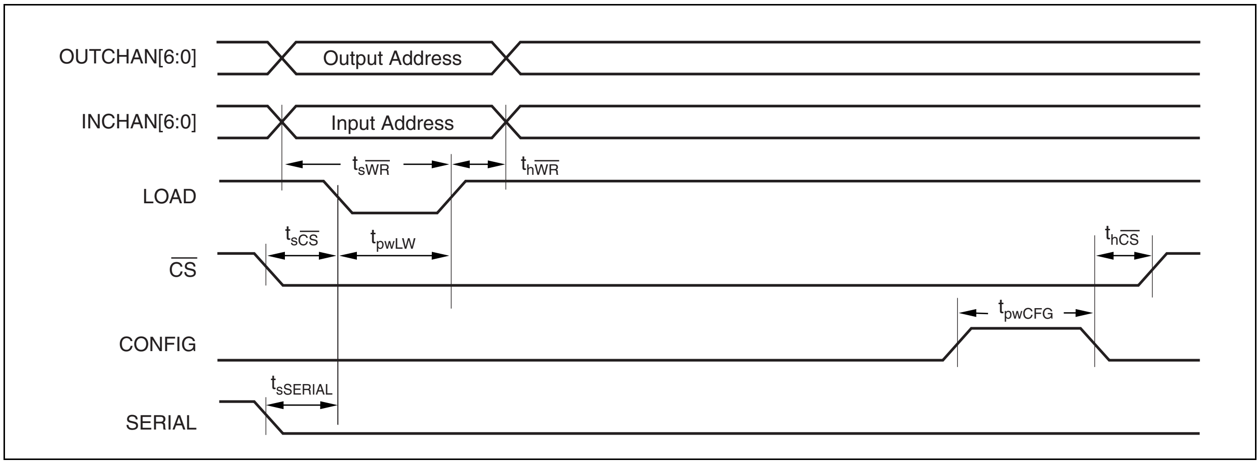


Figure 1. Parallel Mode—Separate Address/Data (leave ALE_SCN pin HIGH)

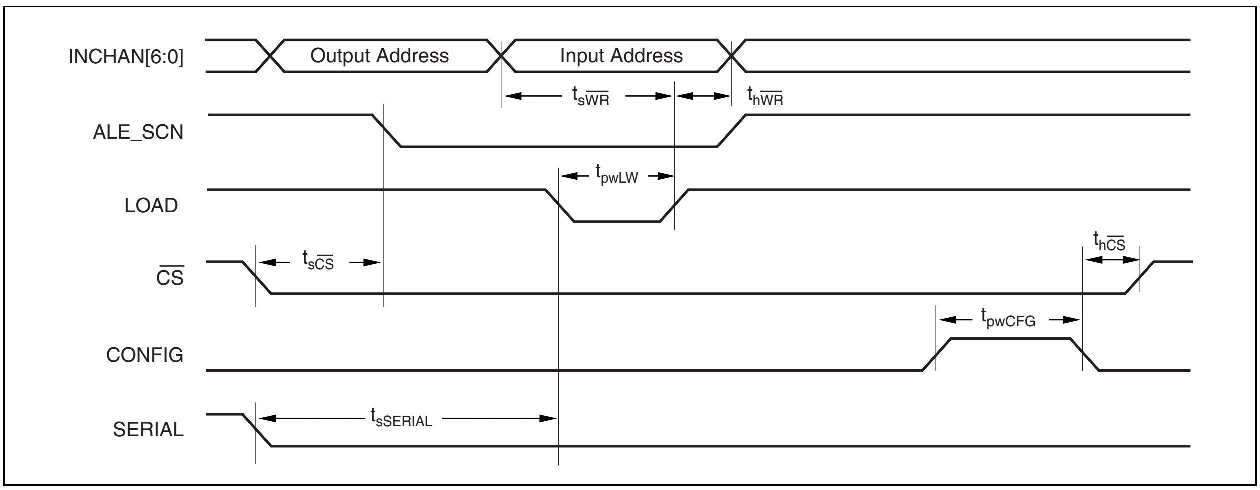


Figure 2. Parallel Mode—Multiplexed Address/Data

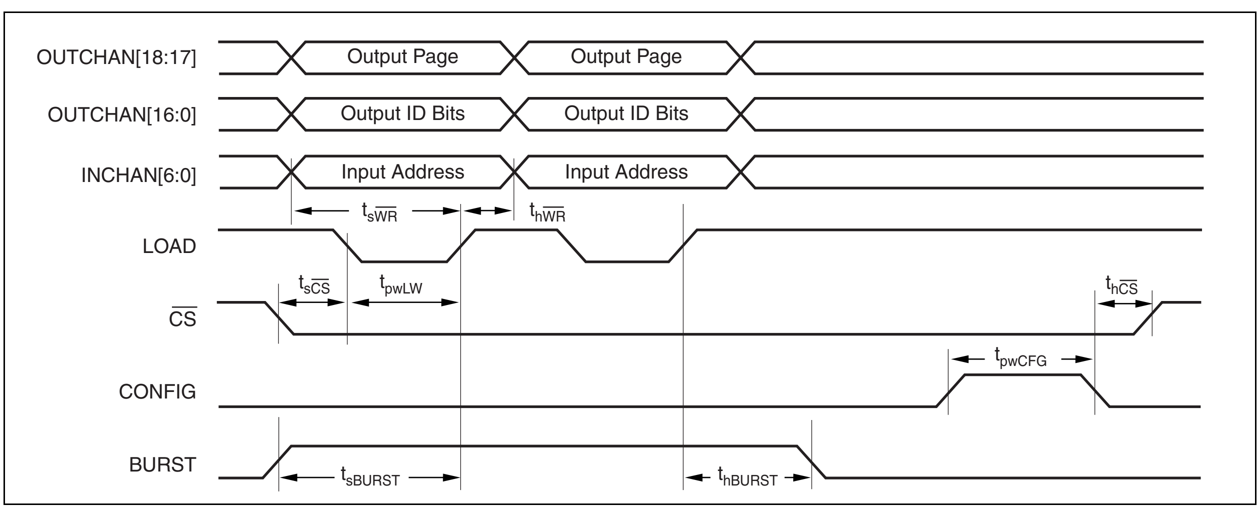


Figure 3. Burst Mode

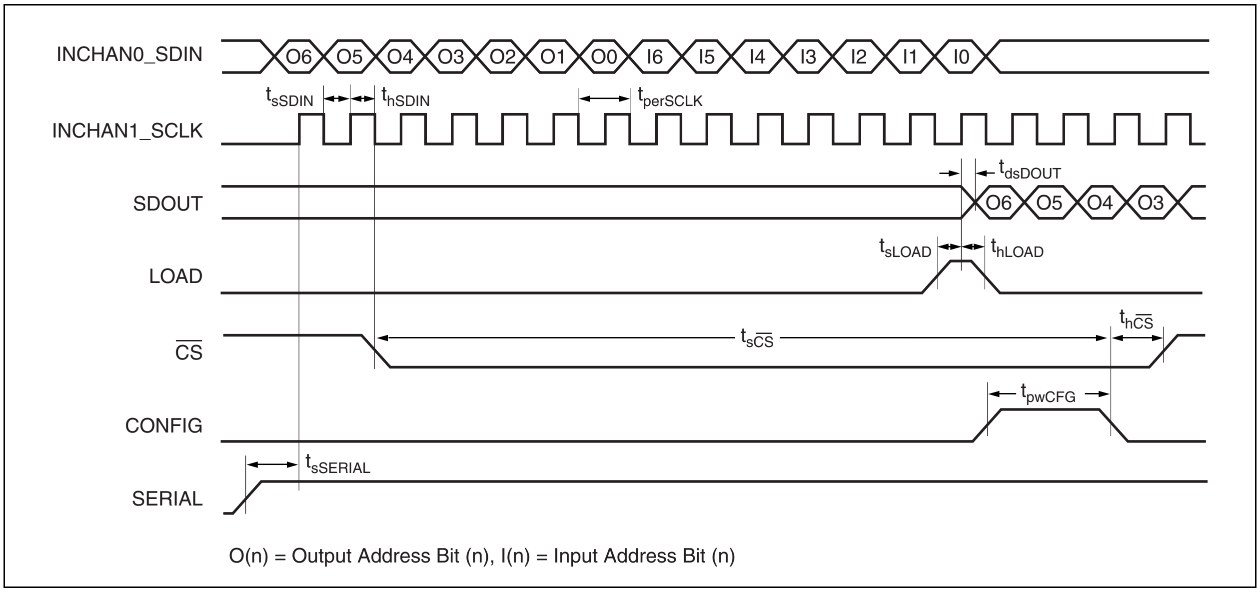


Figure 4. Serial Mode—(leave ALE_SCN pin LOW during programming)

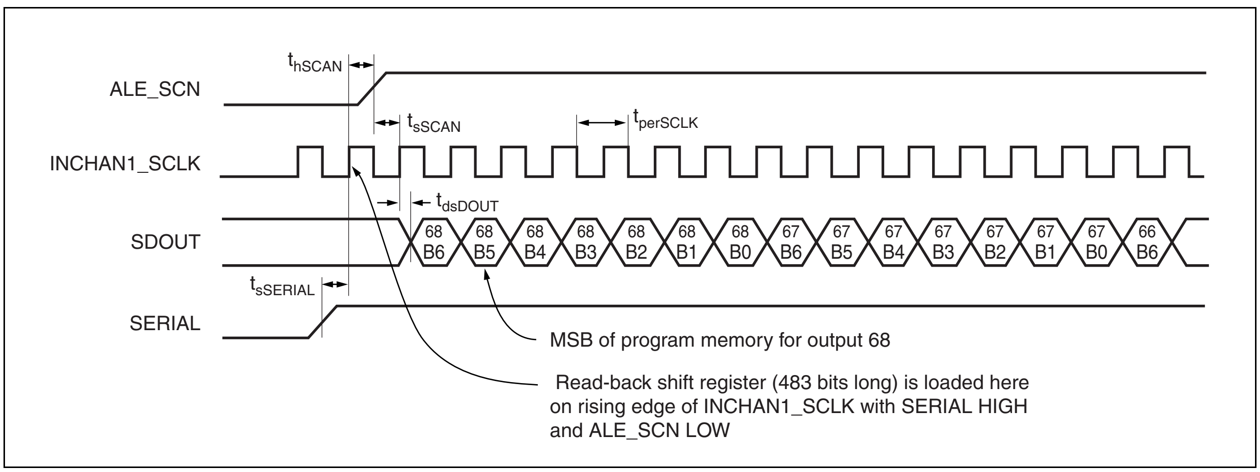


Figure 5. Serial Read-Back

DC Characteristics

Over Recommended Operating Conditions.

Table 3. Power Supply Requirements

Symbol	Parameter	Min	Typ	Max	Unit	Condition
I_{CC}	V_{CC} supply current		5600	6095	mA	
P_T	Total chip power (with I_{TERM} = 0 and back-terminations ON, high drive)		13	16	W	

Table 4. Control Port Input Levels (TTL/CMOS)

Symbol	Parameter	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH voltage	1.7		V_{CC} + 1.0	V	
V_{IL}	Input LOW voltage	0		0.8	V	
$I_{IH\_2.5V}$	Input HIGH current		100		µA	When driven with 2.5V logic.
$I_{IH\_3.3V}$	Input HIGH current		200		µA	When driven with 3.3V logic.
I_{IL}	Input LOW current		100		µA	
V_{OH}	Output HIGH voltage	V_{CC} – 0.2		V_{CC}	V	DC load <500µA
V_{OL}	Output LOW voltage	0		0.2	V	DC load <2mA
V_{OHPU}	V_{OH} with external pull-up(1)	2.4			V	250Ω to 3.3V (5%)
V_{OLPU}	V_{OL} with external pull-up(1)			0.4	V	250Ω to 3.3V (5%)

1. *Guaranteed, but not tested.*

Table 5. Signal Input levels (high-speed signal path)

Symbol	Parameter	Min	Typ	Max	Unit	Condition
V_{IN}	Input voltage amplitude(1)	150		1100	mV	
V_{ICM}	Input common-mode voltage(2)	V_{CC} – 0.7		V_{CC} – 0.2	V	

1. *Mean peak-to-peak amplitude measurement of either true or complement of the differential signal.*
2. *$V_{CC} = V_{CCP} = 2.5V$, $V_{EE} = 0V$.*

Table 6. Signal Output Levels (high-speed signal path) TERM_CTRL = ON, DRIVE_CTRL = HI

Symbol	Parameter	Min	Typ	Max	Unit	Condition
V_{OUT}	Output differential voltage(1, 3)	400		600	mV	
V_{OCM}	Output common-mode voltage(2, 3)	V_{CC} - 0.3		V_{CC} - 0.2	V	

1. *Mean peak-to-peak amplitude measurement of either true or complement of the differential signal.*
2. *$V_{CC} = V_{CCP} = 2.5V$, $V_{EE} = 0V$.*
3. *Terminated in 50Ω to V_{CC}. This termination is used for testing the part, but other terminations are allowed—see* *Table 8 on page 9.*

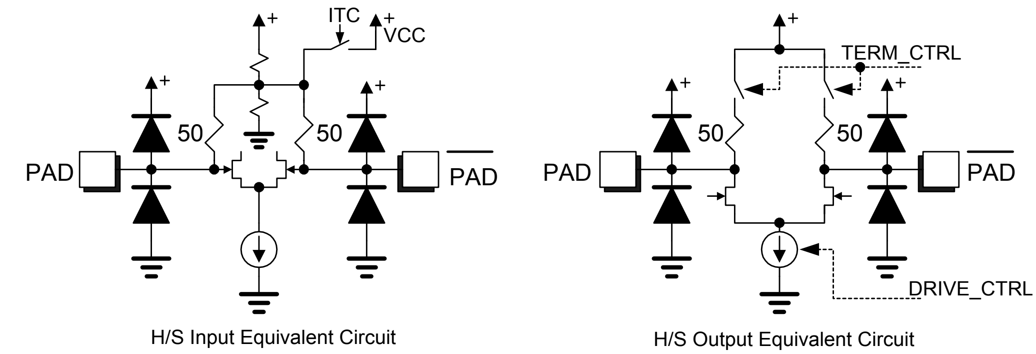


Figure 6. Equivalent Circuits

Input Termination

The high-speed inputs of the VSC837 are internally terminated by a 100Ω resistor between true and complement inputs. Termination resistors are isolated from each other on-chip. The termination will self-bias to +2.0V (nominal) for AC-coupled applications. The ITC pin enables direct interconnection of multiple VSC837 devices. With ITC tied to V_{CC}, the center point of the 100Ω termination resistor is tied to V_{CC}, causing the terminations to act as loads for an open-drain or open-collector differential output.

Table 7. Allowed Input Termination Schemes

Type	Description	Comments
1	AC-coupled input	Tie ITC LOW, 100Ω differential input termination, input self-biased
2	DC-coupled from open-drain CML	Tie ITC HIGH, termination acts as 50Ω load to V_{CC}
3	DC-coupled from back-terminated 2.5V CML	Tie ITC HIGH, termination acts as 50Ω load to V_{CC}
4	DC-coupled from back-terminated 2.5V CML	Tie ITC LOW, 100Ω differential termination (preferred over Type 3)
5	DC-coupled from back-terminated 3.3V LVPECL	Tie ITC LOW, 100Ω differential termination

Output Termination

The high-speed outputs of the VSC837 are internally back-terminated by 50Ω to V_{CC} when the TERM_CTRL pin is HIGH. When this pin is LOW, the output driver functions as an open-drain CML driver. Setting DRIVE_CTRL LOW (GND) saves approximately 2W under maximum power dissipation conditions. See Table 8 for allowable types of terminations and modes of operation.

Table 8. Allowed High-Speed Output Terminations and Modes of Operation

Type	Description	DRIVE_CTRL	TERM_CTRL	V_{OD}(1) (mV) typ	V_{OCM}(1) (V) typ
1	AC-coupled to 50Ω termination to any voltage	V_{CC} (HIGH)	V_{CC} (ON)	500	2.0
2	AC-coupled to 100Ω differential termination	V_{CC} (HIGH)	V_{CC} (ON)	500	2.0
3	DC-coupled, terminated in 50Ω to V_{CC} at far-end only	GND (LOW)	GND (OFF)	500	2.25
4	DC-coupled, terminated in 50Ω to V_{CC} at far-end only	V_{CC} (HIGH)	GND (OFF)	1000	2.0
5	DC-coupled, source and far-end terminated in 50Ω to V_{CC}	GND (LOW)	V_{CC} (ON)	250	2.375
6	DC-coupled, source and far-end terminated in 50Ω to V_{CC}	V_{CC} (HIGH)	V_{CC} (ON)	500	2.25
7	DC-coupled, 100Ω differential termination	GND (LOW)	V_{CC} (ON)	250	2.25
8	DC-coupled, 100Ω differential termination	V_{CC} (HIGH)	V_{CC} (ON)	500	2.0

1. Measured at output of VSC837, with V_{CC} = 2.5V.

Table 9. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Condition
V_{EE}	Power supply voltage		0		V	
V_{CC}, V_{CCP}	Power supply voltage	+2.375	+2.5	+2.625	V	
T	Operating temperature range(1)	0		+85	°C	

1. *Lower limit of specification is ambient temperature and upper limit is case temperature.*

Table 10. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{CC}	Power supply voltage, potential to ground	–0.5	+4.0	V
	Input voltage applied (TTL)	–0.5	V_{CC} +1.0	V
	Input voltage applied (ECL)	–0.5	V_{CC} +0.5	V
I_{OUT}	Output current	–50	+50	mA
T_C	Case temperature under bias	–55	+125	°C
T_S	Storage temperature	–65	+150	°C
V_{ESD}	ESD (Human Body Model)	–500	+500	V

Stresses listed under Absolute Maximum Ratings may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE

This device can be damaged by ESD. Vitesse recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

PACKAGE INFORMATION

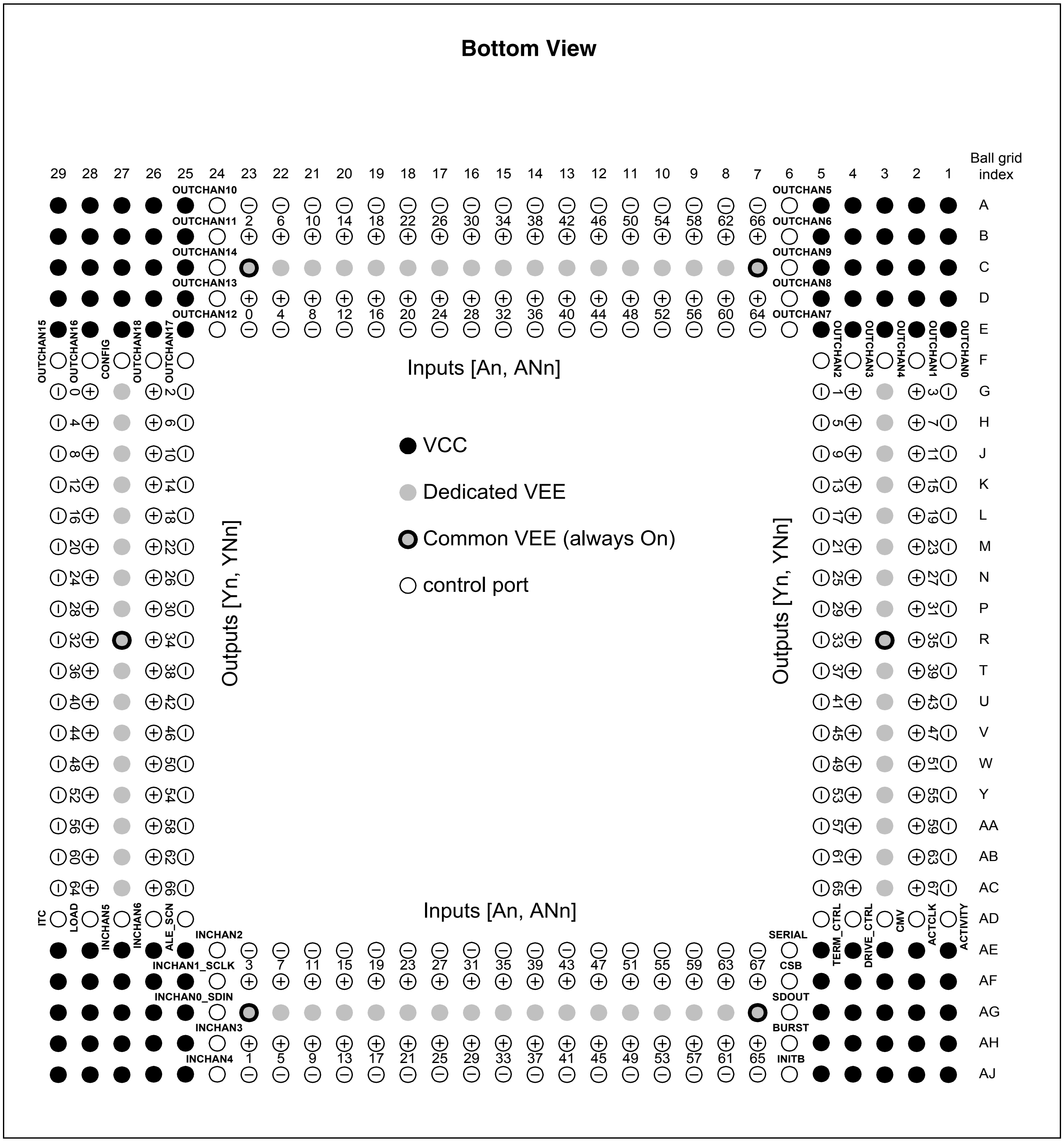


Figure 7. Pin Diagram for 480-Pin TBGA (UG)

Table 11. Pin Identification for 480-Pin TBGA (UG)

Signal	Ball Site	I/O	Level	Description
High-Speed Data Inputs				
A0	D23	I	PECL	High-Speed Data Input Channel 0, True.
A1	AH23	I	PECL	High-Speed Data Input Channel 1, True.
A2	B23	I	PECL	High-Speed Data Input Channel 2, True.
A3	AF23	I	PECL	High-Speed Data Input Channel 3, True.
A4	D22	I	PECL	High-Speed Data Input Channel 4, True.
A5	AH22	I	PECL	High-Speed Data Input Channel 5, True.
A6	B22	I	PECL	High-Speed Data Input Channel 6, True.
A7	AF22	I	PECL	High-Speed Data Input Channel 7, True.
A8	D21	I	PECL	High-Speed Data Input Channel 8, True.
A9	AH21	I	PECL	High-Speed Data Input Channel 9, True.
A10	B21	I	PECL	High-Speed Data Input Channel 10, True.
A11	AF21	I	PECL	High-Speed Data Input Channel 11, True.
A12	D20	I	PECL	High-Speed Data Input Channel 12, True.
A13	AH20	I	PECL	High-Speed Data Input Channel 13, True.
A14	B20	I	PECL	High-Speed Data Input Channel 14, True.
A15	AF20	I	PECL	High-Speed Data Input Channel 15, True.
A16	D19	I	PECL	High-Speed Data Input Channel 16, True.
A17	AH19	I	PECL	High-Speed Data Input Channel 17, True.
A18	B19	I	PECL	High-Speed Data Input Channel 18, True.
A19	AF19	I	PECL	High-Speed Data Input Channel 19, True.
A20	D18	I	PECL	High-Speed Data Input Channel 20, True.
A21	AH18	I	PECL	High-Speed Data Input Channel 21, True.
A22	B18	I	PECL	High-Speed Data Input Channel 22, True.
A23	AF18	I	PECL	High-Speed Data Input Channel 23, True.
A24	D17	I	PECL	High-Speed Data Input Channel 24, True.
A25	AH17	I	PECL	High-Speed Data Input Channel 25, True.
A26	B17	I	PECL	High-Speed Data Input Channel 26, True.
A27	AF17	I	PECL	High-Speed Data Input Channel 27, True.
A28	D16	I	PECL	High-Speed Data Input Channel 28, True.
A29	AH16	I	PECL	High-Speed Data Input Channel 29, True.
A30	B16	I	PECL	High-Speed Data Input Channel 30, True.
A31	AF16	I	PECL	High-Speed Data Input Channel 31, True.
A32	D15	I	PECL	High-Speed Data Input Channel 32, True.
A33	AH15	I	PECL	High-Speed Data Input Channel 33, True.
A34	B15	I	PECL	High-Speed Data Input Channel 34, True.
A35	AF15	I	PECL	High-Speed Data Input Channel 35, True.
A36	D14	I	PECL	High-Speed Data Input Channel 36, True.
A37	AH14	I	PECL	High-Speed Data Input Channel 37, True.
A38	B14	I	PECL	High-Speed Data Input Channel 38, True.
A39	AF14	I	PECL	High-Speed Data Input Channel 39, True.
A40	D13	I	PECL	High-Speed Data Input Channel 40, True.

Table 11. Pin Identification for 480-Pin TBGA (UG) (continued)

Signal	Ball Site	I/O	Level	Description
A41	AH13	I	PECL	High-Speed Data Input Channel 41, True.
A42	B13	I	PECL	High-Speed Data Input Channel 42, True.
A43	AF13	I	PECL	High-Speed Data Input Channel 43, True.
A44	D12	I	PECL	High-Speed Data Input Channel 44, True.
A45	AH12	I	PECL	High-Speed Data Input Channel 45, True.
A46	B12	I	PECL	High-Speed Data Input Channel 46, True.
A47	AF12	I	PECL	High-Speed Data Input Channel 47, True.
A48	D11	I	PECL	High-Speed Data Input Channel 48, True.
A49	AH11	I	PECL	High-Speed Data Input Channel 49, True.
A50	B11	I	PECL	High-Speed Data Input Channel 50, True.
A51	AF11	I	PECL	High-Speed Data Input Channel 51, True.
A52	D10	I	PECL	High-Speed Data Input Channel 52, True.
A53	AH10	I	PECL	High-Speed Data Input Channel 53, True.
A54	B10	I	PECL	High-Speed Data Input Channel 54, True.
A55	AF10	I	PECL	High-Speed Data Input Channel 55, True.
A56	D9	I	PECL	High-Speed Data Input Channel 56, True.
A57	AH9	I	PECL	High-Speed Data Input Channel 57, True.
A58	B9	I	PECL	High-Speed Data Input Channel 58, True.
A59	AF9	I	PECL	High-Speed Data Input Channel 59, True.
A60	D8	I	PECL	High-Speed Data Input Channel 60, True.
A61	AH8	I	PECL	High-Speed Data Input Channel 61, True.
A62	B8	I	PECL	High-Speed Data Input Channel 62, True.
A63	AF8	I	PECL	High-Speed Data Input Channel 63, True.
A64	D7	I	PECL	High-Speed Data Input Channel 64, True.
A65	AH7	I	PECL	High-Speed Data Input Channel 65, True.
A66	B7	I	PECL	High-Speed Data Input Channel 66, True.
A67	AF7	I	PECL	High-Speed Data Input Channel 67, True.
AN0	E23	I	PECL	High-Speed Data Input Channel 0, Complement.
AN1	AJ23	I	PECL	High-Speed Data Input Channel 1, Complement.
AN2	A23	I	PECL	High-Speed Data Input Channel 2, Complement.
AN3	AE23	I	PECL	High-Speed Data Input Channel 3, Complement.
AN4	E22	I	PECL	High-Speed Data Input Channel 4, Complement.
AN5	AJ22	I	PECL	High-Speed Data Input Channel 5, Complement.
AN6	A22	I	PECL	High-Speed Data Input Channel 6, Complement.
AN7	AE22	I	PECL	High-Speed Data Input Channel 7, Complement.
AN8	E21	I	PECL	High-Speed Data Input Channel 8, Complement.
AN9	AJ21	I	PECL	High-Speed Data Input Channel 9, Complement.
AN10	A21	I	PECL	High-Speed Data Input Channel 10, Complement.
AN11	AE21	I	PECL	High-Speed Data Input Channel 11, Complement.
AN12	E20	I	PECL	High-Speed Data Input Channel 12, Complement.
AN13	AJ20	I	PECL	High-Speed Data Input Channel 13, Complement.
AN14	A20	I	PECL	High-Speed Data Input Channel 14, Complement.

Table 11. Pin Identification for 480-Pin TBGA (UG) (continued)

Signal	Ball Site	I/O	Level	Description
AN15	AE20	I	PECL	High-Speed Data Input Channel 15, Complement.
AN16	E19	I	PECL	High-Speed Data Input Channel 16, Complement.
AN17	AJ19	I	PECL	High-Speed Data Input Channel 17, Complement.
AN18	A19	I	PECL	High-Speed Data Input Channel 18, Complement.
AN19	AE19	I	PECL	High-Speed Data Input Channel 19, Complement.
AN20	E18	I	PECL	High-Speed Data Input Channel 20, Complement.
AN21	AJ18	I	PECL	High-Speed Data Input Channel 21, Complement.
AN22	A18	I	PECL	High-Speed Data Input Channel 22, Complement.
AN23	AE18	I	PECL	High-Speed Data Input Channel 23, Complement.
AN24	E17	I	PECL	High-Speed Data Input Channel 24, Complement.
AN25	AJ17	I	PECL	High-Speed Data Input Channel 25, Complement.
AN26	A17	I	PECL	High-Speed Data Input Channel 26, Complement.
AN27	AE17	I	PECL	High-Speed Data Input Channel 27, Complement.
AN28	E16	I	PECL	High-Speed Data Input Channel 28, Complement.
AN29	AJ16	I	PECL	High-Speed Data Input Channel 29, Complement.
AN30	A16	I	PECL	High-Speed Data Input Channel 30, Complement.
AN31	AE16	I	PECL	High-Speed Data Input Channel 31, Complement.
AN32	E15	I	PECL	High-Speed Data Input Channel 32, Complement.
AN33	AJ15	I	PECL	High-Speed Data Input Channel 33, Complement.
AN34	A15	I	PECL	High-Speed Data Input Channel 34, Complement.
AN35	AE15	I	PECL	High-Speed Data Input Channel 35, Complement.
AN36	E14	I	PECL	High-Speed Data Input Channel 36, Complement.
AN37	AJ14	I	PECL	High-Speed Data Input Channel 37, Complement.
AN38	A14	I	PECL	High-Speed Data Input Channel 38, Complement.
AN39	AE14	I	PECL	High-Speed Data Input Channel 39, Complement.
AN40	E13	I	PECL	High-Speed Data Input Channel 40, Complement.
AN41	AJ13	I	PECL	High-Speed Data Input Channel 41, Complement.
AN42	A13	I	PECL	High-Speed Data Input Channel 42, Complement.
AN43	AE13	I	PECL	High-Speed Data Input Channel 43, Complement.
AN44	E12	I	PECL	High-Speed Data Input Channel 44, Complement.
AN45	AJ12	I	PECL	High-Speed Data Input Channel 45, Complement.
AN46	A12	I	PECL	High-Speed Data Input Channel 46, Complement.
AN47	AE12	I	PECL	High-Speed Data Input Channel 47, Complement.
AN48	E11	I	PECL	High-Speed Data Input Channel 48, Complement.
AN49	AJ11	I	PECL	High-Speed Data Input Channel 49, Complement.
AN50	A11	I	PECL	High-Speed Data Input Channel 50, Complement.
AN51	AE11	I	PECL	High-Speed Data Input Channel 51, Complement.
AN52	E10	I	PECL	High-Speed Data Input Channel 52, Complement.
AN53	AJ10	I	PECL	High-Speed Data Input Channel 53, Complement.
AN54	A10	I	PECL	High-Speed Data Input Channel 54, Complement.
AN55	AE10	I	PECL	High-Speed Data Input Channel 55, Complement.
AN56	E9	I	PECL	High-Speed Data Input Channel 56, Complement.

Table 11. Pin Identification for 480-Pin TBGA (UG) (continued)

Signal	Ball Site	I/O	Level	Description
AN57	AJ9	I	PECL	High-Speed Data Input Channel 57, Complement.
AN58	A9	I	PECL	High-Speed Data Input Channel 58, Complement.
AN59	AE9	I	PECL	High-Speed Data Input Channel 59, Complement.
AN60	E8	I	PECL	High-Speed Data Input Channel 60, Complement.
AN61	AJ8	I	PECL	High-Speed Data Input Channel 61, Complement.
AN62	A8	I	PECL	High-Speed Data Input Channel 62, Complement.
AN63	AE8	I	PECL	High-Speed Data Input Channel 63, Complement.
AN64	E7	I	PECL	High-Speed Data Input Channel 64, Complement.
AN65	AJ7	I	PECL	High-Speed Data Input Channel 65, Complement.
AN66	A7	I	PECL	High-Speed Data Input Channel 66, Complement.
AN67	AE7	I	PECL	High-Speed Data Input Channel 67, Complement.
High-Speed Data Outputs				
Y0	G28	O	CML	High-Speed Data Output Channel 0, True.
Y1	G4	O	CML	High-Speed Data Output Channel 1, True.
Y2	G26	O	CML	High-Speed Data Output Channel 2, True.
Y3	G2	O	CML	High-Speed Data Output Channel 3, True.
Y4	H28	O	CML	High-Speed Data Output Channel 4, True.
Y5	H4	O	CML	High-Speed Data Output Channel 5, True.
Y6	H26	O	CML	High-Speed Data Output Channel 6, True.
Y7	H2	O	CML	High-Speed Data Output Channel 7, True.
Y8	J28	O	CML	High-Speed Data Output Channel 8, True.
Y9	J4	O	CML	High-Speed Data Output Channel 9, True.
Y10	J26	O	CML	High-Speed Data Output Channel 10, True.
Y11	J2	O	CML	High-Speed Data Output Channel 11, True.
Y12	K28	O	CML	High-Speed Data Output Channel 12, True.
Y13	K4	O	CML	High-Speed Data Output Channel 13, True.
Y14	K26	O	CML	High-Speed Data Output Channel 14, True.
Y15	K2	O	CML	High-Speed Data Output Channel 15, True.
Y16	L28	O	CML	High-Speed Data Output Channel 16, True.
Y17	L4	O	CML	High-Speed Data Output Channel 17, True.
Y18	L26	O	CML	High-Speed Data Output Channel 18, True.
Y19	L2	O	CML	High-Speed Data Output Channel 19, True.
Y20	M28	O	CML	High-Speed Data Output Channel 20, True.
Y21	M4	O	CML	High-Speed Data Output Channel 21, True.
Y22	M26	O	CML	High-Speed Data Output Channel 22, True.
Y23	M2	O	CML	High-Speed Data Output Channel 23, True.
Y24	N28	O	CML	High-Speed Data Output Channel 24, True.
Y25	N4	O	CML	High-Speed Data Output Channel 25, True.
Y26	N26	O	CML	High-Speed Data Output Channel 26, True.
Y27	N2	O	CML	High-Speed Data Output Channel 27, True.
Y28	P28	O	CML	High-Speed Data Output Channel 28, True.

Table 11. Pin Identification for 480-Pin TBGA (UG) (continued)

Signal	Ball Site	I/O	Level	Description
Y29	P4	O	CML	High-Speed Data Output Channel 29, True.
Y30	P26	O	CML	High-Speed Data Output Channel 30, True.
Y31	P2	O	CML	High-Speed Data Output Channel 31, True.
Y32	R28	O	CML	High-Speed Data Output Channel 32, True.
Y33	R4	O	CML	High-Speed Data Output Channel 33, True.
Y34	R26	O	CML	High-Speed Data Output Channel 34, True.
Y35	R2	O	CML	High-Speed Data Output Channel 35, True.
Y36	T28	O	CML	High-Speed Data Output Channel 36, True.
Y37	T4	O	CML	High-Speed Data Output Channel 37, True.
Y38	T26	O	CML	High-Speed Data Output Channel 38, True.
Y39	T2	O	CML	High-Speed Data Output Channel 39, True.
Y40	U28	O	CML	High-Speed Data Output Channel 40, True.
Y41	U4	O	CML	High-Speed Data Output Channel 41, True.
Y42	U26	O	CML	High-Speed Data Output Channel 42, True.
Y43	U2	O	CML	High-Speed Data Output Channel 43, True.
Y44	V28	O	CML	High-Speed Data Output Channel 44, True.
Y45	V4	O	CML	High-Speed Data Output Channel 45, True.
Y46	V26	O	CML	High-Speed Data Output Channel 46, True.
Y47	V2	O	CML	High-Speed Data Output Channel 47, True.
Y48	W28	O	CML	High-Speed Data Output Channel 48, True.
Y49	W4	O	CML	High-Speed Data Output Channel 49, True.
Y50	W26	O	CML	High-Speed Data Output Channel 50, True.
Y51	W2	O	CML	High-Speed Data Output Channel 51, True.
Y52	Y28	O	CML	High-Speed Data Output Channel 52, True.
Y53	Y4	O	CML	High-Speed Data Output Channel 53, True.
Y54	Y26	O	CML	High-Speed Data Output Channel 54, True.
Y55	Y2	O	CML	High-Speed Data Output Channel 55, True.
Y56	AA28	O	CML	High-Speed Data Output Channel 56, True.
Y57	AA4	O	CML	High-Speed Data Output Channel 57, True.
Y58	AA26	O	CML	High-Speed Data Output Channel 58, True.
Y59	AA2	O	CML	High-Speed Data Output Channel 59, True.
Y60	AB28	O	CML	High-Speed Data Output Channel 60, True.
Y61	AB4	O	CML	High-Speed Data Output Channel 61, True.
Y62	AB26	O	CML	High-Speed Data Output Channel 62, True.
Y63	AB2	O	CML	High-Speed Data Output Channel 63, True.
Y64	AC28	O	CML	High-Speed Data Output Channel 64, True.
Y65	AC4	O	CML	High-Speed Data Output Channel 65, True.
Y66	AC26	O	CML	High-Speed Data Output Channel 66, True.
Y67	AC2	O	CML	High-Speed Data Output Channel 67, True.
YN0	G29	O	CML	High-Speed Data Output Channel 0, Complement.
YN1	G5	O	CML	High-Speed Data Output Channel 1, Complement.
YN2	G25	O	CML	High-Speed Data Output Channel 2, Complement.

Table 11. Pin Identification for 480-Pin TBGA (UG) (continued)

Signal	Ball Site	I/O	Level	Description
YN3	G1	O	CML	High-Speed Data Output Channel 3, Complement.
YN4	H29	O	CML	High-Speed Data Output Channel 4, Complement.
YN5	H5	O	CML	High-Speed Data Output Channel 5, Complement.
YN6	H25	O	CML	High-Speed Data Output Channel 6, Complement.
YN7	H1	O	CML	High-Speed Data Output Channel 7, Complement.
YN8	J29	O	CML	High-Speed Data Output Channel 8, Complement.
YN9	J5	O	CML	High-Speed Data Output Channel 9, Complement.
YN10	J25	O	CML	High-Speed Data Output Channel 10, Complement.
YN11	J1	O	CML	High-Speed Data Output Channel 11, Complement.
YN12	K29	O	CML	High-Speed Data Output Channel 12, Complement.
YN13	K5	O	CML	High-Speed Data Output Channel 13, Complement.
YN14	K25	O	CML	High-Speed Data Output Channel 14, Complement.
YN15	K1	O	CML	High-Speed Data Output Channel 15, Complement.
YN16	L29	O	CML	High-Speed Data Output Channel 16, Complement.
YN17	L5	O	CML	High-Speed Data Output Channel 17, Complement.
YN18	L25	O	CML	High-Speed Data Output Channel 18, Complement.
YN19	L1	O	CML	High-Speed Data Output Channel 19, Complement.
YN20	M29	O	CML	High-Speed Data Output Channel 20, Complement.
YN21	M5	O	CML	High-Speed Data Output Channel 21, Complement.
YN22	M25	O	CML	High-Speed Data Output Channel 22, Complement.
YN23	M1	O	CML	High-Speed Data Output Channel 23, Complement.
YN24	N29	O	CML	High-Speed Data Output Channel 24, Complement.
YN25	N5	O	CML	High-Speed Data Output Channel 25, Complement.
YN26	N25	O	CML	High-Speed Data Output Channel 26, Complement.
YN27	N1	O	CML	High-Speed Data Output Channel 27, Complement.
YN28	P29	O	CML	High-Speed Data Output Channel 28, Complement.
YN29	P5	O	CML	High-Speed Data Output Channel 29, Complement.
YN30	P25	O	CML	High-Speed Data Output Channel 30, Complement.
YN31	P1	O	CML	High-Speed Data Output Channel 31, Complement.
YN32	R29	O	CML	High-Speed Data Output Channel 32, Complement.
YN33	R5	O	CML	High-Speed Data Output Channel 33, Complement.
YN34	R25	O	CML	High-Speed Data Output Channel 34, Complement.
YN35	R1	O	CML	High-Speed Data Output Channel 35, Complement.
YN36	T29	O	CML	High-Speed Data Output Channel 36, Complement.
YN37	T5	O	CML	High-Speed Data Output Channel 37, Complement.
YN38	T25	O	CML	High-Speed Data Output Channel 38, Complement.
YN39	T1	O	CML	High-Speed Data Output Channel 39, Complement.
YN40	U29	O	CML	High-Speed Data Output Channel 40, Complement.
YN41	U5	O	CML	High-Speed Data Output Channel 41, Complement.
YN42	U25	O	CML	High-Speed Data Output Channel 42, Complement.
YN43	U1	O	CML	High-Speed Data Output Channel 43, Complement.
YN44	V29	O	CML	High-Speed Data Output Channel 44, Complement.

Table 11. Pin Identification for 480-Pin TBGA (UG) (continued)

Signal	Ball Site	I/O	Level	Description
YN45	V5	O	CML	High-Speed Data Output Channel 45, Complement.
YN46	V25	O	CML	High-Speed Data Output Channel 46, Complement.
YN47	V1	O	CML	High-Speed Data Output Channel 47, Complement.
YN48	W29	O	CML	High-Speed Data Output Channel 48, Complement.
YN49	W5	O	CML	High-Speed Data Output Channel 49, Complement.
YN50	W25	O	CML	High-Speed Data Output Channel 50, Complement.
YN51	W1	O	CML	High-Speed Data Output Channel 51, Complement.
YN52	Y29	O	CML	High-Speed Data Output Channel 52, Complement.
YN53	Y5	O	CML	High-Speed Data Output Channel 53, Complement.
YN54	Y25	O	CML	High-Speed Data Output Channel 54, Complement.
YN55	Y1	O	CML	High-Speed Data Output Channel 55, Complement.
YN56	AA29	O	CML	High-Speed Data Output Channel 56, Complement.
YN57	AA5	O	CML	High-Speed Data Output Channel 57, Complement.
YN58	AA25	O	CML	High-Speed Data Output Channel 58, Complement.
YN59	AA1	O	CML	High-Speed Data Output Channel 59, Complement.
YN60	AB29	O	CML	High-Speed Data Output Channel 60, Complement.
YN61	AB5	O	CML	High-Speed Data Output Channel 61, Complement.
YN62	AB25	O	CML	High-Speed Data Output Channel 62, Complement.
YN63	AB1	O	CML	High-Speed Data Output Channel 63, Complement.
YN64	AC29	O	CML	High-Speed Data Output Channel 64, Complement.
YN65	AC5	O	CML	High-Speed Data Output Channel 65, Complement.
YN66	AC25	O	CML	High-Speed Data Output Channel 66, Complement.
YN67	AC1	O	CML	High-Speed Data Output Channel 67, Complement.
Control Pins				
ACTCLK	AD2	I	TTL	Clock for Activity Monitor, <10MHz.
ACTIVITY	AD1	I	TTL	Activity Result from Previous ACTCLK Period.
ALE_SCN	AD25	I	TTL	Address Latch Enable for Multiplexed Parallel Mode; Scan Enable for Serial Mode. See Figure 1 through Figure 5 for proper use.
BURST	AH6	I	TTL	Logic HIGH sets Burst Mode
CMV	AD3	I	Analog	Output Drive Current Control. Leave floating.
CONFIG	F27	I	TTL	Logic HIGH Transfers Programming to Main Program Memory.
$\overline{CS}$	AF6	I	TTL	Chip Select, Active LOW. Selects between multiple devices.
DRIVE_CTRL	AD4	I	TTL	Output Drive Current Switch. LOW = 10mA, HIGH = 20mA.
INCHAN0_SDIN	AG24	I	TTL	Input Channel, Bit 0 and Serial Data in Serial Mode.
INCHAN1_SCLK	AF24	I	TTL	Input Channel, Bit 1 and Serial Clock in Serial Mode.
INCHAN2	AE24	I	TTL	Input Channel, Bit 2.
INCHAN3	AH24	I	TTL	Input Channel, Bit 3.
INCHAN4	AJ24	I	TTL	Input Channel, Bit 4.
INCHAN5	AD27	I	TTL	Input Channel, Bit 5.
INCHAN6	AD26	I	TTL	Input Channel, Bit 6.
$\overline{INIT}$	AJ6		TTL	$\overline{INIT}$ = 0 Forces “Straight-Through” Programming.

Table 11. Pin Identification for 480-Pin TBGA (UG) (continued)

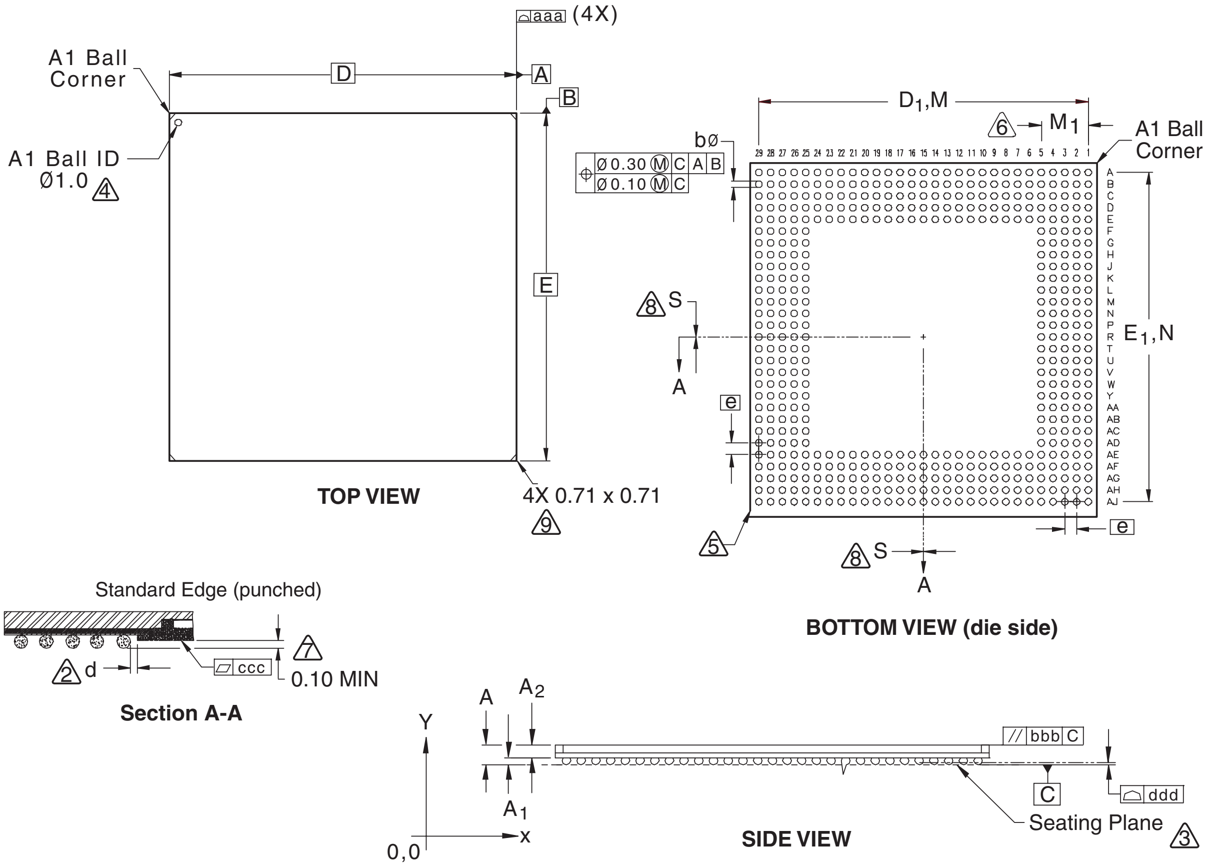
Signal	Ball Site	I/O	Level	Description
ITC	AD29		Analog	Input Termination Control. GND = floating input termination, V_{CC} = CML mode. See Table 7 on page 9. **NOTE:** Do not connect to V_{CC} or V_{EE} supplies using a high value resistor. If a resistor is used to connect ITC to V_{CC} or V_{EE}, the resistor value must be < 100Ω .
LOAD	AD28		TTL	Rising Edge Writes Data in Parallel and Burst Modes. See Figure 5 on page 7 for Serial Mode.
OUTCHAN0	F1	O	TTL	Output Channel, Bit 0.
OUTCHAN1	F2	O	TTL	Output Channel, Bit 1.
OUTCHAN2	F5	O	TTL	Output Channel, Bit 2.
OUTCHAN3	F4	O	TTL	Output Channel, Bit 3.
OUTCHAN4	F3	O	TTL	Output Channel, Bit 4.
OUTCHAN5	A6	O	TTL	Output Channel, Bit 5.
OUTCHAN6	B6	O	TTL	Output Channel, Bit 6.
OUTCHAN7	E6	O	TTL	Output Channel, Bit 7 (burst mode only).
OUTCHAN8	D6	O	TTL	Output Channel, Bit 8 (burst mode only).
OUTCHAN9	C6	O	TTL	Output Channel, Bit 9 (burst mode only).
OUTCHAN10	A24	O	TTL	Output Channel, Bit 10 (burst mode only).
OUTCHAN11	B24	O	TTL	Output Channel, Bit 11 (burst mode only).
OUTCHAN12	E24	O	TTL	Output Channel, Bit 12 (burst mode only).
OUTCHAN13	D24	O	TTL	Output Channel, Bit 13 (burst mode only).
OUTCHAN14	C24	O	TTL	Output Channel, Bit 14 (burst mode only).
OUTCHAN15	F29	O	TTL	Output Channel, Bit 15 (burst mode only).
OUTCHAN16	F28	O	TTL	Output Channel, Bit 16 (burst mode only).
OUTCHAN17	F25	O	TTL	Output Channel, Bit 17 (burst mode only).
OUTCHAN18	F26	O	TTL	Output Channel, Bit 18 (burst mode only).
SDOUT	AG6	O	TTL	Serial Data Out for Serial Mode and Scan.
SERIAL	AE6		TTL	SERIAL = 1 Sets Serial Mode.
TERM_CTRL	AD5		TTL	Output Back-Termination Control. LOW = no back termination; HIGH = 50Ω back-termination to V_{CC}. See Table 8 on page 9.

Table 12. Power Supplies

Signal	Ball Site	Level	Description
VEE	C23, C7, R3, AG7, AG23, R27	GND	Common Negative Power Supply
VCC	A1-A5, A25-A29, AE1-AE5, AE25-AE29, AF1-AF5, AF25-AF29, AG1-AG5, AG25-29, AH1-AH5, AH25-AH29,AJ1-AJ5, AJ25-AJ29 B1-B5, B25-B29 C1-C5, C25-C29 D1-D5, D25-D29 E1-E5, E25-E29	+2.5V	Positive Power Supply
VEEP_T1	C22	GND	Negative Power Supply for Inputs A4/AN4, A6/AN6
VEEP_T2	C21	GND	Negative Power Supply for Inputs A8/AN8, A10/AN10
VEEP_T3	C20	GND	Negative Power Supply for Inputs A12/AN12, A14/AN14
VEEP_T4	C19	GND	Negative Power Supply for Inputs A16/AN16, A18/AN18
VEEP_T5	C18	GND	Negative Power Supply for Inputs A20/AN20, A22/AN22
VEEP_T6	C17	GND	Negative Power Supply for Inputs A24/AN24, A26/AN26
VEEP_T7	C16	GND	Negative Power Supply for Inputs A28/AN28, A30/AN30
VEEP_T8	C15	GND	Negative Power Supply for Inputs A32/AN32, A34/AN34
VEEP_T9	C14	GND	Negative Power Supply for Inputs A36/AN36, A38/AN38
VEEP_T10	C13	GND	Negative Power Supply for Inputs A40/AN40, A42/AN42
VEEP_T11	C12	GND	Negative Power Supply for Inputs A44/AN44, A46/AN46
VEEP_T12	C11	GND	Negative Power Supply for Inputs A48/AN48, A50/AN50
VEEP_T13	C10	GND	Negative Power Supply for Inputs A52/AN52, A54/AN54
VEEP_T14	C9	GND	Negative Power Supply for Inputs A56/AN56, A58/AN58
VEEP_T15	C8	GND	Negative Power Supply for Inputs A60/AN60, A62/AN62
VEEP_B1	AG22	GND	Negative Power Supply for Inputs A5/AN5, A7/AN7
VEEP_B2	AG21	GND	Negative Power Supply for Inputs A9/AN9, A11/AN11
VEEP_B3	AG20	GND	Negative Power Supply for Inputs A13/AN13, A15/AN15
VEEP_B4	AG19	GND	Negative Power Supply for Inputs A17/AN17, A19/AN19
VEEP_B5	AG18	GND	Negative Power Supply for Inputs A21/AN21, A23/AN23
VEEP_B6	AG17	GND	Negative Power Supply for Inputs A25/AN25, A27/AN27
VEEP_B7	AG16	GND	Negative Power Supply for Inputs A29/AN29, A31/AN31
VEEP_B8	AG15	GND	Negative Power Supply for Inputs A33/AN33, A35/AN35
VEEP_B9	AG14	GND	Negative Power Supply for Inputs A37/AN37, A39/AN39
VEEP_B10	AG13	GND	Negative Power Supply for Inputs A41/AN41, A43/AN43
VEEP_B11	AG12	GND	Negative Power Supply for Inputs A45/AN45, A47/AN47
VEEP_B12	AG11	GND	Negative Power Supply for Inputs A49/AN49, A51/AN51
VEEP_B13	AG10	GND	Negative Power Supply for Inputs A53/AN53, A55/AN55
VEEP_B14	AG9	GND	Negative Power Supply for Inputs A57/AN57, A59/AN59
VEEP_B15	AG8	GND	Negative Power Supply for Inputs A61/AN61, A63/AN63
VEEP_L0	G3	GND	Negative Power Supply for Outputs Y1/YN1, Y3/YN3
VEEP_L1	H3	GND	Negative Power Supply for Outputs Y5/YN5, Y7/YN7
VEEP_L2	J3	GND	Negative Power Supply for Outputs Y9/YN9, Y11/YN11

Table 12. Power Supplies

Signal	Ball Site	Level	Description
VEEP_L3	K3	GND	Negative Power Supply for Outputs Y13/YN13, Y15/YN15
VEEP_L4	L3	GND	Negative Power Supply for Outputs Y17/YN17, Y19/YN19
VEEP_L5	M3	GND	Negative Power Supply for Outputs Y21/YN21, Y23/YN23
VEEP_L6	N3	GND	Negative Power Supply for Outputs Y25/YN25, Y27/YN27
VEEP_L7	P3	GND	Negative Power Supply for Outputs Y29/YN29, Y31/YN31
VEEP_L9	T3	GND	Negative Power Supply for Outputs Y37/YN37, Y39/YN39
VEEP_L10	U3	GND	Negative Power Supply for Outputs Y41/YN41, Y43/YN43
VEEP_L11	V3	GND	Negative Power Supply for Outputs Y45/YN45, Y47/YN47
VEEP_L12	W3	GND	Negative Power Supply for Outputs Y49/YN49, Y51/YN51
VEEP_L13	Y3	GND	Negative Power Supply for Outputs Y53/YN53, Y55/YN55
VEEP_L14	AA3	GND	Negative Power Supply for Outputs Y57/YN57, Y59/YN59
VEEP_L15	AB3	GND	Negative Power Supply for Outputs Y61/YN61, Y63/YN63
VEEP_L16	AC3	GND	Negative Power Supply for Outputs Y65/YN65, Y67/YN67
VEEP_R0	G27	GND	Negative Power Supply for Outputs Y0/YN0, Y2/YN2
VEEP_R1	H27	GND	Negative Power Supply for Outputs Y4/YN4, Y6/YN6
VEEP_R2	J27	GND	Negative Power Supply for Outputs Y8/YN8, Y10/YN10
VEEP_R3	K27	GND	Negative Power Supply for Outputs Y12/YN12, Y14/YN14
VEEP_R4	L27	GND	Negative Power Supply for Outputs Y16/YN16, Y18/YN18
VEEP_R5	M27	GND	Negative Power Supply for Outputs Y20/YN20, Y22/YN22
VEEP_R6	N27	GND	Negative Power Supply for Outputs Y24/YN24, Y26/YN26
VEEP_R7	P27	GND	Negative Power Supply for Outputs Y28/YN28, Y30/YN30
VEEP_R9	T27	GND	Negative Power Supply for Outputs Y36/YN36, Y38/YN38
VEEP_R10	U27	GND	Negative Power Supply for Outputs Y40/YN40, Y42/YN42
VEEP_R11	V27	GND	Negative Power Supply for Outputs Y44/YN44, Y46/YN46
VEEP_R12	W27	GND	Negative Power Supply for Outputs Y48/YN48, Y50/YN50
VEEP_R13	Y27	GND	Negative Power Supply for Outputs Y52/YN52, Y54/YN54
VEEP_R14	AA27	GND	Negative Power Supply for Outputs Y56/YN56, Y58/YN58
VEEP_R15	AB27	GND	Negative Power Supply for Outputs Y60/YN60, Y62/YN62
VEEP_R16	AC27	GND	Negative Power Supply for Outputs Y64/YN64, Y66/YN66



NOTES:

SYMBOL	MIN	TYP	MAX	NOTE
A			1.925	Overall thickness
A_1	0.50	0.60	0.70	Ball height
A_2	1.025	1.125	1.225	Body thickness
D		37.5		Body size
D_1	35.46	35.56	35.66	Ball footprint
E		37.5		Body size
E_1	35.46	35.56	35.66	Ball footprint
M, N		29 x 29		Ball matrix
M1 6		5		Number of rows deep
b	0.60	0.75	0.90	Ball diameter
d	0.25			Min distance encap to balls
e		1.27		Ball pitch
aaa			0.20	Package body profile
bbb			0.25	Parallel
ccc			0.20	Encap flatness over die
ddd			0.20	Coplanarity
S		0.00		Solder ball placement

All dimensions are in millimeters unless otherwise noted.

1. All dimensions and tolerances conform to ASME Y14.5M-1994.
2. Dimension “d” is measured at the maximum solder ball diameter, parallel to primary datum C .
3. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
4. Pin A1 I.D. mark, half etched.
5. Shape at corner:

6. Number of rows in from edge to center.
7. Seating plane clearance: maximum height of encapsulant above seating plane.
8. "S" is measured with respect to A and B and defines the position of the center solder ball in the outer row. When there is an odd number of solder balls in the outer row, "S" = 0.000; when there is an even bumber of solder balls in the outer row, the value "S" = e/2. "S" may be either 0.000 or e/2 for each variation.
9. Heat spreader corner profile, square or chamfered, is determined by heat spreader strip configuration.

Figure 8. Package Drawing for 480-Pin TBGA (UG)

Thermal Specifications

Thermal specifications for this device are based on the JEDEC standard EIA/JESD51-2 and have been modeled using a four-layer test board with two signal layers, a power plane, and a ground plane (2s2p PCB). For more information, see the JEDEC standard.

Table 13. Thermal Resistances

Package	θ_{JC}	θ_{JA} (°C/W) vs. Airflow (ft/min)		
		0	100	200
VSC837UG	0.134	11.04	10.1	8.6

Heat Sink Recommendations

A heat sink is required to prevent damage to the device. Please contact your local Vitesse sales representative for recommended heat sink applications.

Moisture Sensitivity Level

This device is rated moisture sensitivity level 3 or better as specified in JEDEC standard IPC/JEDEC J-STD-020B. For more information, see the JEDEC standard.

ORDERING INFORMATION

VSC837 3.2Gb/s 68x68 Crosspoint Switch

Part Number	Description
VSC837UG	480-Pin TBGA, 37.5mm x 37.5mm Body Temperature Range: 0°C ambient to +85°C case

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