



SS-5-8212 ✓
 SS-6-8212 ✓
 SS-7-8212 ✓

S-34

ORIG

002650

T-2650

G1

Dual 16-Bit Static Shift Registers

FEATURES

- TTL/DTL Compatible Clock Input
- TTL/DTL Compatible Data—
No external interfacing components required on data inputs or outputs.
- DC-2MHz Operation
- Full Static Operation—
Data is stored independently of the clock logic level.
- Two Temperature Ranges—
SS-5 & SS-7: 0°C to +70°C
SS-6: -55°C to +125°C
- Zener Protected Inputs
- Glass Passivation Protection

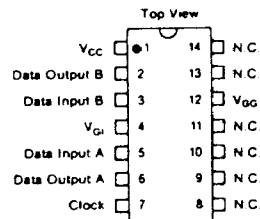
DESCRIPTION

The SS-5-8212, SS-6-8212 and SS-7-8212 are dual 16-bit static shift registers with clock and data inputs and outputs that interface directly with TTL/DTL logic arrays without the use of any special interface components. These devices contain two independent common clock 16-bit DC to 2MHz shift registers, constructed on a single monolithic chip utilizing MTNS P-Channel enhancement mode transistors. Each shift register bit is implemented with a cross coupled flip-flop, so that data is stored indefinitely regardless of the logic level of the clock. A single phase clock input is provided for both registers. Data on the input is sampled while the clock is at a "0" level and the register shifts on a "0" to "1" transition.

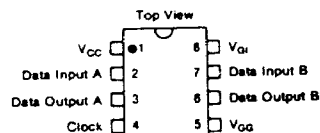
*Available only in Europe (14 Lead Plastic DIP)

PIN CONFIGURATIONS

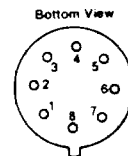
14 LEAD DUAL IN-LINE



8 LEAD DUAL IN-LINE

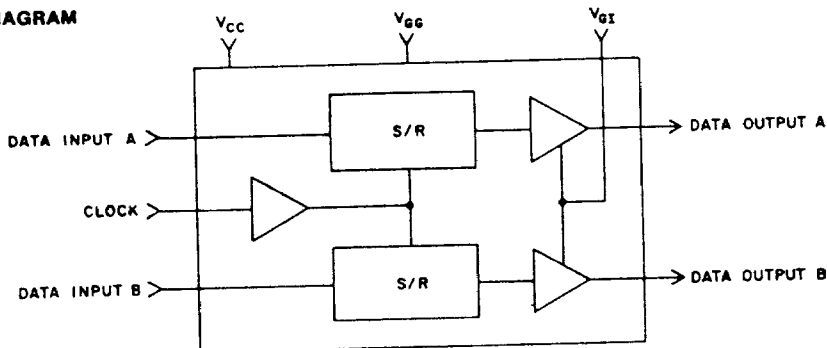


8 LEAD TO-78



- | | |
|-------------------|-------------------|
| 1 Data Input A | 5 V _{GG} |
| 2 Data Output A | 6 Data Output B |
| 3 Clock | 7 Data Input B |
| 4 V _{CC} | 8 V _{GI} |

BLOCK DIAGRAM



Maximum Ratings*

V _{GG} and V _G with respect to V _{CC}	-20V to +0.3V
Clock and Data Inputs with respect to V _{CC}	-15V to +0.3V
Storage Temperature	-65°C to +150°C
Operating Temperature: SS-5-8212, SS-7-8212	0°C to +70°C
SS-6-8212	-55°C to +125°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

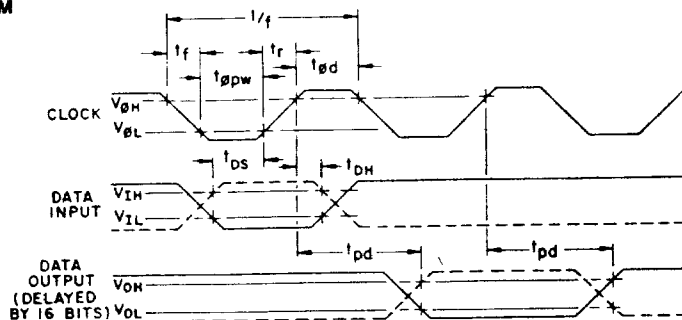
V_{CC} = +5 Volts ±0.5 Volts (V_{CC} is the substrate voltage)
 V_{GG} = -12 Volts ±1 Volt
 V_{G1} = GND
 Operating Temperature (T_A) = 0°C to +70°C (SS-5-8212, SS-7-8212)
 = -55°C to +125°C (SS-6-8212)

One TTL load (C_L total = 10 pF)

Characteristic	Symbol	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Clock Input						
Logic 1 Level	V _{OH}	V _{CC} -1.5	—	—	Volts	V _{in} = V _{CC} -10V
Logic 0 Level	V _{OL}	—	—	+0.8	Volts	
Leakage	I _{Le}	—	—	10	μA	
Data Input						
Logic 1 Level	V _{IH}	V _{CC} -1.5	—	—	Volts	V _{in} = V _{CC} -10V
Logic 0 Level	V _{IL}	—	—	+0.8	Volts	
Leakage	I _{LI}	—	—	10	μA	
Data Output						
Logic 1 Level	V _{OH}	V _{CC} -1.0	—	—	Volts	I _{OH} = 100 μA I _{OL} = 1.6 mA
Logic 0 Level	V _{OL}	—	—	+0.4	Volts	
Power	—	—	125	160	mW	SL-5-8212, SL-7-8212 SL-6-8212
	—	—	125	200	mW	
AC CHARACTERISTICS						
Clock Input						
Frequency	f	DC	—	2.0	MHz	} t _r + t _{pdw} + t _r + t _{ed} ≥ 500ns 1MHz, T _A = +25°C
Pulse Width	t _{pdw}	200	150	—	ns	
Pulse Delay	t _{pd}	200	—	—	ns	
Rise and Fall Times	t _r , t _f	—	—	1000	ns	
Capacitance	C _e	—	15	—	pF	
Data Input						
Set Up Time	t _{DS}	100	50	—	ns	1MHz, T _A = +25°C
Hold Time	t _{DH}	10	0	—	ns	
Capacitance	C _i	—	5	—	pF	
Data Output						
Propagation Delay	t _{pd}	—	150	225	ns	SL-5-8212, SL-7-8212 SL-6-8212
	t _{pd}	—	150	300	ns	

**Typical values are at -25°C and nominal voltages

TIMING DIAGRAM



MEMORY