



CAT525

Configured Digitally Programmable Potentiometer (DPP™):
Programmable Voltage Applications



FEATURES

- Four 8-bit DPPs configured as programmable voltage sources in DAC-like applications
- Independent reference inputs
- Buffered wiper outputs
- Non-volatile NVRAM memory wiper storage
- Output voltage range includes both supply rails
- 4 independently addressable buffered output wipers
- 1 LSB accuracy, high resolution
- Serial Microwire-like interface

- Single supply operation: 2.7V - 5.5V
- Setting read-back without effecting outputs

APPLICATIONS

- Automated product calibration
- Remote control adjustment of equipment
- Offset, gain and zero adjustments in self-calibrating and adaptive control systems
- Tamper-proof calibrations
- DAC (with memory) substitute

DESCRIPTION

The CAT525 is a quad 8-bit digitally programmable potentiometer (DPP™) configured for programmable voltage and DAC-like applications. Intended for final calibration of products such as camcorders, fax machines and cellular telephones on automated high volume production lines and systems capable of self calibration, it is also well suited for applications where equipment requiring periodic adjustment is either difficult to access or located in a hazardous environment.

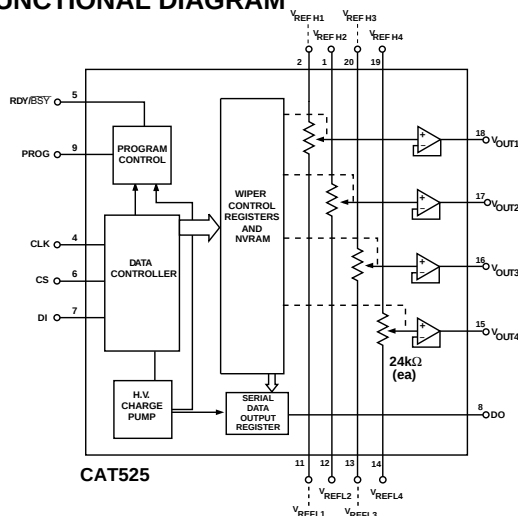
The CAT525 offers four independently programmable DPPs each having its own reference inputs and each capable of rail to rail output swing. The wipers are buffered by rail to rail op amps. Wiper settings, stored in non-volatile NVRAM memory, are not lost when the device is powered down and are automatically reinstated when power is returned. Each wiper can be dithered to

test new output values without effecting the stored settings and stored settings can be read back without disturbing the DPP's output.

Control of the CAT525 is accomplished with a simple 3-wire, Microwire-like serial interface. A Chip Select pin allows several CAT525's to share a common serial interface and communications back to the host controller is via a single serial data line thanks to the CAT525's Tri-Stated Data Output pin. A RDY/BSY output working in concert with an internal low voltage detector signals proper operation of non-volatile NVRAM Memory Erase/Write cycle.

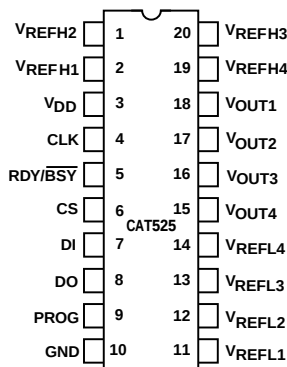
The CAT525 is available in the 0°C to 70°C commercial and -40°C to 85°C industrial operating temperature ranges and offered in 20-pin plastic DIP and surface mount packages.

FUNCTIONAL DIAGRAM

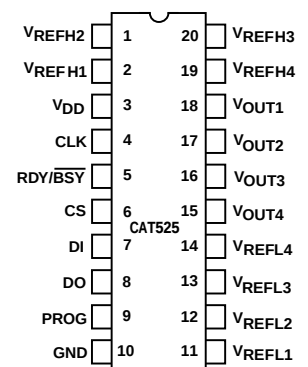


PIN CONFIGURATION

DIP Package (P, L)



SOIC Package (J, W)



ABSOLUTE MAXIMUM RATINGS

Supply Voltage*

V_{DD} to GND -0.5V to +7V

Inputs

CLK to GND -0.5V to V_{DD} +0.5VCS to GND -0.5V to V_{DD} +0.5VDI to GND -0.5V to V_{DD} +0.5VRDY/BSY to GND -0.5V to V_{DD} +0.5VPROG to GND -0.5V to V_{DD} +0.5VV_{REFH} to GND -0.5V to V_{DD} +0.5VV_{REFL} to GND -0.5V to V_{DD} +0.5V

Outputs

D₀ to GND -0.5V to V_{DD} +0.5VV_{OUT} 1– 4 to GND -0.5V to V_{DD} +0.5V

Operating Ambient Temperature

Commercial ('C' or Blank suffix) 0°C to +70°C

Industrial ('I' suffix) -40°C to +85°C

Junction Temperature +150°C

Storage Temperature -65°C to +150°C

Lead Soldering (10 sec max) +300°C

* Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Absolute Maximum Ratings are limited values applied individually while other parameters are within specified operating conditions, and functional operation at any of these conditions is NOT implied. Device performance and reliability may be impaired by exposure to absolute rating conditions for extended periods of time.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min	Max	Units	Test Method
V _{ZAP} ⁽¹⁾	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I _{LTH} ⁽¹⁾⁽²⁾	Latch-Up	100		mA	JEDEC Standard 17

NOTES: 1. This parameter is tested initially and after a design or process change that affects the parameter.

2. Latch-up protection is provided for stresses up to 100mA on address and data pins from -1V to V_{CC} + 1V.

POWER SUPPLY

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I _{DD1}	Supply Current (Read)	Normal Operating	—	400	600	μA
I _{DD2}	Supply Current (Write)	Programming, V _{DD} = 5V	—	1600	2500	μA
		V _{DD} = 3V	—	1000	1600	μA
V _{DD}	Operating Voltage Range		2.7	—	5.5	V

LOGIC INPUTS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I _{IH}	Input Leakage Current	V _{IN} = V _{DD}	—	—	10	μA
I _{IL}	Input Leakage Current	V _{IN} = 0V	—	—	-10	μA
V _{IH}	High Level Input Voltage		2	—	V _{DD}	V
V _{IL}	Low Level Input Voltage		0	—	0.8	V

LOGIC OUTPUTS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V _{OH}	High Level Output Voltage	I _{OH} = -40μA	V _{DD} -0.3	—	—	V
V _{IL}	Low Level Output Voltage	I _{OL} = 1 mA, V _{DD} = +5V	—	—	0.4	V
		I _{OL} = 0.4 mA, V _{DD} = +3V	—	—	0.4	V

POTENTIOMETER CHARACTERISTICS

$V_{DD} = +2.7V$ to $+5.5V$, $V_{REFH} = V_{DD}$, $V_{REFL} = 0V$, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
R_{POT}	Potentiometer Resistance			24		$k\Omega$
	R_{POT} to R_{POT} Match		—	± 0.5	± 1	%
	Pot Resistance Tolerance				± 20	%
	Voltage on V_{REFH} pin		2.7		V_{DD}	V
	Voltage on V_{REFL} pin		0V		$V_{DD} - 2.7$	V
	Resolution			0.4		%
INL	Integral Linearity Error			0.5	1	LSB
DNL	Differential Linearity Error			0.25	0.5	LSB
R_{OUT}	Buffer Output Resistance				10	Ω
I_{OUT}	Buffer Output Current				3	mA
TC_{RPOT}	TC of Pot Resistance			300		ppm/ $^{\circ}C$
C_H/C_L	Potentiometer Capacitances			8/8		pF

AC ELECTRICAL CHARACTERISTICS:

$V_{DD} = +2.7V$ to $+5.5V$, $V_{REFH} = V_{DD}$, $V_{REFL} = 0V$, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
--------	-----------	------------	-----	-----	-----	-------

Digital

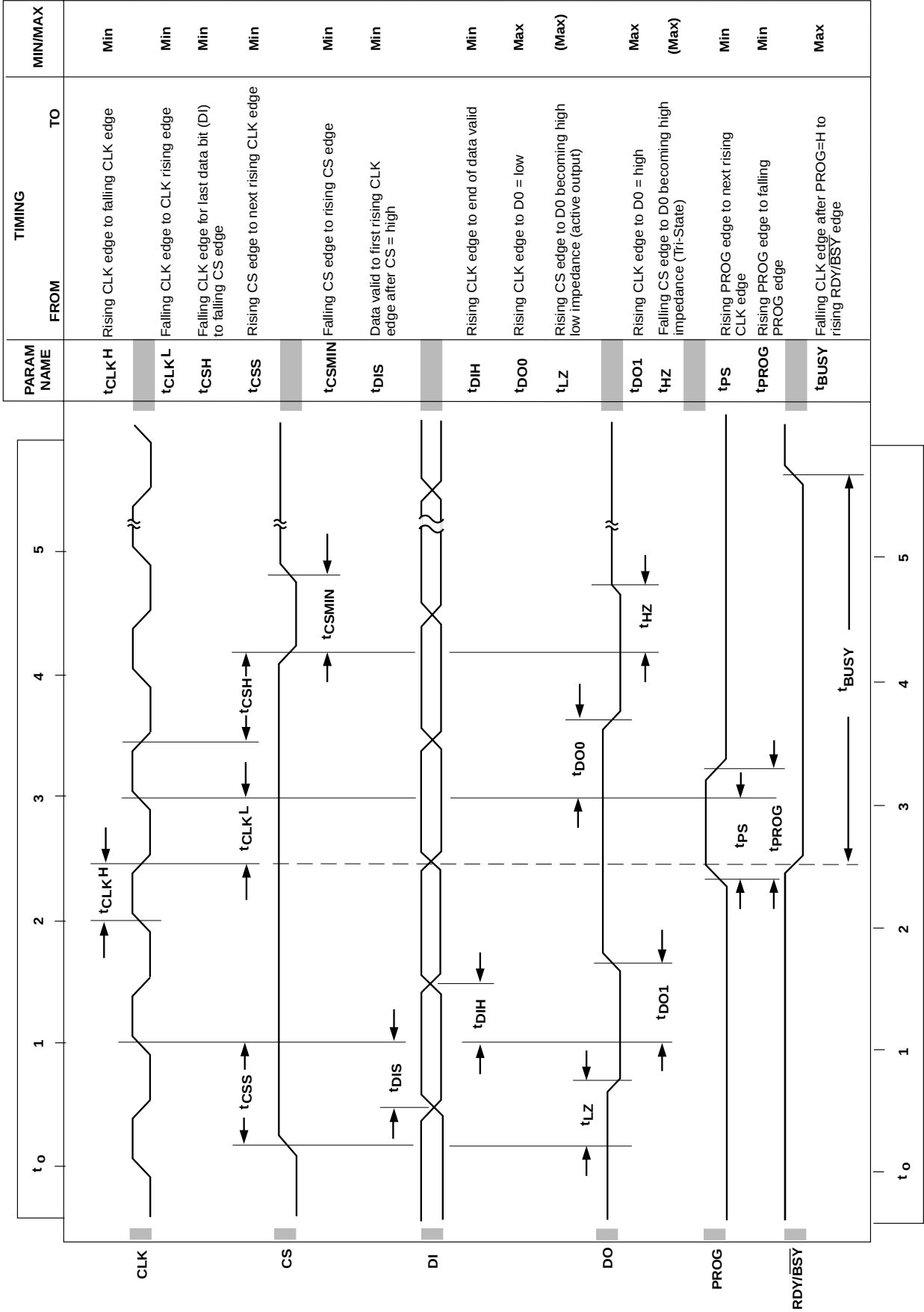
t_{CSMIN}	Minimum CS Low Time		150	—	—	ns
t_{CSS}	CS Setup Time		100	—	—	ns
t_{CSH}	CS Hold Time	$C_L = 100pF$, see note 1	0	—	—	ns
t_{DIS}	DI Setup Time		50	—	—	ns
t_{DIH}	DI Hold Time		50	—	—	ns
t_{DO1}	Output Delay to 1		—	—	150	ns
t_{DO0}	Output Delay to 0		—	—	150	ns
t_{HZ}	Output Delay to High-Z		—	400	—	ns
t_{LZ}	Output Delay to Low-Z		—	400	—	ns
t_{BUSY}	Erase/Write Cycle Time		—	4	5	ms
t_{PS}	PROG Setup Time		150	—	—	ns
t_{PROG}	Minimum Pulse Width		700	—	—	ns
t_{CLKH}	Minimum CLK High Time		500	—	—	ns
t_{CLKL}	Minimum CLK Low Time		300	—	—	ns
f_C	Clock Frequency		DC	—	1	MHz

Analog

t_{DS}	DPP Settling Time to 1 LSB	$C_{LOAD} = 10 pF$, $V_{DD} = +5V$	—	3	10	μs
		$C_{LOAD} = 10 pF$, $V_{DD} = +3V$	—	6	10	μs

- NOTES:** 1. All timing measurements are defined at the point of signal crossing $V_{DD} / 2$.
2. These parameters are periodically sampled and are not 100% tested.

A. C. TIMING DIAGRAM



PIN DESCRIPTION

Pin	Name	Function
1	V _{REFH2}	Maximum DPP 2 output voltage
2	V _{REFH1}	Maximum DPP 1 output voltage
3	V _{DD}	Power supply positive
4	CLK	Clock input pin
5	RDY/ $\overline{\text{BSY}}$	Ready/Busy output
6	CS	Chip select
7	DI	Serial data input pin
8	DO	Serial data output pin
9	PROG	Non-volatile Memory Programming Enable Input
10	GND	Power supply ground
11	V _{REFL1}	Minimum DPP 1 output voltage
12	V _{REFL2}	Minimum DPP 2 output voltage
13	V _{REFL3}	Minimum DPP 3 output voltage
14	V _{REFL4}	Minimum DPP 4 output voltage
15	V _{OUT4}	DPP 4 output
16	V _{OUT3}	DPP 3 output
17	V _{OUT2}	DPP 2 output
18	V _{OUT1}	DPP 1 output
19	V _{REFH4}	Maximum DPP 4 output voltage
20	V _{REFH3}	Maximum DPP 3 output voltage

CDPP/DPP addressing is as follows:

DPP OUTPUT	A0	A1
V _{OUT1}	0	0
V _{OUT2}	1	0
V _{OUT3}	0	1
V _{OUT4}	1	1

DEVICE OPERATION

The CAT525 is a quad 8-bit configured digitally programmable potentiometer (DPP/CDPP) whose outputs can be programmed to any one of 256 individual voltage steps. Once programmed, these output settings are retained in non-volatile memory and will not be lost when power is removed from the chip. Upon power up the DPPs return to the settings stored in non-volatile memory. Each configured DPP can be written to and read from independently without effecting the output voltage during the read or write cycle. Each output can also be adjusted without altering the stored output setting, which is useful for testing new output settings before storing them in memory.

DIGITAL INTERFACE

The CAT525 employs a 3 wire serial, Microwire-like control interface consisting of Clock (CLK), Chip Select (CS) and Data In (DI) inputs. For all operations, address and data are shifted in LSB first. In addition, all digital data must be preceded by a logic "1" as a start bit. The DPP address and data are clocked into the DI pin on the clock's rising edge. When sending multiple blocks of information a minimum of two clock cycles is required between the last block sent and the next start bit.

Multiple devices may share a common input data line by selectively activating the CS control of the desired IC. Data Outputs (DO) can also share a common line because the DO pin is Tri-Stated and returns to a high

impedance when not in use.

CHIP SELECT

Chip Select (CS) enables and disables the CAT525's read and write operations. When CS is high data may be read to or from the chip, and the Data Output (DO) pin is active. Data loaded into the DPP wiper control registers will remain in effect until CS goes low. Bringing CS to a logic low returns all DPP outputs to the settings stored in non-volatile memory and switches DO to its high impedance Tri-State mode.

Because CS functions like a reset the CS pin has been desensitized with a 30 ns to 90 ns filter circuit to prevent noise spikes from causing unwanted resets and the loss of volatile data.

CLOCK

The CAT525's clock controls both data flow in and out of the IC and non-volatile memory cell programming. Serial data is shifted into the DI pin and out of the DO pin on the clock's rising edge. While it is not necessary for the clock to be running between data transfers, the clock must be operating in order to write to non-volatile memory, even though the data being saved may already be resident in the DPP wiper control register.

No clock is necessary upon system power-up. The CAT525's internal power-on reset circuitry loads data from non-volatile memory to the DPPs without using the external clock.

As data transfers are edge triggered clean clock transitions are necessary to avoid falsely clocking data into the control registers. Standard CMOS and TTL logic families work well in this regard and it is recommended that any mechanical switches used for breadboarding or device evaluation purposes be debounced by a flip-flop or other suitable debouncing circuit.

V_{REF}

V_{REF}, the voltage applied between pins V_{REFH} & V_{REFL}, sets the configured DPP's Zero to Full Scale output range where V_{REFL} = Zero and V_{REFH} = Full Scale. V_{REF} can span the full power supply range or just a fraction of it. In typical applications V_{REFH} & V_{REFL} are connected across the power supply rails. When using less than the full supply voltage be mindful of the limits placed on V_{REFH} and V_{REFL} as specified in the References section of DC Electrical Characteristics.

READY/BUSY

When saving data to non-volatile memory, the Ready/Busy output (RDY/BSY) signals the start and duration of the erase/write cycle. Upon receiving a command to store data (PROG goes high) RDY/BSY goes low and remains low until the programming cycle is complete. During this time the CAT525 will ignore any data appearing at DI and no data will be output on DO.

RDY/BSY is internally ANDed with a low voltage detector circuit monitoring V_{DD}. If V_{DD} is below the minimum value required for EEPROM programming, RDY/BSY will remain high following the program command indicating a failure to record the desired data in non-volatile memory.

DATA OUTPUT

Data is output serially by the CAT525, LSB first, via the Data Out (DO) pin following the reception of a start bit and two address bits by the Data Input (DI). DO becomes active whenever CS goes high and resumes its high impedance Tri-State mode when CS returns low. Tri-Stating the DO pin allows several 525s to share a

single serial data line and simplifies interfacing multiple 525s to a microprocessor.

WRITING TO MEMORY

Programming the CAT525's non-volatile memory is accomplished through the control signals: Chip Select (CS) and Program (PROG). With CS high, a start bit followed by a two bit DPP address and eight data bits are clocked into the DPP wiper control register via the DI pin. Data enters on the clock's rising edge. The DPP output changes to its new setting on the clock cycle following D7, the last data bit.

Programming is accomplished by bringing PROG high sometime after the start bit and at least 150 ns prior to the rising edge of the clock cycle immediately following the D7 bit. Two clock cycles after the D7 bit the DPP control register will be ready to receive the next set of address and data bits. The clock must be kept running throughout the programming cycle. Internal control circuitry takes care of generating and ramping up the programming voltage for data transfer to the non-volatile memory cells. The CAT525's non-volatile memory cells will endure over 100,000 write cycles and will retain data for a minimum of 20 years without being refreshed.

READING DATA

Each time data is transferred into a DPP wiper control register currently held data is shifted out via the D0 pin, thus in every data transaction a read cycle occurs. Note, however, that the reading process is destructive. Data must be removed from the register in order to be read. Figure 2 depicts a Read Only cycle in which no change occurs in the DPP's output. This feature allows μ Ps to poll DPPs for their current setting without disturbing the output voltage but it assumes that the setting being read is also stored in non-volatile memory so that it can be restored at the end of the read cycle. In Figure 2 CS returns low before the 13th clock cycle completes. In doing so the non-volatile memory setting is reloaded into the DPP wiper control register. Since this value is the

Figure 1. Writing to Memory

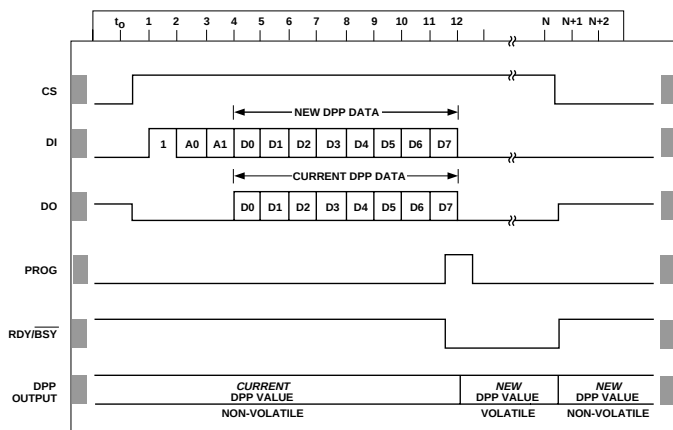
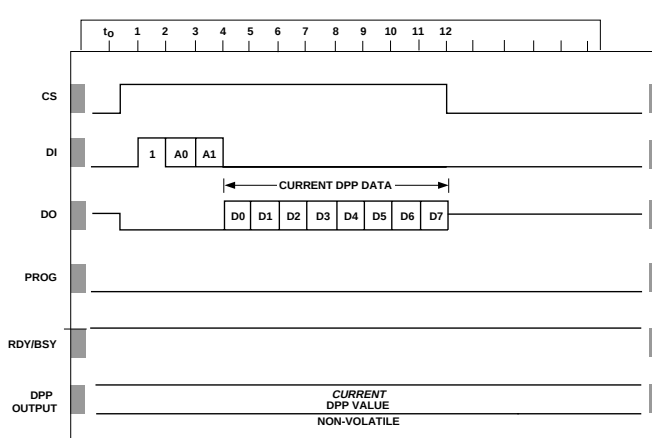


Figure 2. Reading from Memory



same as that which had been there previously no change in the DPP's output is noticed. Had the value held in the control register been different from that stored in non-volatile memory then a *change would occur* at the read cycle's conclusion.

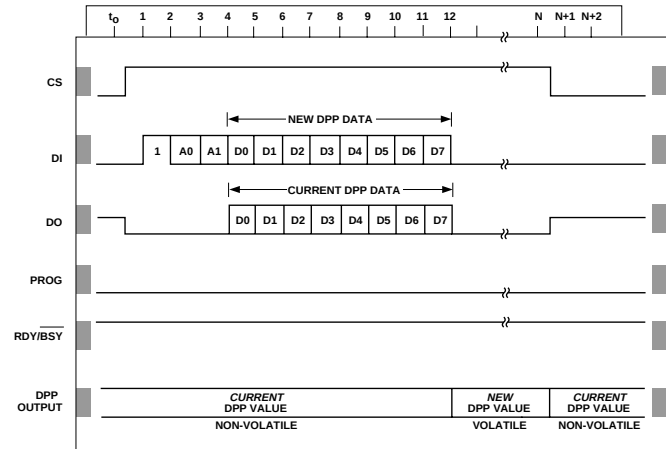
TEMPORARILY CHANGE OUTPUT

The CAT525 allows temporary changes in DPP's output to be made without disturbing the settings retained in non-volatile memory. This feature is particularly useful when testing for a new output setting and allows for user adjustment of preset or default values without losing the original factory settings.

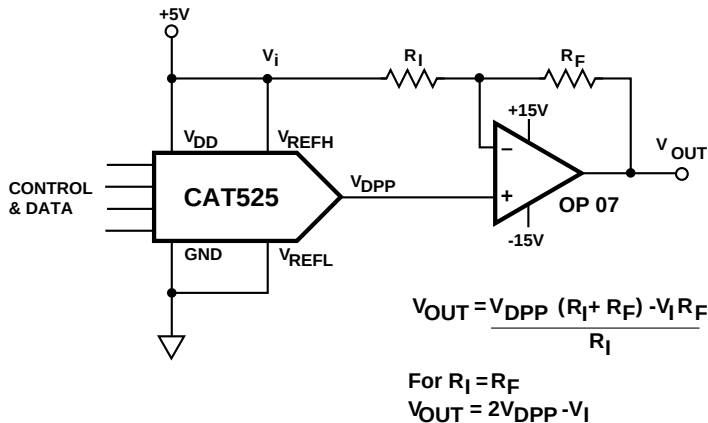
Figure 3 shows the control and data signals needed to effect a temporary output change. DPP settings may be changed as many times as required and can be made to any of the four DPPs in any order or sequence. The temporary setting(s) remain in effect long as CS remains high. When CS returns low all four DPPs will return to the output values stored in non-volatile memory.

When it is desired to save a new setting acquired using this feature, the new value must be reloaded into the DPP control register prior to programming. This is because the CAT525's internal control circuitry discards from the programming register the new data two clock cycles after receiving it if no PROG signal is received.

Figure 3. Temporary Change in Output

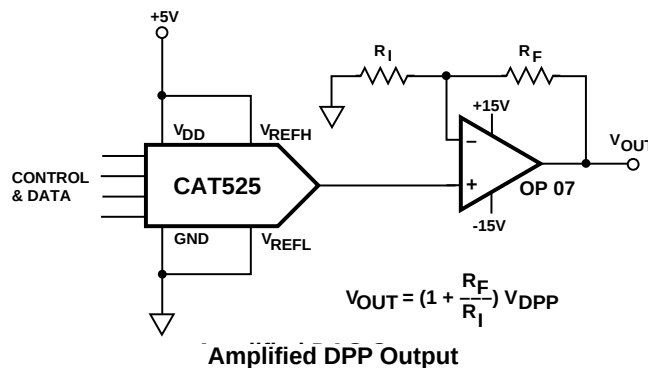


APPLICATION CIRCUITS

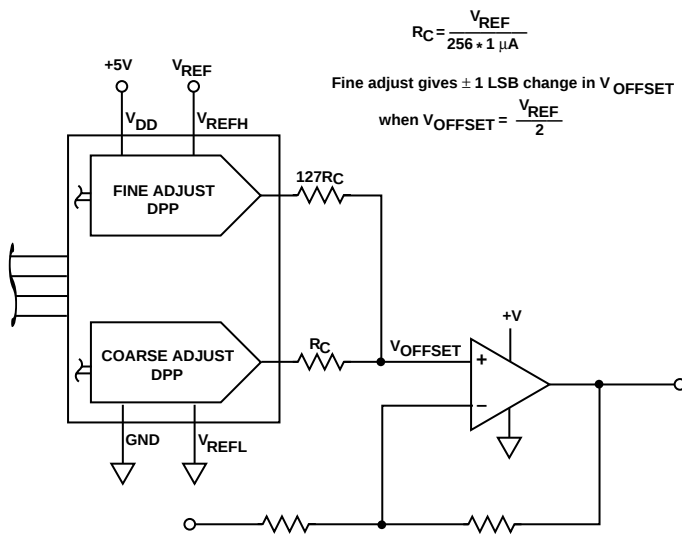


DPP INPUT		DPP OUTPUT	ANALOG OUTPUT
		$V_{DPP} = \frac{CODE}{255} (V_{FS} - V_{ZERO}) + V_{ZERO}$	
		$V_{FS} = 0.99 V_{REF}$	$V_{REF} = 5V$
MSB	LSB	$V_{ZERO} = 0.01 V_{REF}$	$R_I = R_F$
1111	1111	$\frac{255}{255} (.98 V_{REF}) + .01 V_{REF} = .990 V_{REF}$	$V_{OUT} = +4.90V$
1000	0000	$\frac{128}{255} (.98 V_{REF}) + .01 V_{REF} = .502 V_{REF}$	$V_{OUT} = +0.02V$
0111	1111	$\frac{127}{255} (.98 V_{REF}) + .01 V_{REF} = .498 V_{REF}$	$V_{OUT} = -0.02V$
0000	0001	$\frac{1}{255} (.98 V_{REF}) + .01 V_{REF} = .014 V_{REF}$	$V_{OUT} = -4.86V$
0000	0000	$\frac{0}{255} (.98 V_{REF}) + .01 V_{REF} = .010 V_{REF}$	$V_{OUT} = -4.90V$

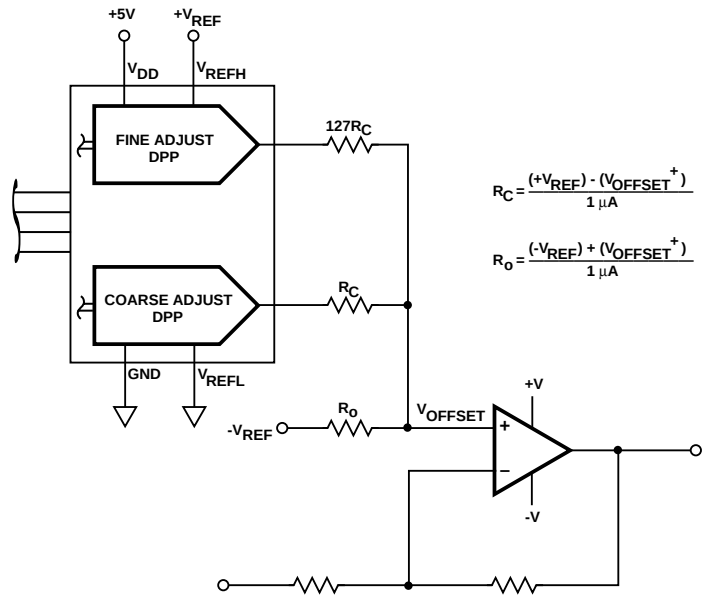
Bipolar DPP Output



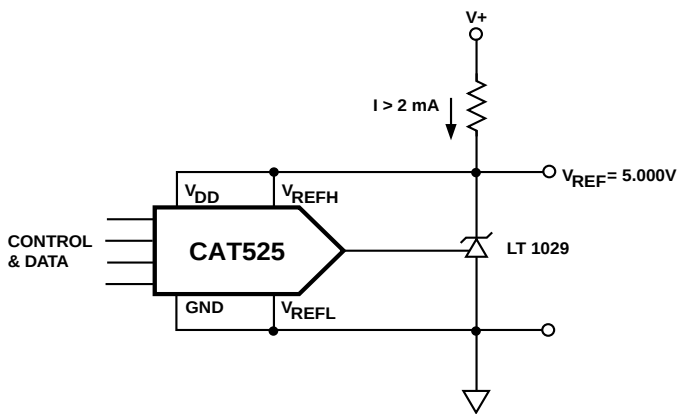
APPLICATION CIRCUITS (Cont.)



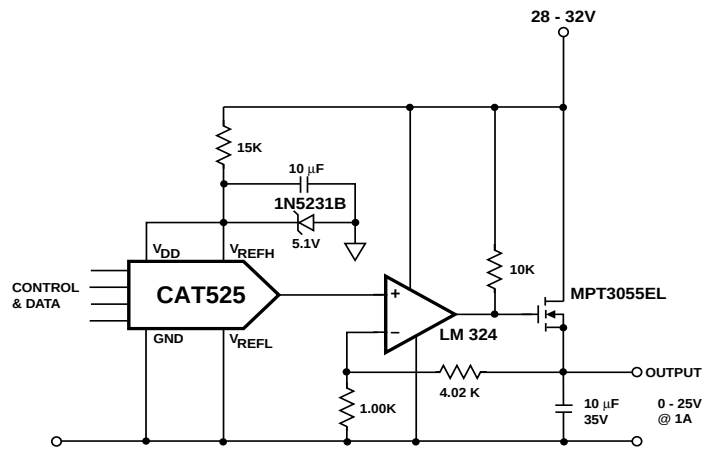
Coarse-Fine Offset Control by Averaging DPP Outputs for Single Power Supply Systems



Coarse-Fine Offset Control by Averaging DPP Outputs for Dual Power Supply Systems

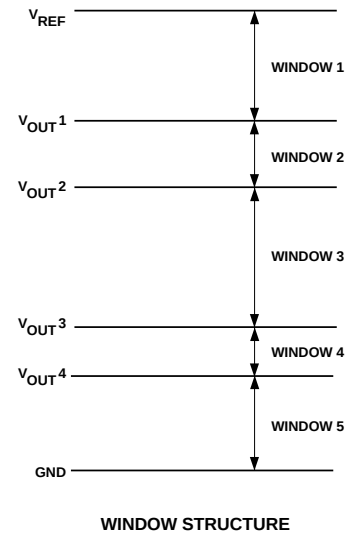
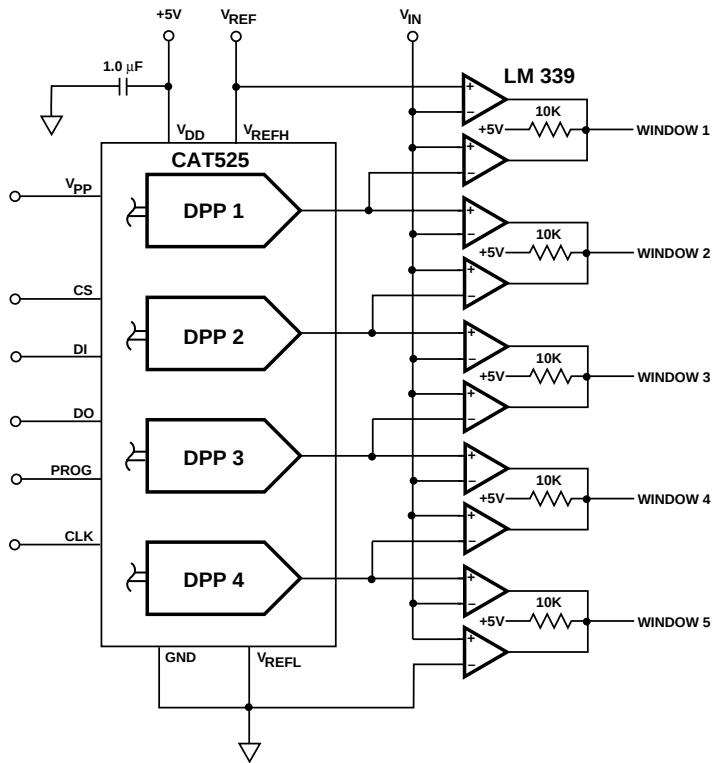


Digitally Trimmed Voltage Reference

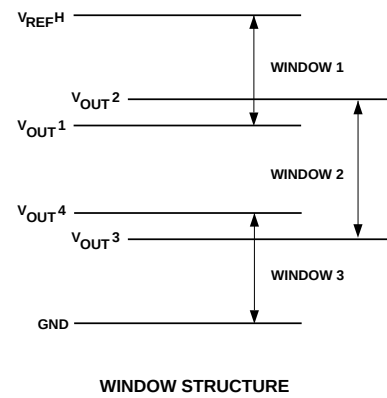
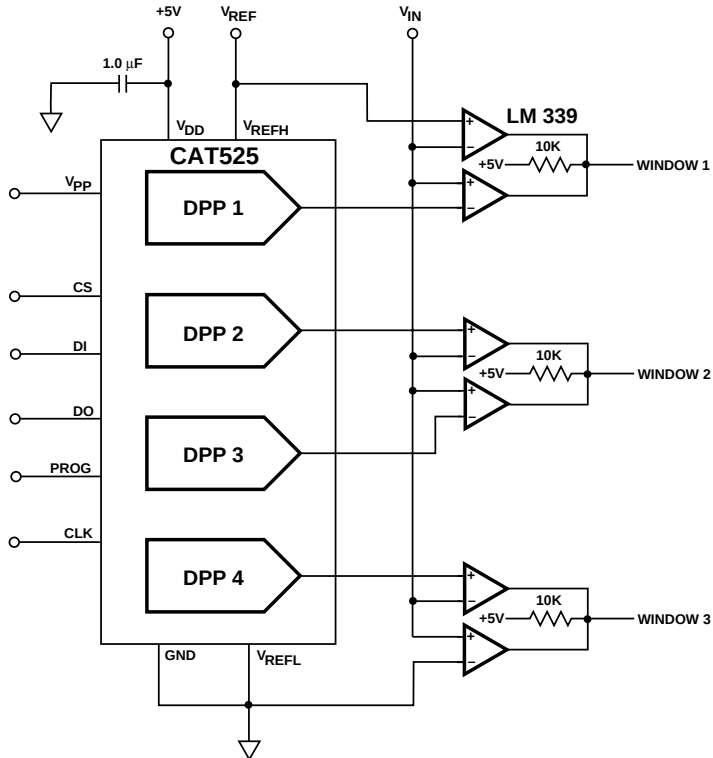


Digitally Controlled Voltage Reference

APPLICATION CIRCUITS (Cont.)

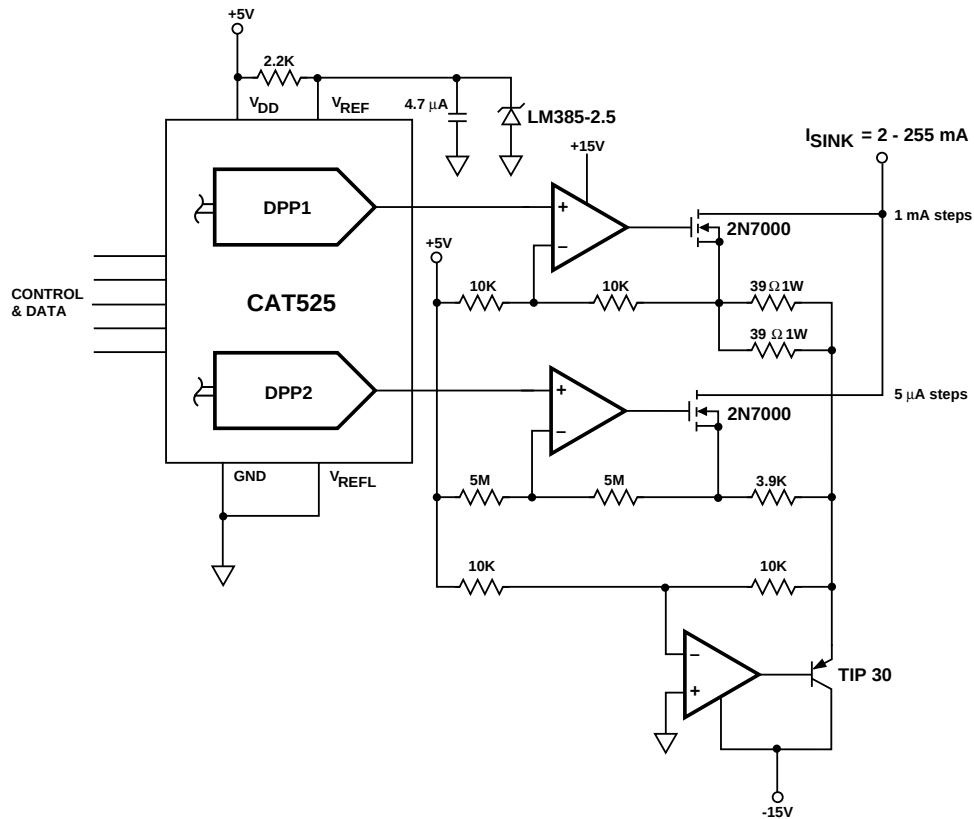


Staircase Window Comparator

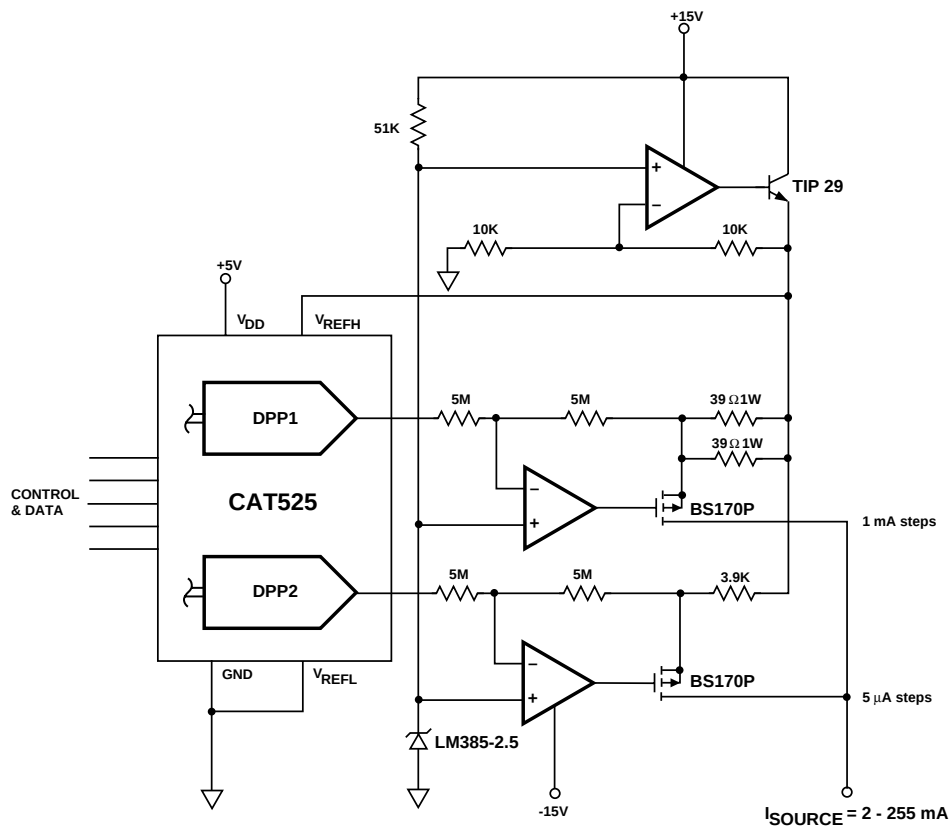


Overlapping Window Comparator

APPLICATION CIRCUITS (Cont.)

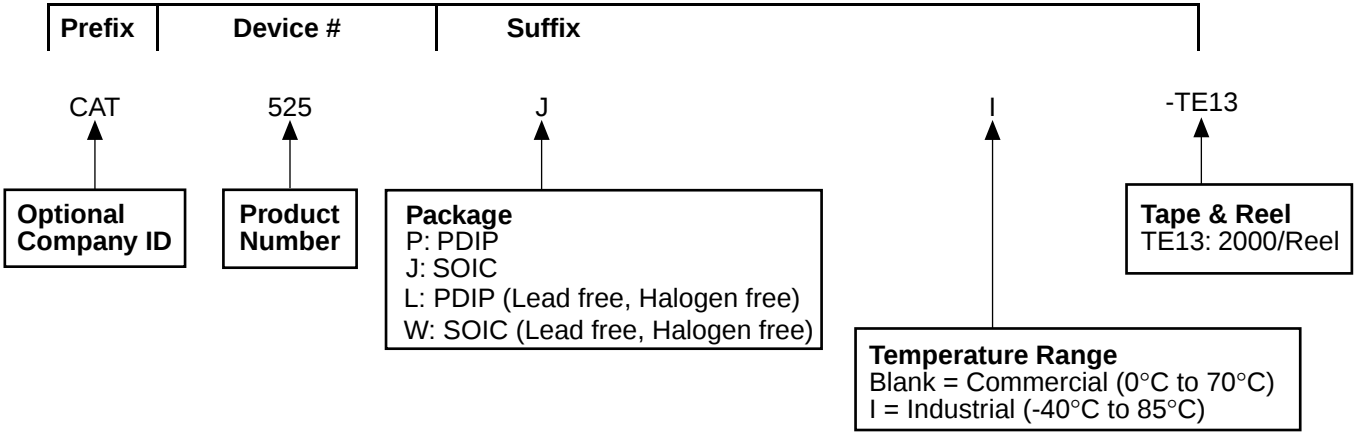


Current Sink with 4 Decades of Resolution



Current Source with 4 Decades of Resolution

ORDERING INFORMATION



Notes:
(1) The device used in the above example is a CAT525JI-TE13 (SOIC, Industrial Temperature, Tape & Reel)

REVISION HISTORY

Date	Rev.	Reason
3/16/2004	D	Updated Potentiometer Characteristics
7/12/2004	E	Updated Functional Diagram Updated Potentiometer Characteristics

Copyrights, Trademarks and Patents

Trademarks and registered trademarks of Catalyst Semiconductor include each of the following:

DPP TM AE² TM

Catalyst Semiconductor has been issued U.S. and foreign patents and has patent applications pending that protect its products. For a complete list of patents issued to Catalyst Semiconductor contact the Company's corporate office at 408.542.1000.

CATALYST SEMICONDUCTOR MAKES NO WARRANTY, REPRESENTATION OR GUARANTEE, EXPRESS OR IMPLIED, REGARDING THE SUITABILITY OF ITS PRODUCTS FOR ANY PARTICULAR PURPOSE, NOR THAT THE USE OF ITS PRODUCTS WILL NOT INFRINGE ITS INTELLECTUAL PROPERTY RIGHTS OR THE RIGHTS OF THIRD PARTIES WITH RESPECT TO ANY PARTICULAR USE OR APPLICATION AND SPECIFICALLY DISCLAIMS ANY AND ALL LIABILITY ARISING OUT OF ANY SUCH USE OR APPLICATION, INCLUDING BUT NOT LIMITED TO, CONSEQUENTIAL OR INCIDENTAL DAMAGES.

Catalyst Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Catalyst Semiconductor product could create a situation where personal injury or death may occur.

Catalyst Semiconductor reserves the right to make changes to or discontinue any product or service described herein without notice. Products with data sheets labeled "Advance Information" or "Preliminary" and other products described herein may not be in production or offered for sale.

Catalyst Semiconductor advises customers to obtain the current version of the relevant product information before placing orders. Circuit diagrams illustrate typical semiconductor applications and may not be complete.



CATALYST

Catalyst Semiconductor, Inc.
Corporate Headquarters
1250 Borregas Avenue
Sunnyvale, CA 94089
Phone: 408.542.1000
Fax: 408.542.1200
www.catsemi.com

Publication #: 2001
Revision: E
Issue Date: 7/12/04
Type: Final