

Accutek Microcircuit Corporation

AK49256S / AK49256G 262,144 Word by 9 Bit MOS Dynamic Random Access Memory

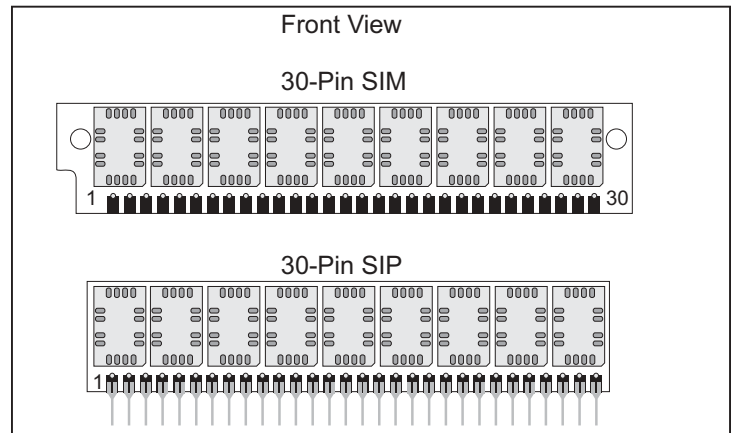
DESCRIPTION

The Accutek AK49256 high density memory modules is a random access memory organized in 256K x 9 bit words. The assembly consists of nine standard 256K x 1 DRAMs in plastic leaded chip carriers (PLCC) mounted on the front side of a printed circuit board. The module can be configured as a leadless 30 pad SIM or a leaded 30 pin SIP. This packaging approach provides a 6 to 1 density increase over standard DIP packaging.

The operation of the AK49256 is identical to nine 256K x 1 DRAMs. For the lower eight bits data input is tied to the data output and brought out separately for each device, with common RAS and CAS control. This common I/O feature dictates the use of early-write cycles to prevent contention of D and Q. Since the Write-Enable (\overline{WE}) signal must always go low before \overline{CAS} in a write cycle, Read-Write and Read-Modify-Write operation is not possible. For the ninth bit, the data input (D_9) and the data output (Q_9) pins are brought out separately and controlled by a separate PCAS for that bit. Bit nine is generally used for parity.

FEATURES

- 262,144 by 9 bit organization
- Optional 30 Pad leadless SIM (Single In-Line Module) or 30 Pin leaded SIP (Single In-Line Package)
- JEDEC standard pinout
- Common \overline{CAS} and \overline{RAS} control for the lower eight bits
- Separate PCAS control for D_9 and Q_9
- 3.15 Watt active and 205 mW standby (max)
- Operating free air temperature 0°C to 70°C
- Upward compatible with AK491024, AK591024, AK594096 and AK5916384
- Functionally and Pin compatible with AK59256A



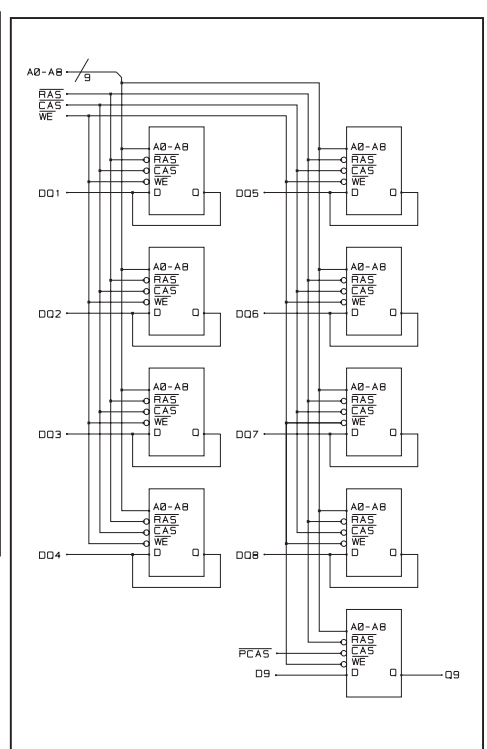
PIN NOMENCLATURE

| | |
|-----------------------------------|-----------------------|
| A ₀ - A ₈ | Address Inputs |
| DQ ₁ - DQ ₈ | Data In / Data Out |
| D ₉ | Data In 9 |
| Q ₉ | Data Out 9 |
| \overline{CAS} , PCAS | Column Address Strobe |
| \overline{RAS} | Row Address Strobe |
| \overline{WE} | Write Enable |
| V _{cc} | 5v Supply |
| V _{ss} | Ground |
| NC | No Connect |

PIN ASSIGNMENT

| PIN # | SYMBOL | PIN # | SYMBOL |
|-------|------------------|-------|------------------|
| 1 | V _{cc} | 16 | DQ ₅ |
| 2 | \overline{CAS} | 17 | A ₈ |
| 3 | DQ ₁ | 18 | NC |
| 4 | A ₀ | 19 | NC |
| 5 | A ₁ | 20 | DQ ₆ |
| 6 | DQ ₂ | 21 | \overline{WE} |
| 7 | A ₂ | 22 | V _{ss} |
| 8 | A ₃ | 23 | DQ ₇ |
| 9 | V _{ss} | 24 | NC |
| 10 | DQ ₃ | 25 | DQ ₈ |
| 11 | A ₄ | 26 | Q ₉ |
| 12 | A ₅ | 27 | \overline{RAS} |
| 13 | DQ ₄ | 28 | PCAS |
| 14 | A ₆ | 29 | D ₉ |
| 15 | A ₇ | 30 | V _{cc} |

FUNCTIONAL DIAGRAM



MODULE OPTIONS

| |
|------------------------|
| Leadless SIM: AK49256S |
| Leaded SIP: AK49256G |
| |

ORDERING INFORMATION

PART NUMBER CODING INTERPRETATION

| Position | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|--|---|---|---|------------|---|---|---|
| 1 Product | | | | | | | | |
| | AK = Accuthek Memory | | | | | | | |
| 2 Type | | | | | | | | |
| | 4 = Dynamic RAM 5 = CMOS Dynamic RAM 6 = Static RAM | | | | | | | |
| 3 Organization/Word Width | | | | | | | | |
| | 1 = by 1 16 = by 16 4 = by 4 32 = by 32 8 = by 8 36 = by 36 9 = by 9 | | | | | | | |
| 4 Size/Bits Depth | | | | | | | | |
| | 64 = 64K 4096 = 4 MEG 256 = 256K 8192 = 8 MEG 1024 = 1 MEG 16384 = 16 MEG | | | | | | | |
| 5 Package Type | | | | | | | | |
| | G = Single In-Line Package (SIP) S = Single In-Line Module (SIM) D = Dual In-Line Package (DIP) W = .050 inch Pitch Edge Connect Z = Zig-Zag In-Line Package (ZIP) | | | | | | | |
| 6 Special Designation | | | | | | | | |
| | P = Page Mode N = Nibble Mode K = Static Column Mode W = Write Per Bit Mode V = Video Ram | | | | | | | |
| 7 Separator | | | | | | | | |
| | - = Commercial 0°C to +70°C M = Military Equivalent Screened (-55°C to +125°C) I = Industrial Temperature Tested (-45°C to +85°C) X = Burned In | | | | | | | |
| 8 Speed (first two significant digits) | | | | | | | | |
| | DRAMS | | | | SRAMS | | | |
| | 50 = 50 nS | | | | 8 = 8 nS | | | |
| | 60 = 60 nS | | | | 10 = 10 nS | | | |
| | 70 = 70 nS | | | | 12 = 12 nS | | | |
| | 80 = 80 nS | | | | 15 = 15 nS | | | |

The numbers and coding on this page do not include all variations available but are show as examples of the most widely used variations. Contact Accuthek if other information is required.

EXAMPLES:

AK49256SP-10

256K x 9, 100 nSEC DRAM 30 pin SIM Configuration, Page Mode

AK49256GK-80

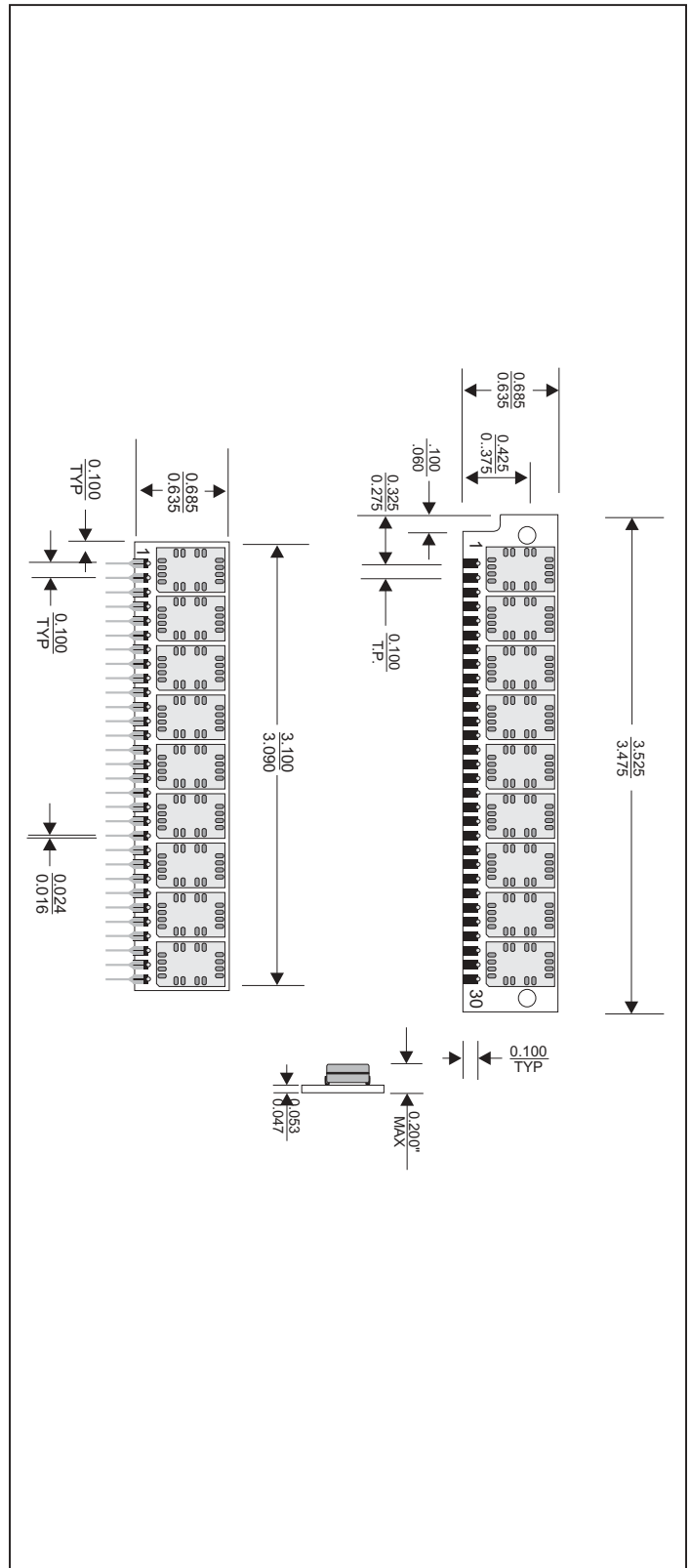
256K x 9, 80 nSEC DRAM 30 pin SIP Configuration, Static Column Mode



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MECHANICAL DIMENSIONS

Inches



Accuthek reserves the right to make changes in specifications at any time and without notice. Accuthek does not assume any responsibility for the use of any circuitry described; no circuit patent licenses are implied. Preliminary data sheets contain minimum and maximum limits based upon design objectives, which are subject to change upon full characterization over the specific operating conditions.