HARRIS SEMICONDUCTOR

CDP68HC05J3

August 1997

8-Bit Microcontroller Series

Features

The following are some of the hardware and software highlights of the CDP68HC05J3 family of HCMOS Microcomputers.

HARDWARE FEATURES

- **HCMOS Technology**
- **8-Bit Architecture**
- **Power-Saving STOP, WAIT, and Data Retention Modes**
- **Fully Static Operation**
- **On-Chip Memory**
  - **2,352 bytes of ROM**
  - **128 bytes of RAM**
- **12 Bidirectional I/O Lines**
  - **8 Software Programmable as Open Drain**
  - **4 Interruptible Inputs**
- **Internal 16-Bit Timer**
  - **Output Compare**
  - **Input Capture**
  - **Separate Timer Oscillator Allows:**
    - **Timing During Power Saving Mode**
    - **Counting of External Events**
- **Self-Check Mode**
- **External, Timer, and Port B Interrupts**
- **Master Reset and Power-On Reset**
- **On-Chip Oscillator with RC or Crystal Mask Options**
- **CDP68HC05J3**
  - **4.2MHz Operating Frequency (2.1MHz Internal Bus Frequency) at 5V; 2.0MHz at 3.0V**
  - **Single 3.0V to 8.0V Supply (2.0V Data Retention)**
- **CDP68HCL05J3**
  - **Lower Supply Current, I_{DD} in RUN, WAIT and STOP Modes at 5.5V, 3.6V and 2.4V**
  - **Single 2.4V to 6.0V Supply (2V Data Retention)**
- **CDP68HSC05J3**
  - **8.0MHz Operating Frequency (4.0MHZ Internal Bus Frequency)**
  - **Single 3.0V to 6.0V Supply (2.0V Data Retention)**

SOFTWARE FEATURES

- **Supports Full CDP68HC05 Instruction Set**
- **8 x 8 Unsigned Multiply Instruction**
- **True Bit-Manipulation**
- **Two Power Saving Standby Modes**
- **Efficient Use of Program Space**
- **Memory Mapped I/O**

Description

The CDP68HC05J3 HCMOS Microcomputer is a member of the CDP68HC05 family of single chip microcomputers. This 8-bit microcomputer unit (MCU) contains a CPU, 128 bytes of RAM, 2,352 bytes of masked ROM, a flexible 16-bit timer with input capture and output compare features, 12 bidirectional I/O lines (eight programmable as open drain outputs and four programmable as interruptible inputs), an on-chip oscillator, and an optional, independent oscillator for the 16-bit timer. The fully static design allows operation at frequencies down to DC, further reducing the already low, power consumption.

The timer can be used for pulse width measurements, timing, or event counting. Optionally, the timer can run off an oscillator that is independent of (and typically at a lower frequency than) the CPU oscillator. The dedicated timer oscillator allows timekeeping functions to be maintained during the low power STOP mode.

In conjunction with the open drain outputs, the four interruptible Port B lines can be used for switch scanning.

The interruptible port lines provide additional interrupts and can be used to exit the power down modes.

The CDP68HCL05J3 MCU device is a low-power version of the CDP68HC05J3 with lower power consumption in the RUN, WAIT, and STOP modes; and low voltage operation down to 2.4V.

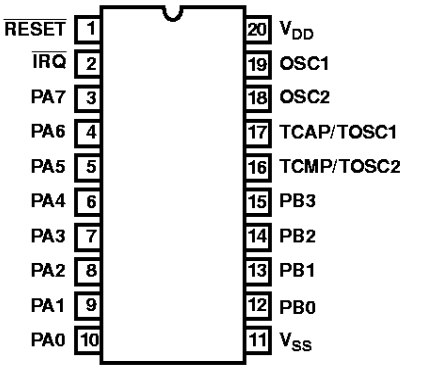
The CDP68HSC05J3 MCU device is a high-speed version of the CDP68HC05J3 with up to 8.0MHz operation.

The CDP68HC05J3 family supports the full CDP68HC05 instruction set. Development can be performed with tools supplied by Harris or offered by numerous third party vendors. Available tools include assemblers, C compilers, and ICE systems.

The CDP68HC05J3 is supplied in a 20 lead dual-in-line plastic package (E suffix) and in a 20 lead small outline plastic package (M suffix).

Pinout

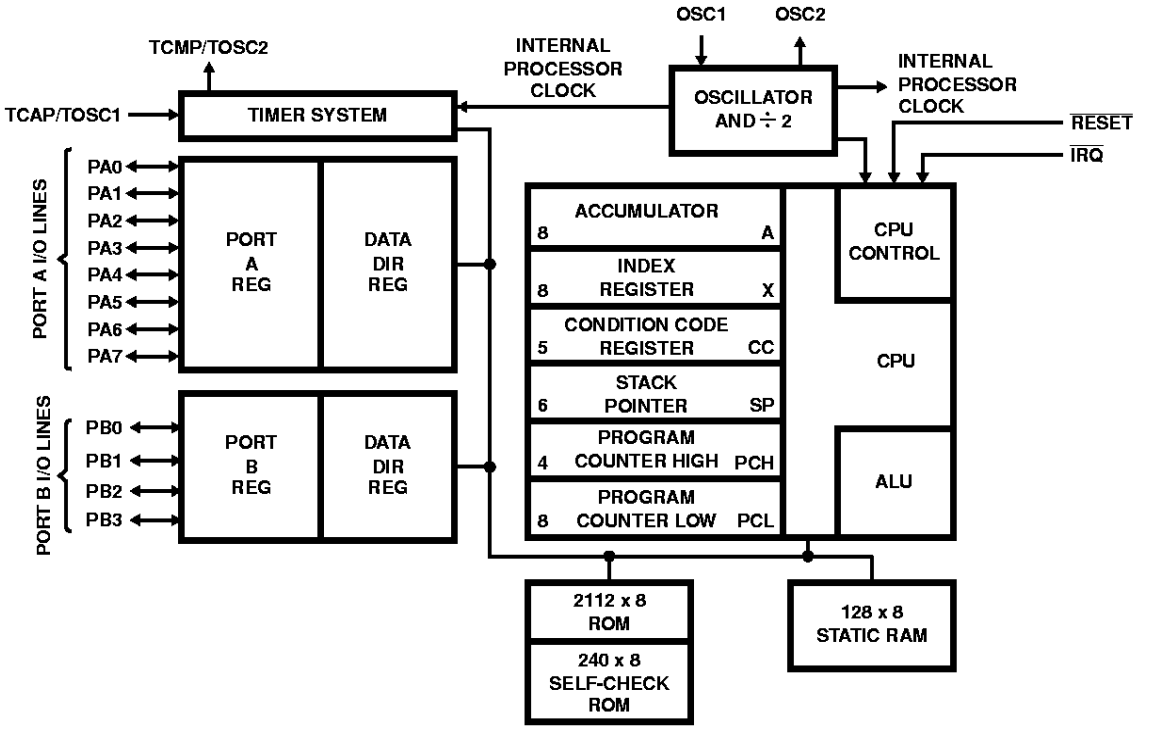
CDP68HC05J3 (SOIC, PDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2757.2**

Block Diagram



Power Considerations

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad \text{(EQ. 1)}$$

Where: T_A = Ambient Temperature, °C
θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W
$P_D = P_{INT} + P_{I/O}$
$P_{INT} = I_{CC} \times V_{CC}$, Watts - Chip Internal Power
$P_{I/O}$ = Power Dissipation on Input and Output Pins - User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

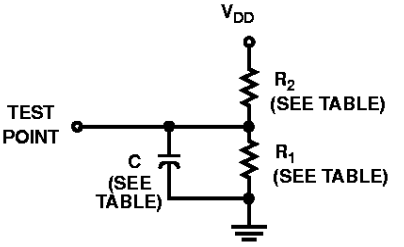
$$P_D = K \div (T_J + 273°C) \quad \text{(EQ. 2)}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D 2 \quad \text{(EQ. 3)}$$

Where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

PINS	R1	R2	C
V_{DD} = 4.5V: PA0-7, PB0-3	3.26Ω	2.38Ω	50pF
V_{DD} = 3.0V: PA0-7, PB0-3	10.19Ω	6.32Ω	50pF



EQUIVALENT TEST LOAD

Absolute Maximum Ratings

Supply Voltage (V_{DD}) . . . . . -0.5V to +7.0V
Input Voltage (V_{IN}) . . . . . V_{SS} -0.3V to V_{DD} +0.3V
Self-Check Mode (V_{IN})
$\overline{IRQ}$ Pin Only . . . . . V_{SS} -0.3V to 2 x V_{DD} +0.3V
Current Drain Per Pin (I)
Excluding V_{DD} and V_{SS} 25mA
Storage Temperature Range (T_{STG}) . . . . . -65°C to +150°C

Thermal Information

Thermal Resistance θ_{JA}
Plastic DIP Package . . . . . 60°C/W
Plastic SOIC Package . . . . . 75°C/W
Junction Temperature . . . . . +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range (T_A) . . . . . -40°C to +125°C
Low Power . . . . . 0°C to +70°C
High Speed . . . . . 0°C to +70°C

Input High Voltage . . . . . ($0.8 \cdot V_{DD}$) to V_{DD}

DC Electrical Specifications

V_{DD} = 5V ±10%, V_{SS} = 0V, T_A = -40°C to +125°C, Unless Otherwise Specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	V_{OL}	I_{LOAD} <10µA	-	-	0.1	V
	V_{OH}		V_{DD} -0.1	-	-	V
Output High Voltage: PA0-7, PB0-3, TCMP	V_{OH}	I_{LOAD} = -0.8mA	V_{DD} -0.8	-	-	V
Output Low Voltage: PA0-7, PB0-3, TCMP	V_{OL}	I_{LOAD} = 1.6mA	-	-	0.4	V
Input High Voltage: PA0-7, PB0-3, OSC1, TCAP/ TOSC1	V_{IH}		-	$0.5 \cdot V_{DD}$	$0.7 \cdot V_{DD}$	V
Input High Voltage: $\overline{RESET}$, $\overline{IRQ}$	V_{IH}		-	$0.5 \cdot V_{DD}$	3.5	V
Input Low Voltage: PA0-7, PB0-3, OSC1, TCAP/ TOSC1	V_{IL}		$0.3 \cdot V_{DD}$	$0.5 \cdot V_{DD}$	-	V
Input Low Voltage: $\overline{RESET}$, $\overline{IRQ}$	V_{IL}		0.8	$0.3 \cdot V_{DD}$	-	V
Input Hysteresis Voltage: $\overline{RESET}$, $\overline{IRQ}$	V_{HYS}		0.5	1.0	-	V
Data Retention Voltage	VRM	0°C to +70°C	2	-	-	V
Supply Current (Notes 1, 2)						
RUN	I_{RUN}		-	2.0	4.0	mA
WAIT	I_{WAIT}		-	0.8	1.6	mA
STOP	I_{STOP}	T_A = -40°C to +125°C	-	20	40	µA
I/O Ports Hi-Z Leakage Current: PA0-7, PB0-3	I_{IL}		-	-	±10	µA
Input Current: $\overline{RESET}$, $\overline{IRQ}$, TCAP/TOSC1, OSC1	I_{IN}		-	-	±1	µA
Capacitance: (Note 2)	C_{OUT}		-	-	12	pF
$\overline{RESET}$, $\overline{IRQ}$, TCAP/TOSC1, OSC1, PA0-7, PB0-3	C_{IN}		-	-	8	pF

NOTES:

1. This device contains circuitry to protect the inputs against damage due to high static voltages of electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to the range $V_{SS} < (V_{IN}$ or $V_{OUT}) < V_{DD}$. Reliability of operation is enhanced if unused inputs except OSC2 are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).
2. Includes Ports used as Input/Output Pins, Ports used as Input only Pins; Ports used as Output only Pins.

DC Electrical Specifications

V_{DD} = 3.3V_{DC} ±10%, V_{SS} = 0V_{DC}, T_A = -40°C to +125°C, Unless Otherwise Specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	V_{OL}	I_{LOAD} <10µA	-	-	0.1	V
	V_{OH}		V_{DD} -0.1	-	-	V
Output High Voltage: PA0-7, PB0-3, TCMP	V_{OH}	I_{LOAD} = -0.2mA	V_{DD} -0.3	-	-	V
Output Low Voltage: PA0-7, PB0-3, TCMP	V_{OL}	I_{LOAD} = 0.4mA	-	-	0.3	V
Input High Voltage: PA0-7, PB0-3, OSC1, TCAP/ TOSC1	V_{IH}		-	0.5•V_{DD}	0.7•V_{DD}	V
Input High Voltage: $\overline{RESET}$, $\overline{IRQ}$	V_{IH}		-	0.5•V_{DD}	2.5	V
Input Low Voltage: PA0-7, PB0-3, OSC1, TCAP/ TOSC1	V_{IL}		0.2•V_{DD}	0.5•V_{DD}	-	V
Input Low Voltage: $\overline{RESET}$, $\overline{IRQ}$	V_{IL}		0.5	0.3•V_{DD}	-	V
Input Hysteresis Voltage: $\overline{RESET}$, $\overline{IRQ}$	V_{HYS}		0.3	0.6	-	V
Data Retention Voltage	V_{RM}	0°C to +70°C	2	-	-	V
Supply Current (Notes 1, 2)						
RUN	I_{RUN}		-	1.2	2.4	mA
WAIT	I_{WAIT}		-	0.5	1.0	mA
STOP	I_{STOP}	T_A = -40°C to +125°C	-	10	20	µA
I/O Ports Hi-Z Leakage Current: PA0-7, PB0-3	I_{IL}		-	-	±10	µA
Input Current: $\overline{RESET}$, $\overline{IRQ}$, TCAP/TOSC1, OSC1	I_{IN}		-	-	±1	µA
Capacitance: (Note 2)	C_{OUT}		-	-	12	pF
$\overline{RESET}$, $\overline{IRQ}$, TCAP/TOSC1, OSC1, PA0-7, PB0-3	C_{IN}		-	-	8	pF

NOTES:

1. This device contains circuitry to protect the inputs against damage due to high static voltages of electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to the range V_{SS} < (V_{IN} or V_{OUT}) < V_{DD}. Reliability of operation is enhanced if unused inputs except OSC2 are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).
2. Includes Ports used as Input/Output Pins, Ports used as Input only Pins; Ports used as Output only Pins.

Control Timing

V_{DD} = 5V ±10%, V_{SS} = 0V, T_A = -40°C to +125°C

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Of Operation						
Crystal Option	f_{OSC}		-	-	4.2	MHz
External Clock Option	f_{OSC}		DC	-	4.2	MHz
Internal Operating Frequency						
Crystal (f_{OSC} + 2)	f_{OP}		-	-	2.1	MHz
External Clock (f_{OSC} + 2)	f_{OP}		DC	-	2.1	MHz
Cycle Time	t_{CYC}		480	-	-	ns
Crystal Oscillator Start-Up Time for AT-Cut Crystal	t_{OXOV}		-	-	100	ms

Control Timing V_{DD} = 5V ±10%, V_{SS} = 0V, T_A = -40°C to +125°C **(Continued)**

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Stop Recovery Start-Up Time (AT-Cut Crystal Oscillator)	t_{ILCH}		-	-	100	ms
$\overline{RESET}$ Pulse Width	t_{RL}		1.5	-	-	t_{CYC}
Timer						
Resolution (Note 1)	t_{RES}		4.0	-	-	t_{CYC}
Input Capture Pulse Width	t_{TH}, t_{TL}		125	-	-	ns
Input Capture Pulse Period	t_{TLTL}		(Note 2)	-	-	t_{CYC}
Interrupt Pulse Width Low (Edge-Triggered)	t_{ILIH}		125	-	-	ns
Interrupt Pulse Period	t_{ILIH}		(Note 3)	-	-	t_{CYC}
OSC1 Pulse Width	t_{OH}, t_{OL}		90	-	-	ns

NOTES:

1. Since a 2-bit prescaler in the timer must count four internal cycles (t_{CYC}), this is the limiting minimum factor in determining the timer resolution.
2. The minimum period t_{TLTL} should not be less than the number of cycle times it takes to execute the capture interrupt service routine plus 24 t_{CYC}.
3. The minimum period t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 t_{CYC}.

Control Timing V_{DD} = 3.3V ±10%, V_{SS} = 0V, T_A = -40°C to +125°C

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Of Operation						
Crystal Option	f_{OSC}		-	-	2.0	MHz
External Clock Option	f_{OSC}		DC	-	2.0	MHz
Internal Operating Frequency						
Crystal (f_{OSC} + 2)	f_{OP}		-	-	1.0	MHz
External Clock (f_{OSC} + 2)	f_{OP}		DC	-	1.0	MHz
Cycle Time	t_{CYC}		1000	-	-	ns
Crystal Oscillator Start-up Time for AT-cut Crystal	t_{OXOV}		-	-	100	ms
Stop Recovery Start-up Time (AT-cut Crystal Oscillator)	t_{ILCH}		-	-	100	ms
$\overline{RESET}$ Pulse Width	t_{RL}		1.5	-	-	t_{CYC}
Timer						
Resolution (Note 1)	t_{RES}		4.0	-	-	t_{CYC}
Input Capture Pulse Width	t_{TH}, t_{TL}		250	-	-	ns
Input Capture Pulse Period	t_{TLTL}		(Note 2)	-	-	t_{CYC}
Interrupt Pulse Width Low (Edge-Triggered)	t_{ILIH}		250	-	-	ns
Interrupt Pulse Period	t_{ILIH}		(Note 3)	-	-	t_{CYC}
OSC1 Pulse Width	t_{OH}, t_{OL}		200	-	-	ns

NOTES:

1. Since a 2-bit prescaler in the timer must count four internal cycles (t_{CYC}), this is the limiting minimum factor in determining the timer resolution.
2. The minimum period t_{TLTL} should not be less than the number of cycle times it takes to execute the capture interrupt service routine plus 24 t_{CYC}.
3. The minimum period t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 t_{CYC}.