

32-Channel Serial To Parallel Converter With Push-Pull Outputs

Ordering Information

Device	Package Options			
	44 J-Lead Quad Ceramic Chip Carrier	44 J-Lead Quad Plastic Chip Carrier	Die in waffle pack	44 J-Lead Quad Ceramic Chip Carrier (MIL-STD-883 Processed*)
HV57	HV5708DJ	HV5708PJ	HV5708X	RBHV5708DJ
HV58	HV5808DJ	HV5808PJ	HV5808X	RBHV5808DJ

* For Hi-Rel process flows, refer to page 5-3 of the Databook.

Features

- Processed with HVCMOS[®] technology
- Output voltages up to 80V
- Low power level shifting
- Source/sink current minimum 20mA
- Shift register speed 8MHz
- Latched data outputs
- Forward and reverse shifting options
- Diode to V_{PP} allows efficient power recovery
- CMOS compatible inputs

Absolute Maximum Ratings¹

Supply voltage, V _{DD} ²	-0.5V to +15V	
Output voltage, V _{PP} ²	-0.5V to +80V	
Logic input levels ²	-0.5V to V _{DD} +0.5V	
Ground current ³	1.5A	
Continuous total power dissipation ⁴	Ceramic	1500mW
	Plastic	1200mW
Operating temperature range	Commercial	-40°C to +85°C
	Military	-55°C to +125°C
Storage temperature range	-65°C to +150°C	
Lead temperature 1.6mm (1/16 inch) from case for 10 seconds	260°C	

Notes:

1. Device will survive (but operation may not be specified or guaranteed) at these extremes.
2. All voltages are referenced to GND.
3. Duty cycle is limited by the total power dissipated in the package.
4. For operation above 25°C ambient, derate linearly to 70°C at 12mW/°C.

General Description

The HV57 and HV58 are low-voltage serial to high-voltage parallel converters with push-pull outputs. These devices have been designed for use as drivers for AC-electroluminescent displays. They can also be used in any application requiring multiple output high-voltage current sourcing and sinking capabilities such as driving plasma panels, vacuum fluorescent displays, or large matrix LCD displays. The inputs are fully CMOS compatible.

These devices consist of a 32-bit shift register, 32 latches, and control logic to perform the polarity select and blanking of the outputs. HV_{OUT1} is connected to the first stage of the shift register through the polarity and blanking logic. Data is shifted through the shift register on the logic low to high transition of the clock. The HV57 shifts data in the clockwise direction when viewed from the top of the package and the HV58 shifts in the counter-clockwise direction. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register (HV_{OUT32}). Operation of the shift register is not affected by the LE (latch enable), BL (blanking), or the POL (polarity) inputs. Transfer of data from the shift register to the latch occurs when the LE (latch enable) input is high. The data in the latch is stored when LE is low.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
I_{DD}	V_{DD} supply current		15	mA	$V_{DD} = V_{DD\ max}$ $f_{CLK} = 8\text{MHz}$
I_{PP}	High voltage supply current		0.5	mA	Outputs high
			0.5	mA	Outputs low
I_{DDQ}	Quiescent V_{DD} supply current		100	μA	All $V_{IN} = V_{SS}$ or V_{DD}
V_{OH}	High-level output	HV _{OUT}	52	V	$I_O = -20\text{mA}(-15\text{mA}^*)$
		Data out	$V_{DD} - 1$	V	$I_O = -100\mu\text{A}$
V_{OL}	Low-level output	HV _{OUT}	8	V	$I_O = 20\text{mA}(15\text{mA}^*)$
		Data out	1	V	$I_O = 100\mu\text{A}$
I_{IH}	High-level logic input current		1	μA	$V_{IH} = V_{DD}$
I_{IL}	Low-level logic input current		-1	μA	$V_{IL} = 0\text{V}$

* Over Military temperature range

AC Characteristics ($V_{DD} = 12\text{V}$, $T_C = 25^\circ\text{C}$)

Symbol	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency		8	MHz	
t_W	Clock width high or low	62		ns	
t_{SU}	Data set-up time before clock rises	25		ns	
t_H	Data hold time after clock rises	10		ns	
t_{ON}, t_{OFF}	Time from latch enable to HV _{OUT}		500	ns	
t_{DHL}	Delay time clock to data high to low		100	ns	$C_L = 15\text{pF}$
t_{DLH}	Delay time clock to data low to high		100	ns	$C_L = 15\text{pF}$
t_{DLE}	Delay time clock to \overline{LE} low to high	50		ns	
t_{WLE}	Width of \overline{LE} pulse	50		ns	
t_{SLE}	\overline{LE} set-up time before clock rises	50		ns	

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units	
V_{DD}	Logic supply voltage	10.8	13.2	V	
V_{PP}	Output high voltage	8.0	75	V	
V_{IH}	High-level input voltage	$V_{DD} - 2\text{V}$	V_{DD}	V	
V_{IL}	Low-level input voltage	0	2.0	V	
f_{CLK}	Clock frequency		8.0	MHz	
T_A	Operating free-air temperature	Commercial	-40	+85	$^\circ\text{C}$
		Military Hi-Rel (RB)	-55	+125	$^\circ\text{C}$

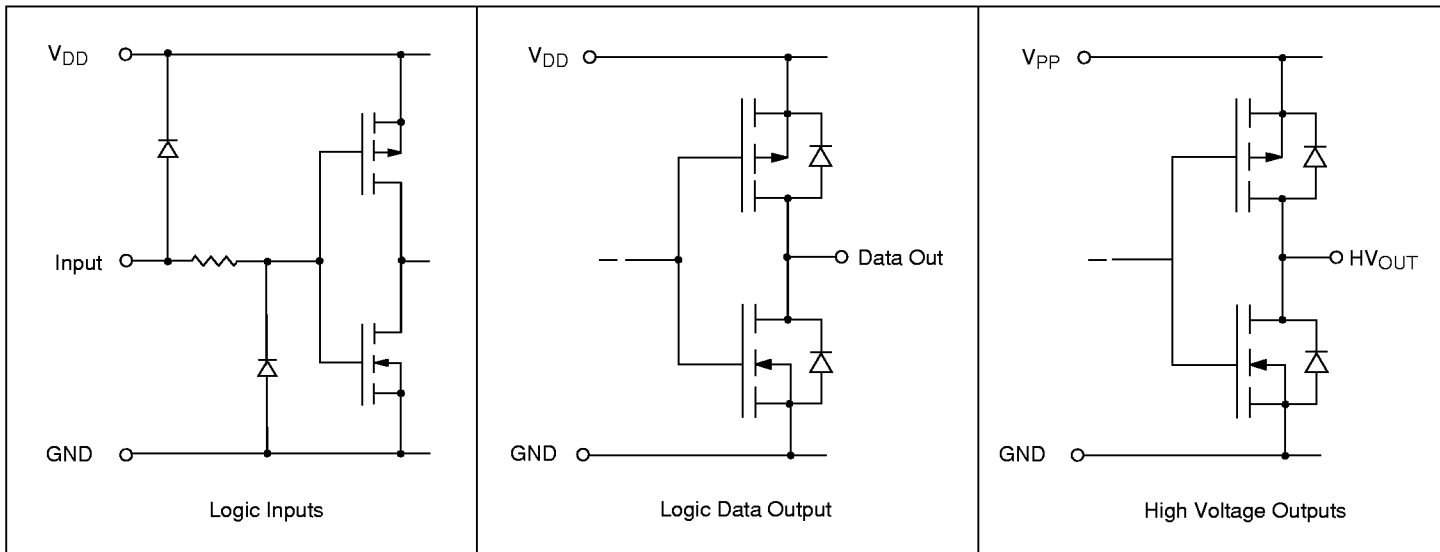
Note:

Power-up sequence should be the following:

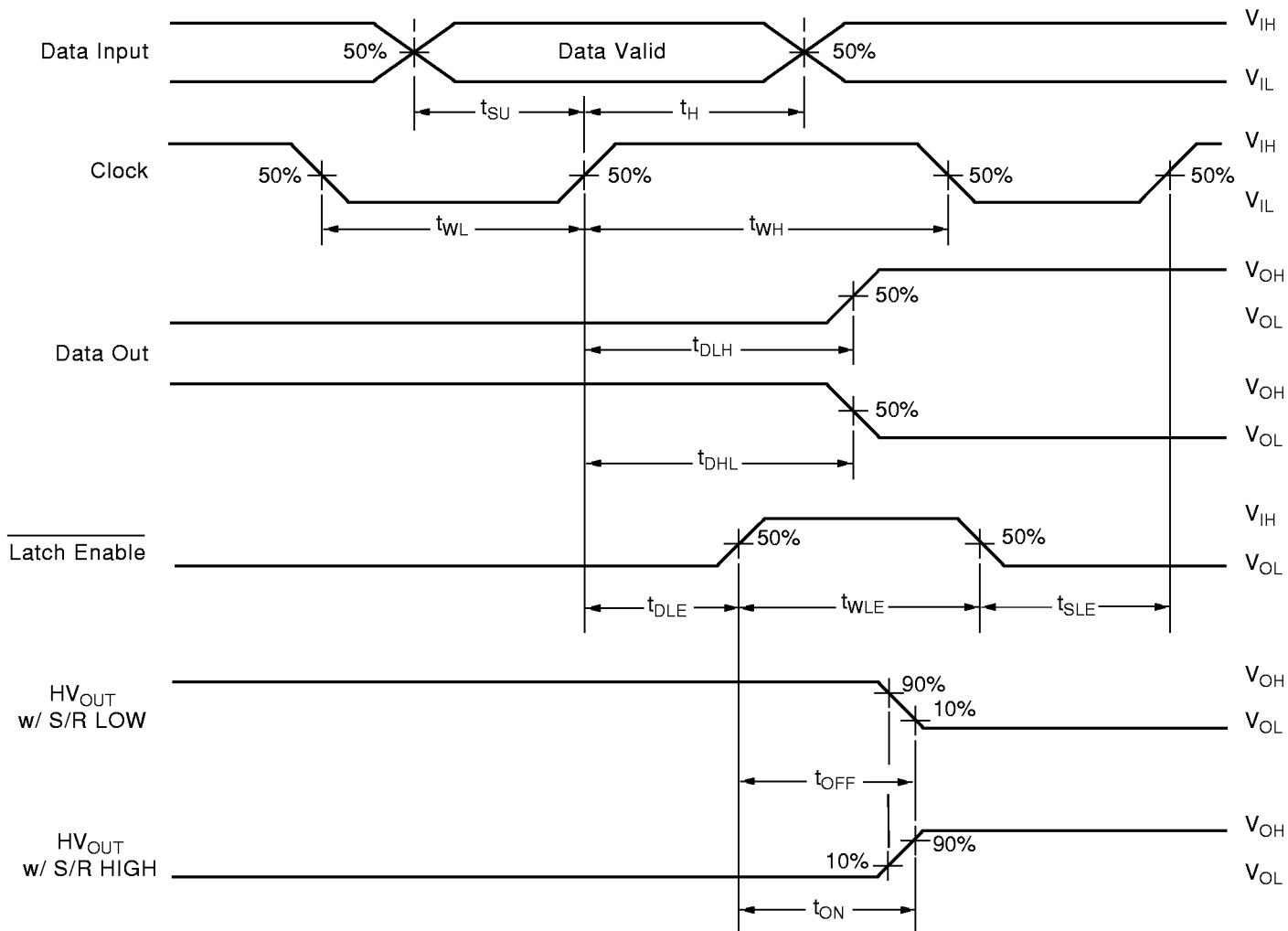
1. Connect ground.
2. Apply V_{DD} .
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply V_{PP} .

Power-down sequence should be the reverse of the above.

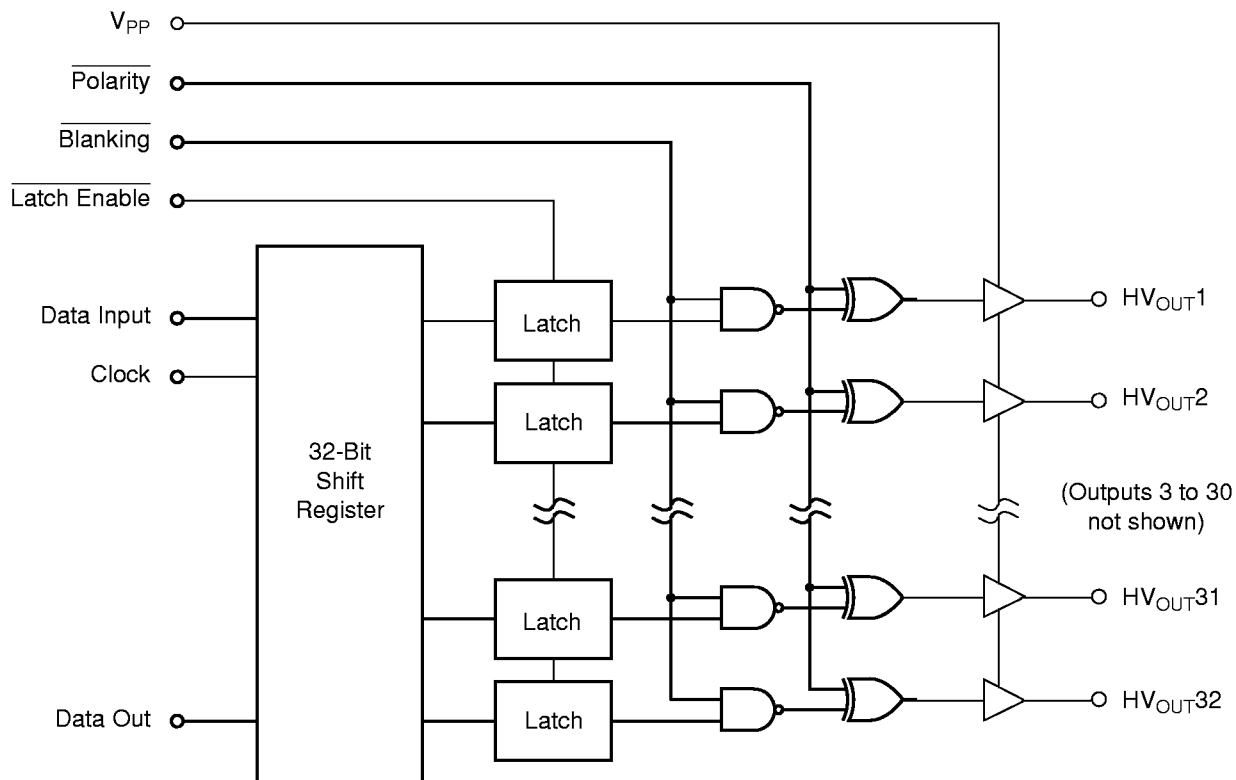
Input and Output Equivalent Circuits



Switching Waveforms



Functional Block Diagram



Function Table

Function	Inputs					Outputs				
	Data	CLK	\overline{LE}	\overline{BL}	\overline{POL}	Shift Reg 1 2...32	HV Outputs 1 2...32	Data Out *		
All on	X	X	X	L	L	* *...*	H H...H	*		
All off	X	X	X	L	H	* *...*	L L...L	*		
Invert mode	X	X	L	H	L	* *...*	$\overline{*} \overline{*} \dots \overline{*}$	*		
Load S/R	H or L	↑	L	H	H	H or L *...*	* *...*	*		
Load latches	X	H or L	↑	H	H	* *...*	* *...*	*		
	X	H or L	↑	H	L	* *...*	$\overline{*} \overline{*} \dots \overline{*}$	*		
Transparent latch mode	L	↑	H	H	H	L *...*	L *...*	*		
	H	↑	H	H	H	H *...*	H *...*	*		

Notes:
 H = high level, L = low level, X = irrelevant, ↑ = low-to-high transition.
 * = dependent on previous stage's state before the last CLK or last LE high,

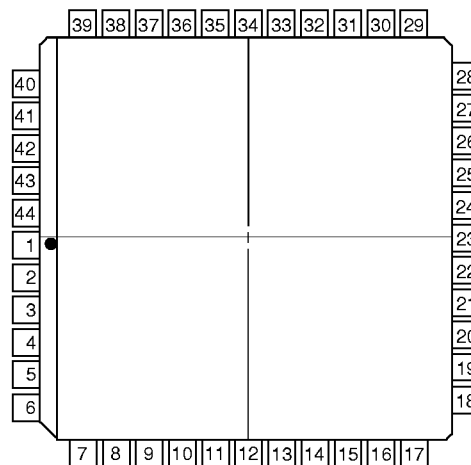
Pin Configurations

Package Outline

HV57

44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HV _{OUT} 17	23	GND
2	HV _{OUT} 16	24	V _{PP}
3	HV _{OUT} 15	25	V _{DD}
4	HV _{OUT} 14	26	Latch Enable
5	HV _{OUT} 13	27	Data In
6	HV _{OUT} 12	28	Blanking
7	HV _{OUT} 11	29	N/C
8	HV _{OUT} 10	30	HV _{OUT} 32
9	HV _{OUT} 9	31	HV _{OUT} 31
10	HV _{OUT} 8	32	HV _{OUT} 30
11	HV _{OUT} 7	33	HV _{OUT} 29
12	HV _{OUT} 6	34	HV _{OUT} 28
13	HV _{OUT} 5	35	HV _{OUT} 27
14	HV _{OUT} 4	36	HV _{OUT} 26
15	HV _{OUT} 3	37	HV _{OUT} 25
16	HV _{OUT} 2	38	HV _{OUT} 24
17	HV _{OUT} 1	39	HV _{OUT} 23
18	Data Out	40	HV _{OUT} 22
19	N/C	41	HV _{OUT} 21
20	N/C	42	HV _{OUT} 20
21	Polarity	43	HV _{OUT} 19
22	Clock	44	HV _{OUT} 18



top view
44-pin J-Lead Package

HV58

44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HV _{OUT} 16	23	GND
2	HV _{OUT} 17	24	V _{PP}
3	HV _{OUT} 18	25	V _{DD}
4	HV _{OUT} 19	26	Latch Enable
5	HV _{OUT} 20	27	Data In
6	HV _{OUT} 21	28	Blanking
7	HV _{OUT} 22	29	N/C
8	HV _{OUT} 23	30	HV _{OUT} 1
9	HV _{OUT} 24	31	HV _{OUT} 2
10	HV _{OUT} 25	32	HV _{OUT} 3
11	HV _{OUT} 26	33	HV _{OUT} 4
12	HV _{OUT} 27	34	HV _{OUT} 5
13	HV _{OUT} 28	35	HV _{OUT} 6
14	HV _{OUT} 29	36	HV _{OUT} 7
15	HV _{OUT} 30	37	HV _{OUT} 8
16	HV _{OUT} 31	38	HV _{OUT} 9
17	HV _{OUT} 32	39	HV _{OUT} 10
18	Data Out	40	HVout 11
19	N/C	41	HVout 12
20	N/C	42	HVout 13
21	Polarity	43	HVout 14
22	Clock	44	HVout 15