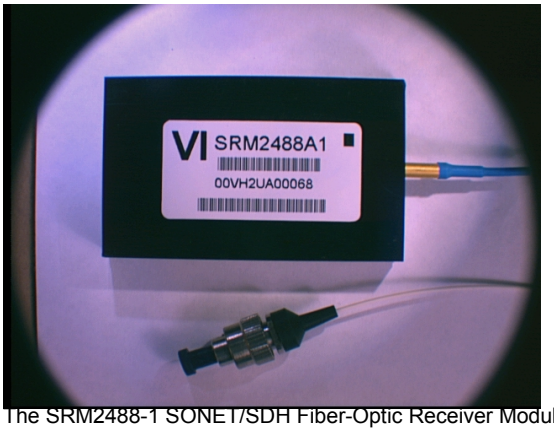
VECTRON INTERNATIONAL
A DOVER TECHNOLOGIES COMPANY

Preliminary Product Data Sheet

SRM2488-1

SONET/SDH Fiber-Optic Receiver Module with Clock and Data Recovery



The SRM2488-1 SONET/SDH Fiber-Optic Receiver Module

The product described herein is currently in development and samples are available. Target specifications contained in this data sheet reflect preliminary data and are subject to change without notice.

Features

- SONET OC-48 and SDH STM-16 Compatible
- Multi-Sourced 24Pin Footprint (1.00” leadspacing)
- -22dBm minimum sensitivity
- Differential Clock and Data Outputs
- +5/-5.2V Power Supply
- CMOS Link Status Flag
- Operation at 1300 nm and 1550 nm
- -5° to +75°C Case Operating Temperature
- Wide Dynamic Range

Applications

- Telecommunications
  - Medium Haul – OC48/STM16
  - Metropolitan area networks
- High-speed data communications

Description

VI’s SRM2488-1 is a fiber-optic receiver module with integrated clock and data recovery. It is powered by +5V/-5.2V power supplies and is housed in a multi-Sourced 24 pin DIL package (with 1.00” lead spacing). It is ideally suited for SONET OC-48, SDH STM-16 and other 2488 Mb/s fiber-optic transmission applications that demand superior performance. It is available with a single-mode fiber pigtail, with either an FC/PC or SC connector.

Functional Overview

This highly integrated module converts a 2488.32 Mb/s fiber-optic NRZ signal to differential data and clock outputs. A LOS flag alerts the user to a loss of signal condition when the optical input falls below an acceptable level.

The +5V/-5.2V supply provides power for the module's PiN-photodiode, preamplifier, data quantizer, and clock recovery circuits. All elements are integrated into fiber-coupled 1.4 inch by 2.3 inch, 24-pin industry common package for ease of integration (1.00" leadspacing).

The optical signal is coupled through a short length of singlemode optical fiber to a hermetic module which encases the PiN-photodiode and preamplifier. The PiN-photodiode converts the optical signal to an electrical current, which is then converted to a voltage and amplified by a low noise transimpedance preamplifier.

Further gain is provided by the data quantizer, which also detects LOS when the optical signal falls below an acceptable level. The quantized Data signal is input to a PLL-based Clock recovery circuit, which regenerates a system clock, then re-times and reshapes the Data signal. The regenerated Clock is provided as a low-jitter system Clock.

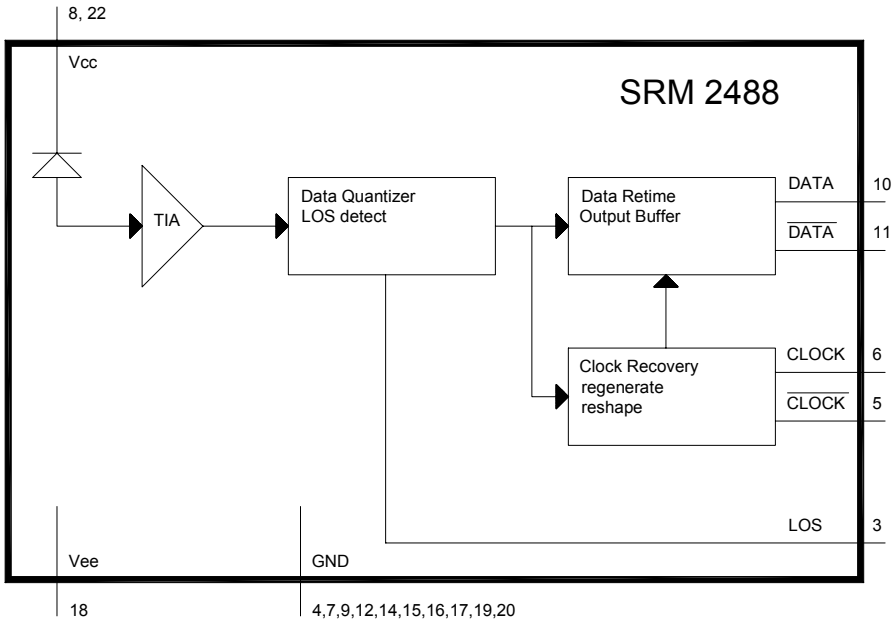


Figure 1. SRM2488-1 Functional Block Diagram

Pin Diagram

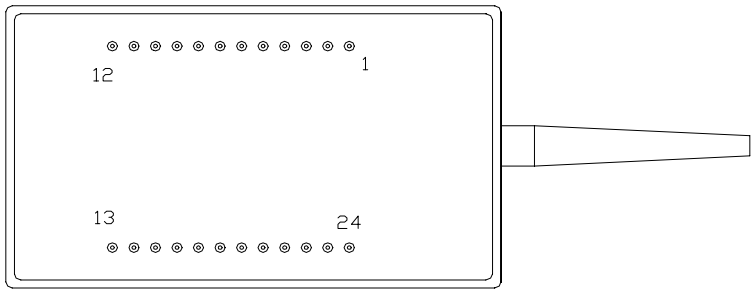


Figure 2. SRM2488-1 Pin Diagram (Top View)

Table 1. Pin Function

Pin	Symbol	Function
10	Data	Re-timed Data Output.
11	$\overline{\text{Data}}$	Complementary Re-timed Data Output.
6	Clock	Recovered Clock Output.
5	$\overline{\text{Clock}}$	Complementary Recovered Clock Output.
3	LOS	LOS Flag, CMOS high when LOS (Loss of signal)
8,22	V_{CC}	Positive Supply Voltage (+5.0V)
18	V_{EE}	Negative Supply Voltage (-5.2V)
4,7,9,12,14,15, 16,17,19,20	GND	Ground.
1,2,13,21,23,24	NC	No User Connection.

Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
Storage Case Temperature Range	T_S	-40	85	°C
Operating Case Temperature Range	T_o	-5	75	°C
Positive Supply Voltage	V_{CC}	0	+6	V
Negative Supply Voltage	V_{EE}	-6.0	0	V
Lead Soldering Conditions			250/10	°C/s

Absolute maximum ratings are provided here as worst case and short duration exposure conditions only. Exposure to conditions at or in excess of the Absolute Maximum Ratings may result in permanent damage. Functional operation of the device is not implied at these conditions.

Performance Characteristics

Table 3. Electrical Performance

Parameter	Symbol	Minimum	Typical	Maximum	Units
Input Signal Rate	f_O	2488.07	2488.32	2488.57	Mb/s
Operating Case Temperature	T_O	-5		+75	°C
Supply Voltage (Positive)	V_{CC}	4.5	5.0	5.5	V
	I_{CC}		100		mA
Supply Voltage (Negative)	V_{EE}	-5.46	-5.20	-4.94	V
	I_{EE}		350		mA
Power Consumption			2.3		W
Data and Clock Output Levels [1]					
Single-ended output		0.3		1.0	V
Differential output		0.6		2.0	V
Clock to Data Alignment [2]	T_{CDA}	-90	0	+90	ps
Data and Clock Output Rise and Fall Times [3]	t_R, t_F			500	ps
Output Clock Duty Cycle	Duty	45	50	55	%
LOS Received Power Level Flag	LOS				
Decreasing Optical Power			-26		dBm
Increasing Optical Power			-24		dBm
High Output Level		4.0	4.5	Vcc	V
Low Output Level		0.0	0.5	1.0	V
Jitter Generation				<0.01	UI RMS
Jitter Transfer		GR-253/ ITU-T G958			
Jitter Tolerance		GR-253/ ITU-T G958			

1. Measured with a load of R_L = 50Ω to GND. Outputs must be AC-coupled.
2. Alignment of clock and data outputs (see Figure 5.).
3 Measured at 20% to 80% levels.

Table 4. Optical Performance

Parameter	Symbol	Minimum	Typical	Maximum	Units
Average Sensitivity [1]	Sens.	-22.0			dBm
Optical Input Power[1]	P_{MAX}			-5.0	dBm
Input Wavelength	λ	1280		1580	nm

1. For a BER less than 1E-10. Measured using a 2^{23} - 1 pseudorandom word and a 50% average optical duty cycle and a 10 dB Extinction Ratio.

Qualification

The SRM2488-1 has been designed to comply with the intent of Bellcore specifications GR-468-CORE, Reliability Assurance for Opto-electronic devices and will be subject to a complete qualification test plan to demonstrate full compliance. All of the technologies used in the assembly of the module represent standard microelectronics and optical technologies that are used in similar products, and have extensive field reliability data.

While all components and technologies used in the optical receiver are backed by qualification data and should present no reliability risk, VI is presently qualifying the fully assembled module. The qualification plan will entail mechanical and environmental tests along with accelerated life tests. Typical tests, test conditions and sample size are listed below

Table 5. Qualification Plan

Parameter	Test Method	Sample Size
Physical Dimensions	MIL-STD-883, Method 2016	11
Mechanical Shock	MIL-STD-883, Method2002, Test B	11
Vibration, variable frequency	MIL-STD-883, Method 2007, Test A	11
Lead Solderability	MIL-STD-883, Method 2003	24 leads
Lead Integrity	MIL-STD-883, Method 2004	15 leads
Temperature Cycling	-40°C/85°C, 300 cycles	11
High Temperature Aging	85°C under bias, 2000 hours	11
Damp Bake	85°C/85% RH/1000 hours	11
Low Temperature Storage	-40°C, 168 hours	11
ESD	MIL-STD-883Method 3015	3
Destructive Bond Pull	MIL-STD-883Method 2011	40

Table 6. Optical Fiber Characteristics

Parameter	Minimum	Typical	Maximum	Units
Fiber Length		1000		mm
Fiber Core		8.3		µm
Fiber Buffer		900		µm

Outline Diagram

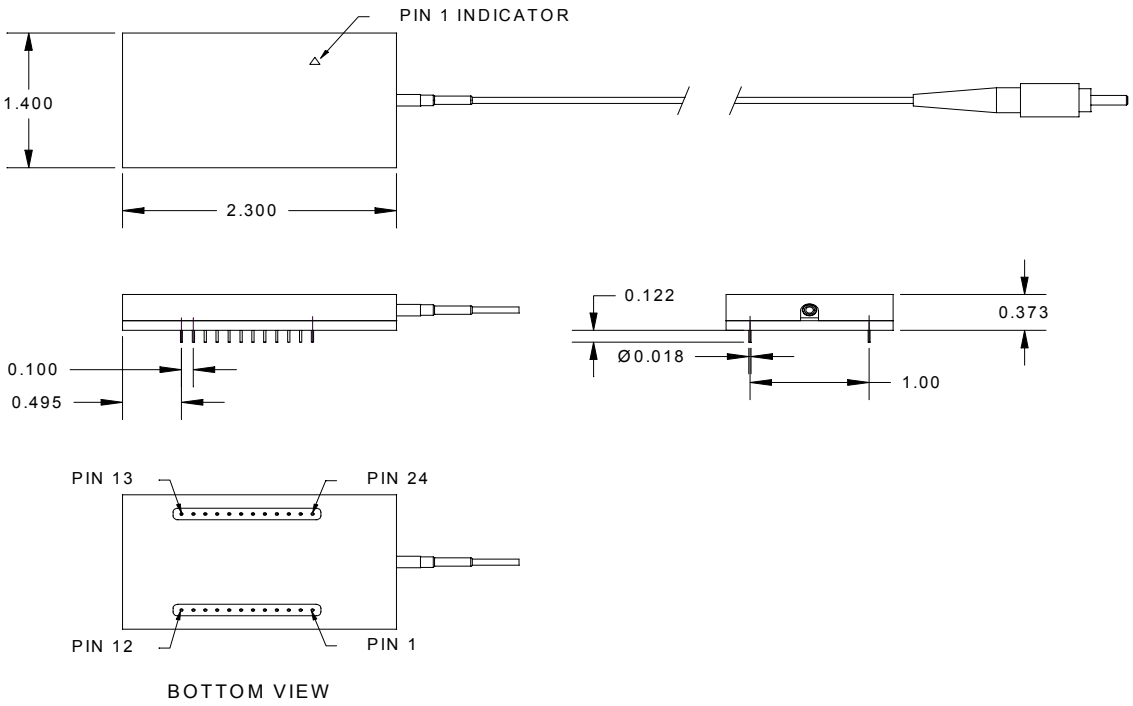


Figure 3. SRM2488-1 Outline Diagram

Ordering Information

Standard modules are built with Singlemode fiber, PVC buffer with an outer jacket diameter of 900um. Alternative fiber type, connector type and fiber lengths are available upon request. Contact factory for specific details. Evaluation fixtures are available to facilitate module and system tests.

Table 7. Part Numbers

Fiber-Optic Connector[1]	Model Number	VI Code Number
FC/PC	SRM2488-1A	330022542
SC	SRM2488-1C	330022559
Evaluation Fixture	SRM2488-1TF	330020678

1. Other connectors or fiber requirements are available to meet specific application requirement

Application Diagram

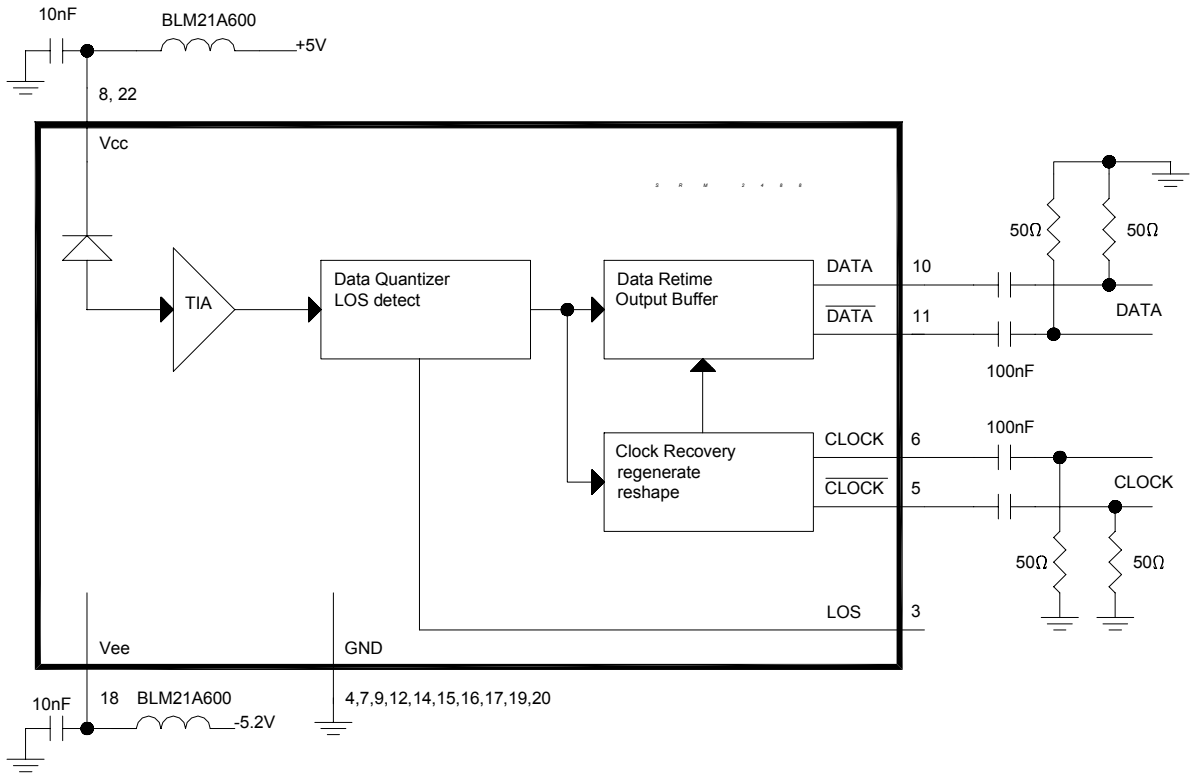


Figure 4. SRM2488-1 Application Diagram

When interfacing and biasing the SRM2488-1 Fiber-Optic Receiver module, please refer to Figure 4 and note the following.

1. Use High quality multilayer printed wiring board with an imbedded ground plane. Ground plane should also occupy the area directly beneath the optical module.
2. Install a 10nF, 0603 low-ESR chip capacitor as close as possible to each Vcc and Vee power supply pin, providing a short low-inductance path to the internal ground plane. Additional filtering can be provided by adding an inductor bead in series with each supply.
3. The optical receiver outputs are designed to drive matched-impedance, AC-coupled 50Ω loads. Clock and Data outputs must be terminated with matched loads, even if only one output is to be used.

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