630AG Receive Converter

Features

- Data loopback mode
- Automatic output shutdown
- Dual-rail PCM output
- Internal phase-locked loop
- Unipolar clock output
- TTL-compatible output

Description

The 630AG Receive Converter hybrid integrated circuit (HIC) extracts clock and PCM information from the incoming bipolar digital line and regenerates unipolar clock and dual-rail PCM signals at its output for DS1 applications. A data loopback capability and an automatic output shutdown mechanism are provided. The 630AG Receive Converter is available in a 20-pin ceramic HIC DIP and requires a single 5 V supply.

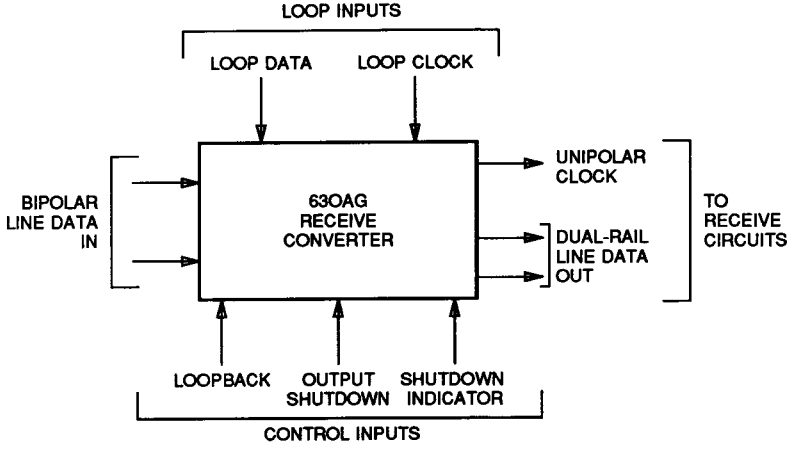
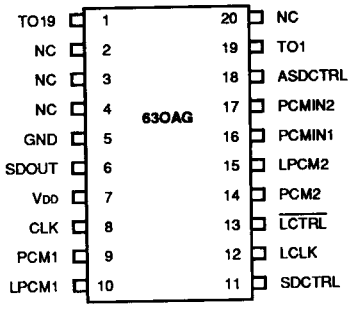


Figure 1. Receive Converter Simplified Functional Diagram

User Information

Pin Descriptions



Symbol	Pin	Symbol	Pin
ASDCTRL	18	PCM1	9
CLK	8	PCM2	14
GND	5	PCMIN1	16
LCLK	12	PCMIN2	17
$\overline{\text{LCTRL}}$	13	SDCTRL	11
LPCM1	10	SDOUT	6
LPCM2	15	TO1	19
NC	2—4,	TO19	1
	20	VDD	7

Figure 2. Pin Function Diagram and Alphabetical Listing of Symbols

Table 1. Pin Descriptions

Pin	Symbol	Type	Name/Function
1	TO19	—	**Connect to Pin 19.**
2 3 4	NC	—	**No Connection.**
5	GND	—	**Ground.**
6	SDOUT	O	**Shutdown Output.** When high, indicates output shutdown.
7	VDD	—	**5 V Supply.**
8	CLK	O	**Recovered Clock.** 1.544-MHz square-wave clock output.
9	PCM1	O	**Line Data Output 1.** In conjunction with PCM2 (pin 14), provides dual-rail output.
10	LPCM1	I	**Loop Line Data 1.** When high, input for data loopback mode is looped back to the input via LPCM1 and LPCM2 (pin 15).
11	SDCTRL	I	**Shutdown Control.** When tied to ASDCTRL (pin 18), turns off the clock and PCM outputs if there is a loss of incoming signal. This feature is disabled by tying SDCTRL high.
12	LCLK	I	**Loop Clock.** Clock signal used in loopback mode.
13	$\overline{\text{LCTRL}}$	I	**Loop Control.** When low, inputs LPCM1 and LPCM2 are inverted and looped back to outputs PCM1 and PCM2.

Table 1. Pin Descriptions (Continued)

Pin	Symbol	Type	Name/Function
14	PCM2	O	**Line Data Output 2.** In conjunction with PCM1 (pin 9), provides dual-rail output.
15	LPCM2	I	**Loop Line Data Input 2.** When high, input for data loopback mode is looped back to the input via LPCM2 and LPCM1 (pin 10).
16	PCMIN1	I	**Line Data Input 1.** Bipolar line data input from the digital line.
17	PCMIN2	I	**Line Data Input 2.** Bipolar line data input from the digital line.
18	ASDCTRL	O	**Automatic Shutdown Control.** Active when tied to SDCTRL (pin 11). Turns off the clock and PCM outputs if there is a loss of incoming signal.
19	TO1	—	**Connect to Pin 1.**
20	NC	—	**No Connection.**

Operation

The primary functions of the 630AG Receive Converter (RCV) are to extract clock and PCM information from the incoming 1.544-MHz bipolar digital line and to regenerate unipolar clock and dual-rail PCM signals.

The incoming signal is applied to the RCV at PCMIN1 and PCMIN2. A transformer and resistor network is needed to provide the proper impedance match to the 100-Ω twisted-pair line (see Figure 3). The RCV converts this bipolar signal to a dual-rail, 100% duty cycle, TTL-compatible signal. The dual-rail output is required to detect bipolar violations. The nominal bipolar signal measured at pins 16 and 17 is 6 Vpp, with the minimum and maximum values at 2 Vpp and 12 Vpp, respectively.

The RCV contains a phase-locked loop (PLL) to extract the clock from the line signal. The extracted clock appears at CLK. The PLL free-running frequency is preadjusted to 1.544 MHz. In order for the RCV to lock onto the incoming signal, there must be a minimum density of at least one 1 every 16 bits (i.e., a maximum of fifteen 0s in a row).

Timing for the dual rail signal is shown in Figure 4. If the incoming PCM bit is a 0, both rails are high. Incoming 1s are represented by a low pulse on one rail only, with the low pulse alternating between the two rails for successive incoming data bits that are equal to 1. Two successive low pulses on the same rail represents a bipolar violation. Data is accepted on the falling edge of the 1.544-MHz clock.

An automatic output shutdown mechanism is incorporated to turn off the clock and PCM outputs if there is a loss of incoming signal. This feature is enabled by tying SDCTRL to ASDCTRL and is disabled by tying SDCTRL high.

Approximately 400 μs after the last 1 has been received, the voltage level on ASDCRTL is 0. If the automatic output shutdown mechanism is being used (SDCTRL tied to ASDCTRL), the clock stops and SDOUT goes high, indicating that a shutdown condition exists.

For maintenance purposes, a data loopback feature is provided. A low at the $\overline{\text{LCTRL}}$ input puts the 630AG in loopback mode. When the receive converter is in the loopback mode, the clock signal is taken from LCLK and is not extracted from the incoming data. The data entered via LPCM1 and LPCM2 is the inverse of the data output on PCM1 and PCM2. The automatic output shutdown feature is not available in the loopback mode.

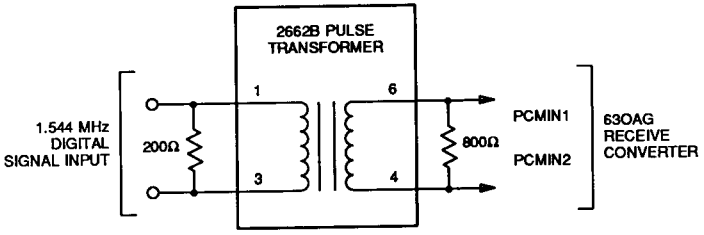


Figure 3. Transformer and Resistor Network

Characteristics

Clocks

Recovered clock: 1.544 MHz
Loop clock: 1.544 MHz

Electrical Characteristics

T_A = 0 to 85 °C, V_{DD} = 5 V ± 0.5 V, GND = 0 V

Parameter	Symbol	Min	Max	Unit
Supply current	I_{DD}	—	80	mA
Input current:				
high	I_{IH}	—	40	μA
low	I_{IL}	—	−1.6	mA
Output current:				
high	I_{OH}	—	−0.4	mA
low	I_{OL}	—	3	mA
Input voltage:				
high	V_{IH}	2.2	V_{DD}	V
low	V_{IL}	—	0.8	V
Output voltage:				
high	V_{OH}	2.4	V_{DD}	V
low	V_{OL}	—	0.6	V
Power dissipation	PD	—	400	mW

Maximum Ratings

Voltage range on any pin with respect to ground ..... −0.5 to +7 V
Ambient operating temperature (T_A) range ..... 0 to 85 °C
Storage temperature (Tstg) range ..... −40 to +90 °C
Power dissipation (PD) ..... 400 mW

Maximum ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

The external leads can be bonded or soldered safely at temperatures up to 300 °C.

Timing Characteristics and Requirements

Table 2. Normal Mode I/O Format (See Figure 4)

Symbol	Description	Min	Typ	Max	Unit
Requirements					
tLDIHLDIL	Line data input high	294	324	354	ns
tCLKHCLKH	CLK period*	647	647	648	ns
Characteristics					
tASDLCLKO	ASDCTRL low to CLK off	—	0	—	μs
tLDIHPCM1L	LDI high to PCM1 low	—	324	—	ns
tPCMPW	PCM1 pulse width	647	647	648	ns
tASDLSDOH	ASD low to SDOUT high	—	0	—	μs
tLDILASDL	Input data zero to ASDL low	—	400	—	μs

* This corresponds to a line frequency of 1.544 MHz ± 50 ppm.

Table 3. Loopback Mode I/O Format (See Figure 5)

Symbol	Description	Min	Typ	Max	Unit
Requirements					
tLCLKHLCLKH	Loop CLK period	647	647	648	ns
tLPCM1HLPCM1L	LPCM1 high	647	647	648	ns

Timing Diagrams

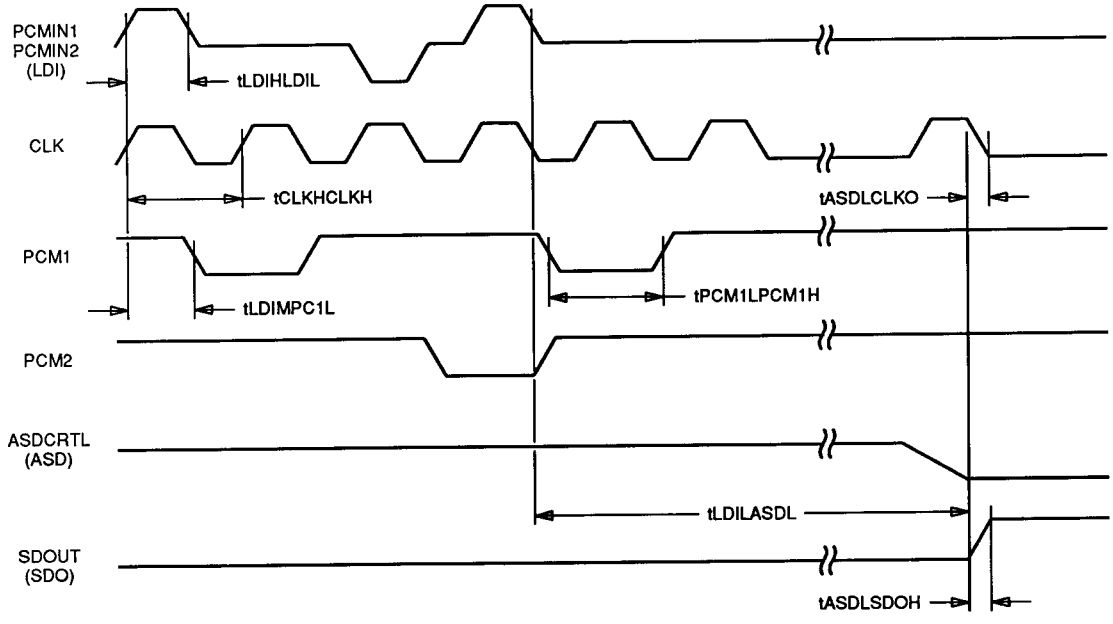


Figure 4. Normal Mode I/O Format

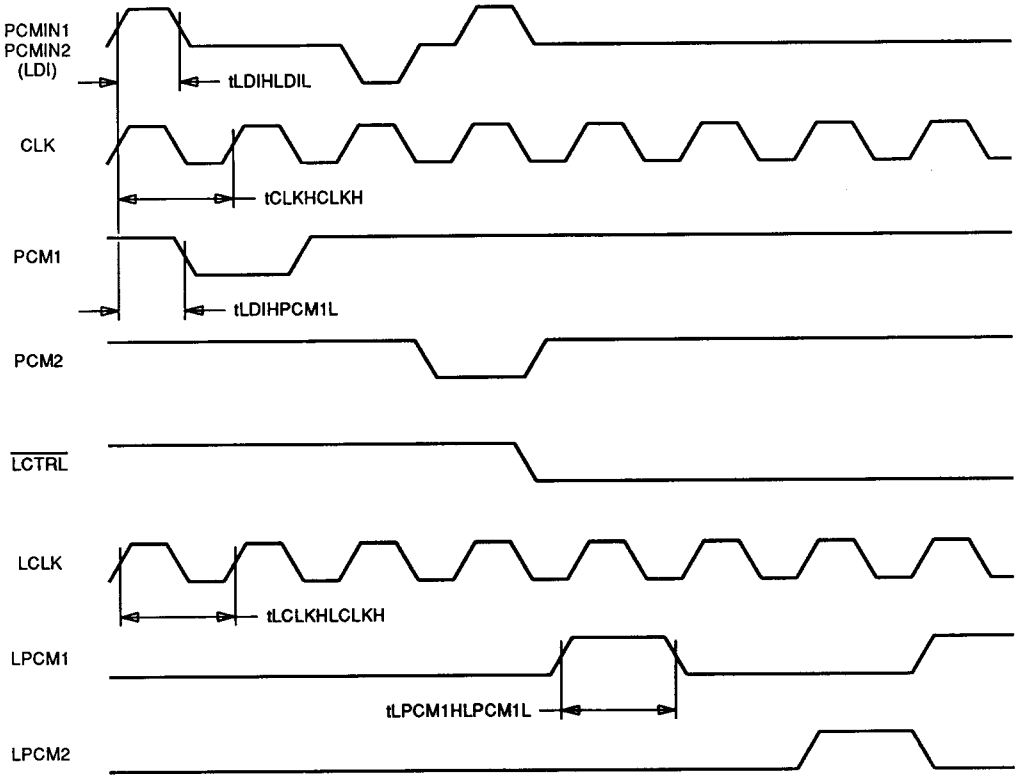


Figure 5. Loopback Mode I/O Format