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MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

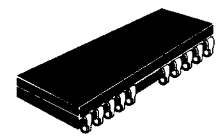
MCM514101A

Advance Information
4Mx1 CMOS Dynamic RAM
Nibble Mode

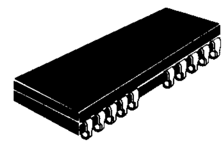
The MCM514101A is a 0.7μ CMOS high-speed, dynamic random access memory. It is organized as 4,194,304 one-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost. The fast nibble mode feature allows high–speed serial access of up to 4 bits of data.

The MCM514101A requires only 11 address lines; row and column address inputs are multiplexed. The device is packaged in standard 300 mil and 350 mil J–lead small outline packages, and a 100 mil zig-zag in-line package (ZIP).

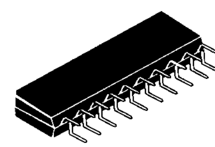
- Three-State Data Output
- Fast Nibble Mode
- Test Mode
- TTL-Compatible Inputs and Outputs
- $\overline{RAS}$ Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 1024 Cycle Refresh: MCM514101A = 16 ms
- Fast Access Time (t_{RAC}):
  - MCM514101A-60 = 60 ns (Max)
  - MCM514101A-70 = 70 ns (Max)
  - MCM514101A-80 = 80 ns (Max)
  - MCM514101A-10 = 100 ns (Max)
- Low Active Power Dissipation:
  - MCM514101A-60 = 660 mW (Max)
  - MCM514101A-70 = 550 mW (Max)
  - MCM514101A-80 = 468 mW (Max)
  - MCM514101A-10 = 413 mW (Max)
- Low Standby Power Dissipation:
  - MCM514101A = 11 mW (Max, TTL Levels)
  - MCM514101A = 5.5 mW (Max, CMOS Levels)



NJ PACKAGE
300 MIL SOJ
CASE 822



J PACKAGE
350 MIL SOJ
CASE 822A

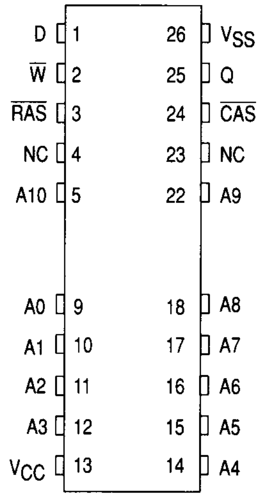


Z PACKAGE
PLASTIC
ZIG-ZAG IN-LINE
CASE 836

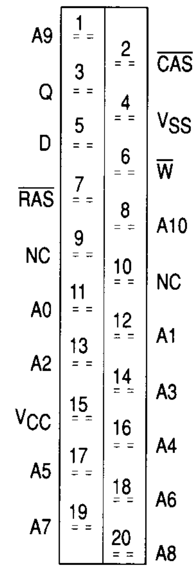
PIN NAMES	
A0–A10	Address Input
D	Data Input
Q	Data Output
$\overline{W}$	Read/Write Enable
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power Supply (+5 V)
V_{SS}	Ground
NC	No Connection

PIN ASSIGNMENT

300 AND 350 MIL SOJ



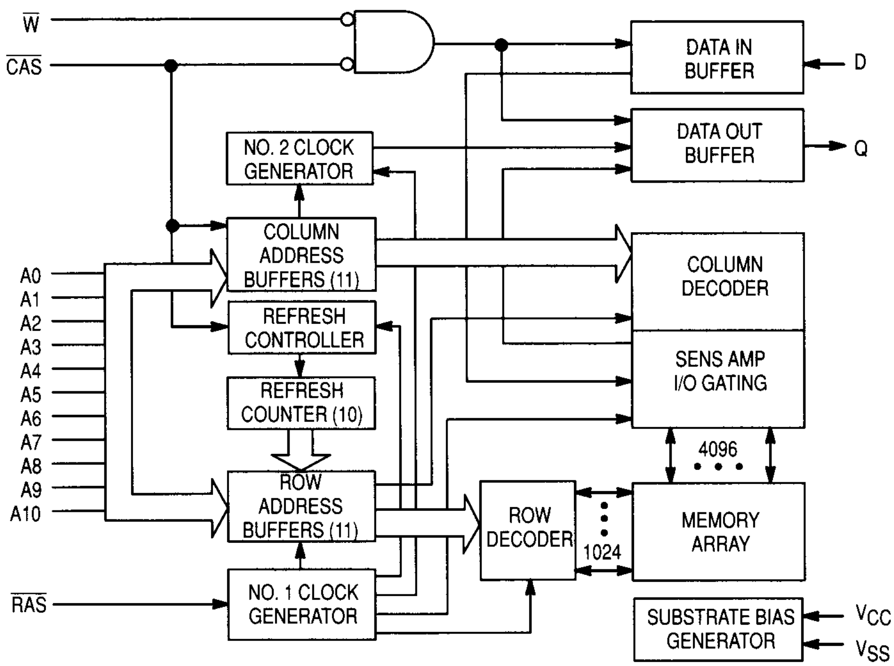
100 MIL ZIP



This document contains information on a new product. Specifications and information herein are subject to change without notice.

MOTOROLA

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–1 to +7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	–1 to +7	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	700	mW
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	–55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0		
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V	1
Logic Low Voltage, All Inputs	V_{IL}	–1.0	—	0.8	V	1

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	I_{CC1}			mA	2, 3
MCM514101A-60, t_{RC} = 110 ns		—	120		
MCM514101A-70, t_{RC} = 130 ns		—	100		
MCM514101A-80, t_{RC} = 150 ns		—	85		
MCM514101A-10, t_{RC} = 180 ns		—	75		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$=$\overline{CAS}$=V_{IH})	I_{CC2}	—	2.0	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ Only Refresh Cycles ($\overline{CAS}$=V_{IH})	I_{CC3}			mA	2, 3
MCM514101A-60, t_{RC} = 110 ns		—	120		
MCM514101A-70, t_{RC} = 130 ns		—	100		
MCM514101A-80, t_{RC} = 150 ns		—	85		
MCM514101A-10, t_{RC} = 180 ns		—	75		
V_{CC} Power Supply Current During Nibble Mode Cycle ($\overline{RAS}$ = V_{IL})	I_{CC4}			mA	2, 3
MCM514101A-60, t_{NC} = 40 ns		—	50		
MCM514101A-70, t_{NC} = 40 ns		—	50		
MCM514101A-80, t_{NC} = 40 ns		—	50		
MCM514101A-10, t_{NC} = 45 ns		—	45		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$=$\overline{CAS}$=V_{CC}–0.2 V)	I_{CC5}	—	1.0	mA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	I_{CC6}			mA	2
MCM514101A-60, t_{RC} = 110 ns		—	120		
MCM514101A-70, t_{RC} = 130 ns		—	100		
MCM514101A-80, t_{RC} = 150 ns		—	85		
MCM514101A-10, t_{RC} = 180 ns		—	75		
Input Leakage Current (0 V ≤ V_{in} ≤ 6.5 V)	$I_{lkg(I)}$	–10	10	µA	
Output Leakage Current ($\overline{CAS}$ = V_{IH}, 0 V ≤ V_{out} ≤ 5.5 V)	$I_{lkg(O)}$	–10	10	µA	
Output High Voltage (I_{OH} = –5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit	Notes
Input Capacitance	A0–A10, D	C_{in}	5	pF	4
	$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$		7		
Output Capacitance ($\overline{CAS}$ = V_{IH} to Disable Output)	Q	C_{out}	7	pF	4

NOTES:

1. All voltages referenced to V_{SS}.
2. Current is a function of cycle rate and output loading; maximum currents are specified cycle time (minimum) with the output open.
3. Column address can be changed once or less while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
4. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		514100A-60		514100A-70		514100A-80		514100A-10		Unit	Notes
	Std.	Alt.	Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	110	—	130	—	150	—	180	—	ns	5
Read-Write Cycle Time	t_{RELREL}	t_{RWC}	135	—	155	—	175	—	210	—	ns	5
Nibble Mode Cycle Time	t_{CEHCEH}	t_{NC}	40	—	40	—	40	—	45	—	ns	
Nibble Mode Read-Write Cycle Time	t_{CELCEL}	t_{NRWC}	65	—	65	—	65	—	70	—	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	—	60	—	70	—	80	—	100	ns	6, 7
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	—	20	—	20	—	20	—	25	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	30	—	35	—	40	—	50	ns	6, 9
Nibble Mode Access Time	t_{CELQV}	t_{NCAC}	—	20	—	20	—	20	—	25	ns	6
$\overline{CAS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	0	—	0	—	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	0	20	0	20	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	40	—	50	—	60	—	70	—	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	60	10 k	70	10 k	80	10 k	100	10 k	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	20	—	20	—	25	—	ns	
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	60	—	70	—	80	—	100	—	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10 k	20	10 k	20	10 k	25	10 k	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	40	20	50	20	60	25	75	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	30	15	35	15	40	20	50	ns	12
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	5	—	10	—	ns	
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CP}	10	—	10	—	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	10	—	15	—	ns	

(continued)

NOTES:

1. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is ensured.
6. Measured with a current load equivalent to 2 TTL (–200 µA, +4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \le t_{RCD}$ (max).
8. Assumes that $t_{RCD} \ge t_{RCD}$ (max).
9. Assumes that $t_{RAD} \ge t_{RAD}$ (max).
10. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.

READ, WRITE, AND READ-WRITE CYCLES (Continued)

Parameters	Symbol		514101A-60		514101A-70		514101A-80		514101A-10		Unit	Notes
	Std.	Alt.	Min	Max	Min	Max	Min	Max	Min	Max		
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	15	—	20	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t_{AVREH}	t_{RAL}	30	—	35	—	40	—	50	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CEHWX}	t_{RCH}	0	—	0	—	0	—	0	—	ns	13
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{REHWX}	t_{RRH}	0	—	0	—	0	—	0	—	ns	13
Write Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CELWH}	t_{WCH}	10	—	15	—	15	—	20	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	10	—	15	—	15	—	20	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	20	—	25	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	20	—	25	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	0	—	0	—	ns	14
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	15	—	20	—	ns	14
Refresh Period	t_{RVRV}	t_{RFSH}	—	16	—	16	—	16	—	16	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	0	—	0	—	ns	15
$\overline{\text{CAS}}$ to Write Delay	t_{CELWL}	t_{CWD}	20	—	20	—	20	—	25	—	ns	15
$\overline{\text{RAS}}$ to Write Delay	t_{RELWL}	t_{RWD}	60	—	70	—	80	—	100	—	ns	15
Column Address to Write Delay Time	t_{AVWL}	t_{AWD}	30	—	35	—	45	—	50	—	ns	15
$\overline{\text{CAS}}$ Setup Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEL}	t_{CSR}	5	—	5	—	5	—	5	—	ns	
$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEH}	t_{CHR}	15	—	15	—	15	—	20	—	ns	
$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	0	—	0	—	ns	
$\overline{\text{CAS}}$ Precharge Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Counter Test	t_{CEHCEL}	t_{CPT}	30	—	40	—	40	—	50	—	ns	

(continued)

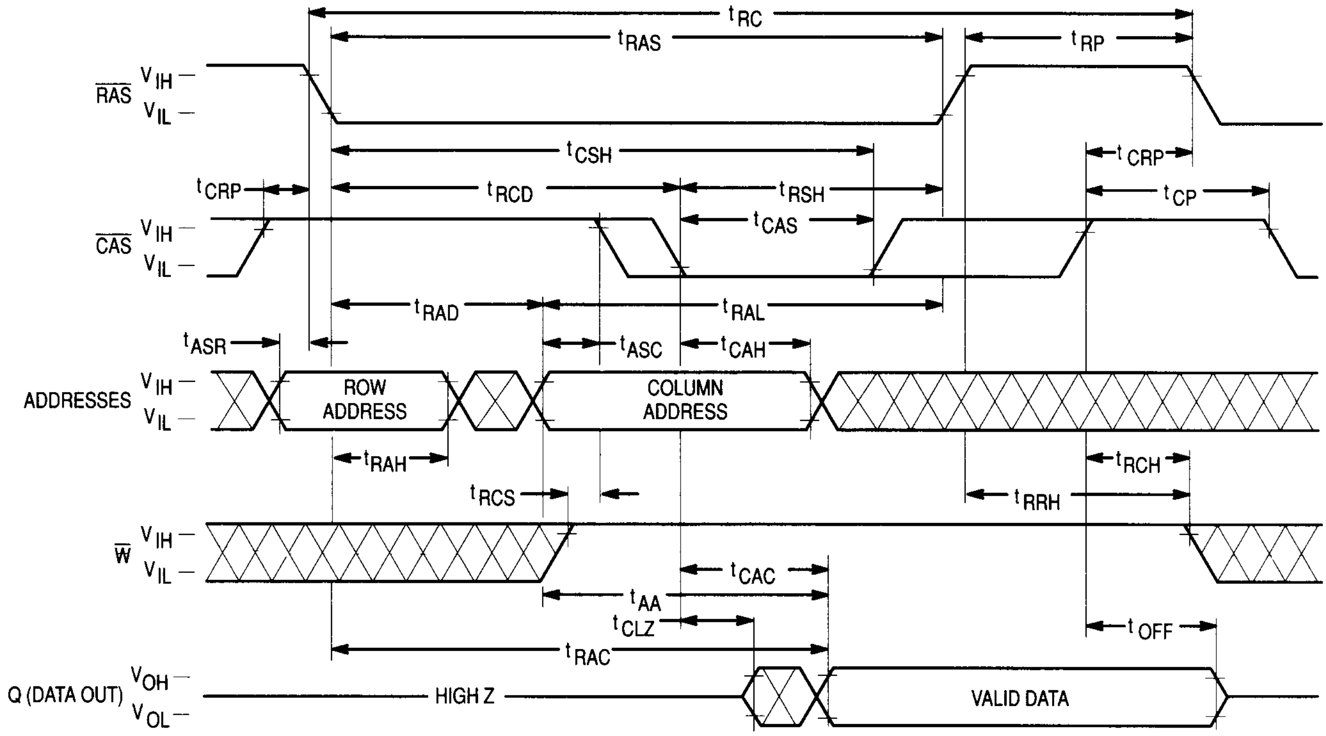
NOTES:

13. Either t_{RRH} or t_{RCH} must be staisfied for a read cycle.
14. These two parameters are referecnced to $\overline{\text{CAS}}$ leading edgein early write cycles and to $\overline{\text{W}}$ leading edge in read–write cycles.
15. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPWD} \geq t_{CPWD}$ (min) (page mode), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

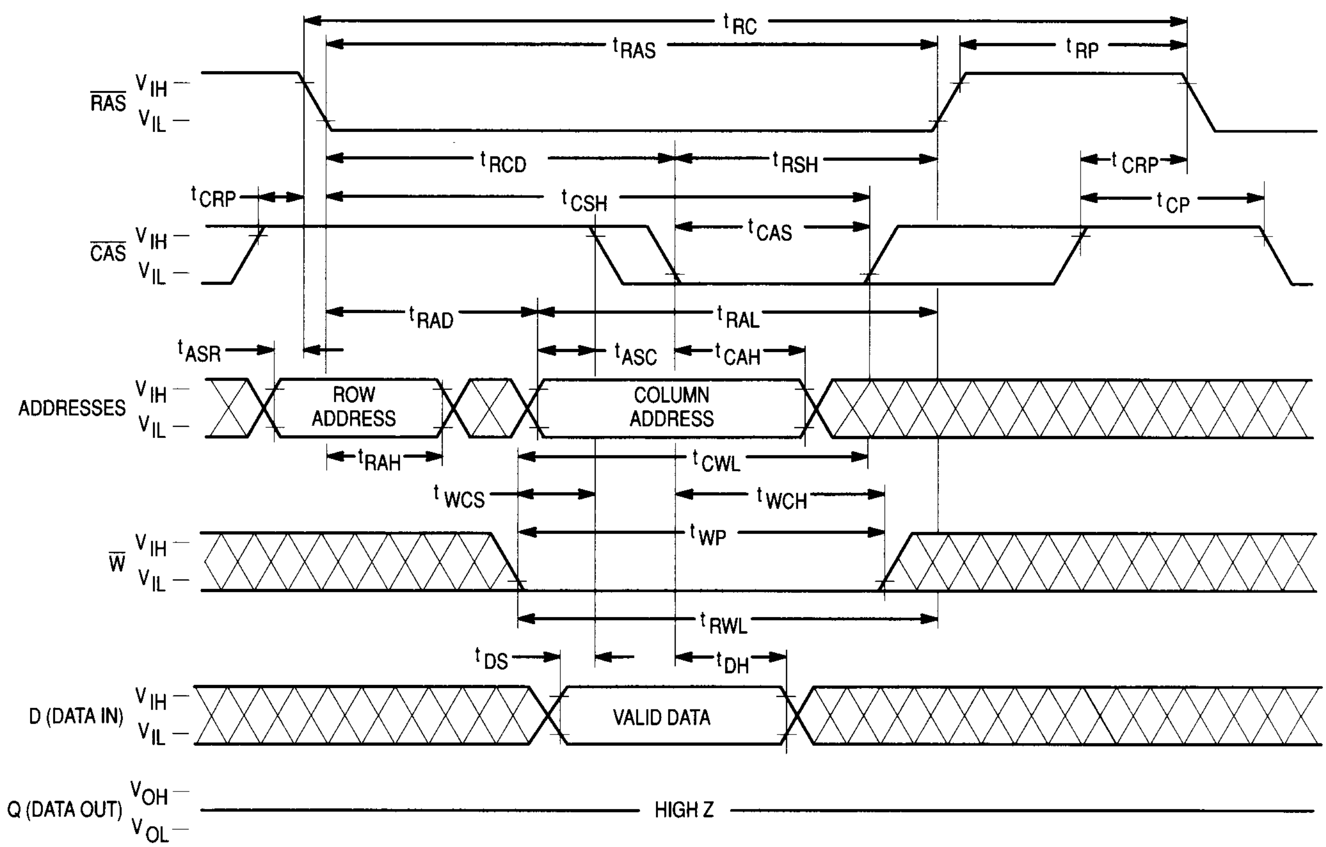
READ, WRITE, AND READ-WRITE CYCLES (Continued)

Parameters	Symbol		514101A-60		514101A-70		514101A-80		514101A-10		Unit	Notes
	Std.	Alt.	Min	Max	Min	Max	Min	Max	Min	Max		
Nibble Mode Pulse Width	t_{CELCEH}	t_{NCAS}	20	—	20	—	20	—	25	—	ns	
Nibble Mode $\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{NCP}	10	—	10	—	10	—	10	—	ns	
Nibble Mode $\overline{RAS}$ Hold Time	t_{CELREH}	t_{NRSH}	20	—	20	—	20	—	25	—	ns	
Nibble Mode $\overline{CAS}$ to Write Delay TIme	t_{CELWL}	t_{NCWD}	20	—	20	—	20	—	25	—	ns	
Nibble Mode Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{NRWL}	20	—	20	—	20	—	25	—	ns	
Nibble Mode Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{NCWL}	20	—	20	—	20	—	25	—	ns	
Write Command Setup Time (Test Mode)	t_{WLREL}	t_{WTS}	10	—	10	—	10	—	10	—	ns	
Write Command Hold Time (Test Mode)	t_{RELWH}	t_{WTH}	10	—	10	—	10	—	10	—	ns	
Write to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{WHREL}	t_{WRP}	10	—	10	—	10	—	10	—	ns	
Write to $\overline{RAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{RELWL}	t_{WRH}	10	—	10	—	10	—	10	—	ns	

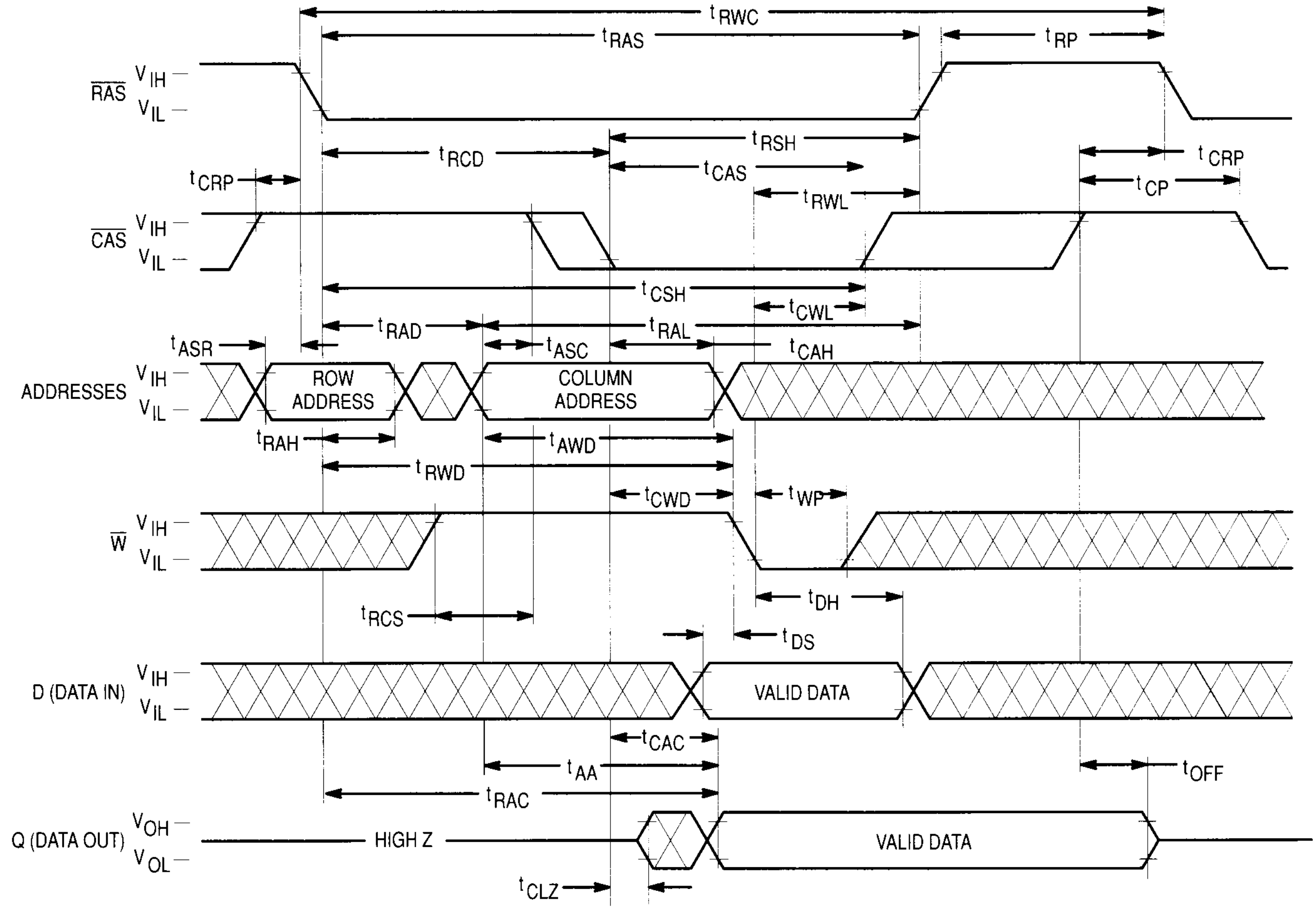
READ CYCLE



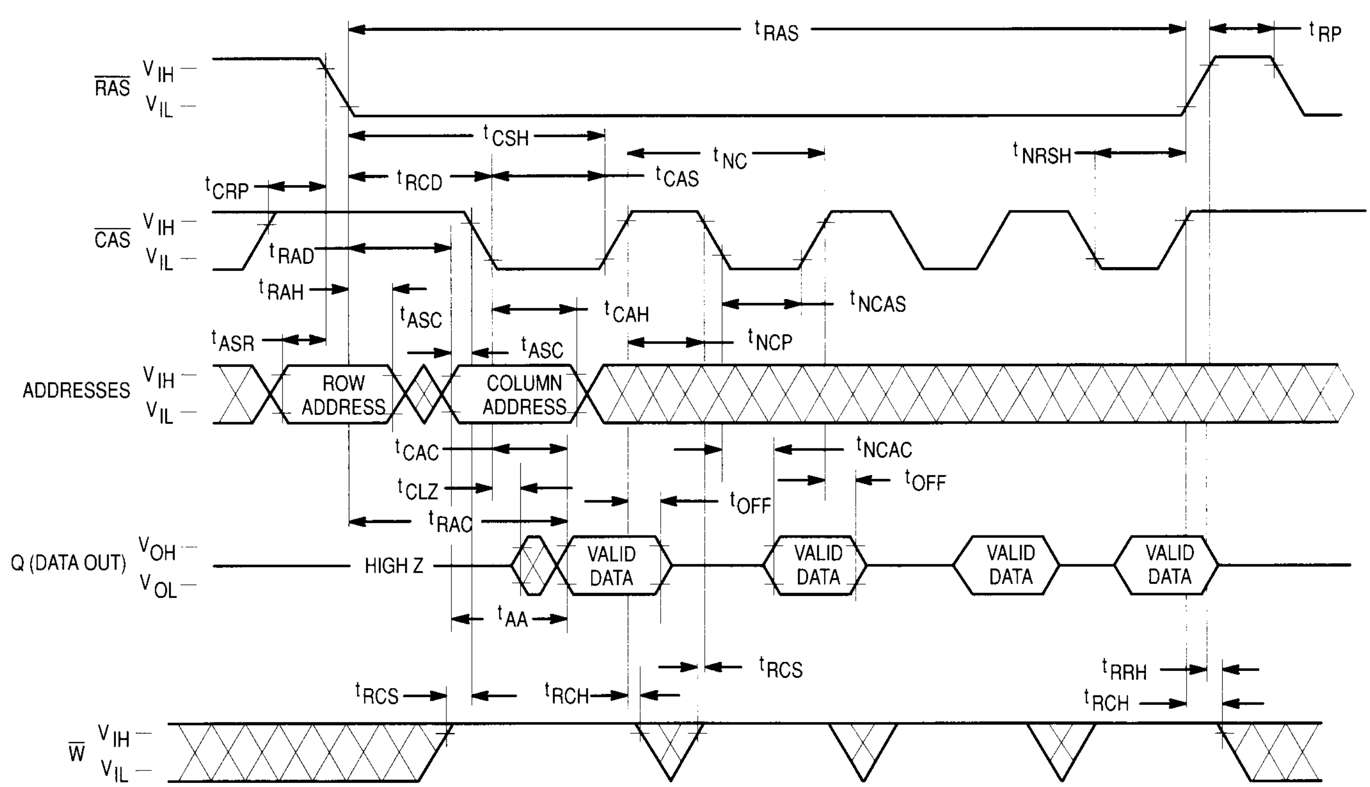
EARLY WRITE CYCLE



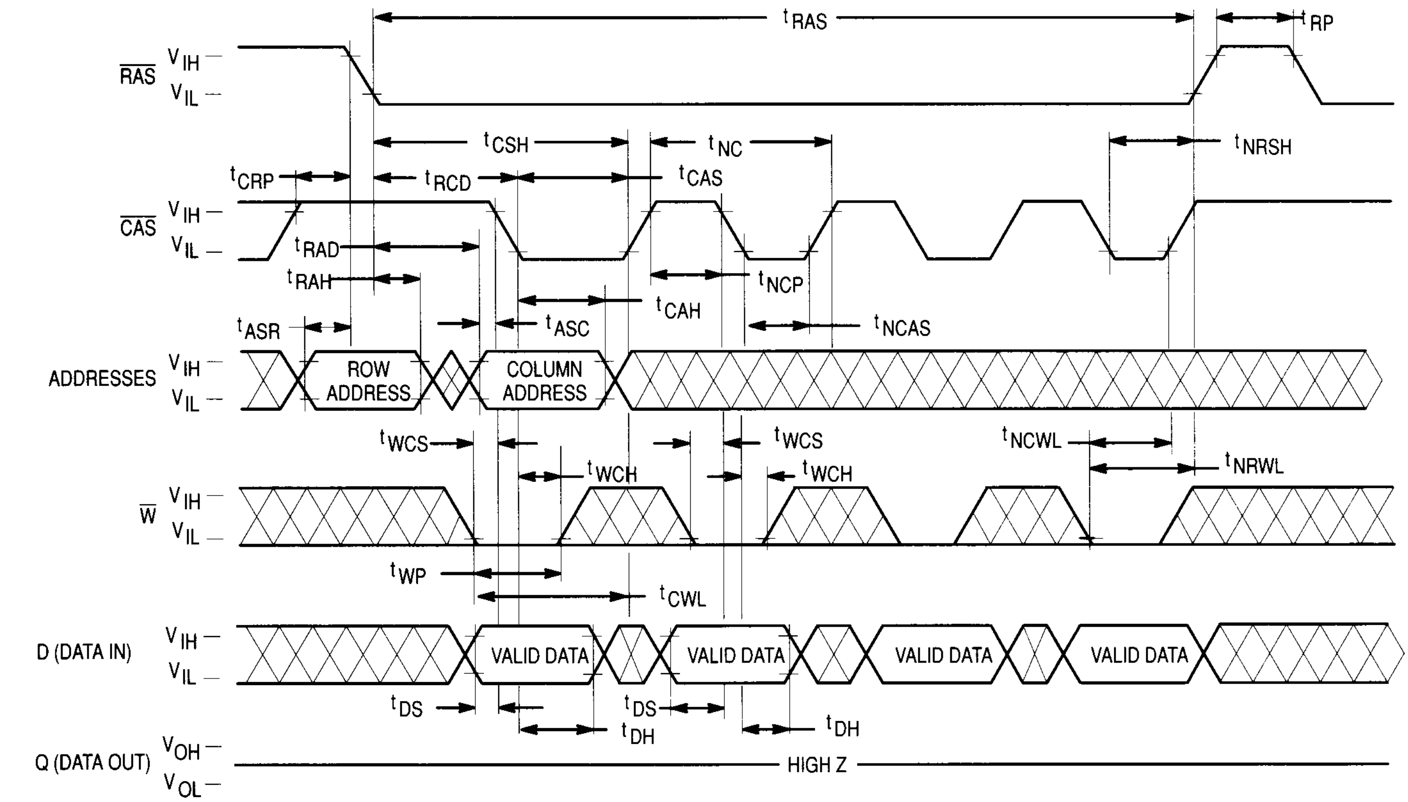
READ-WRITE CYCLE



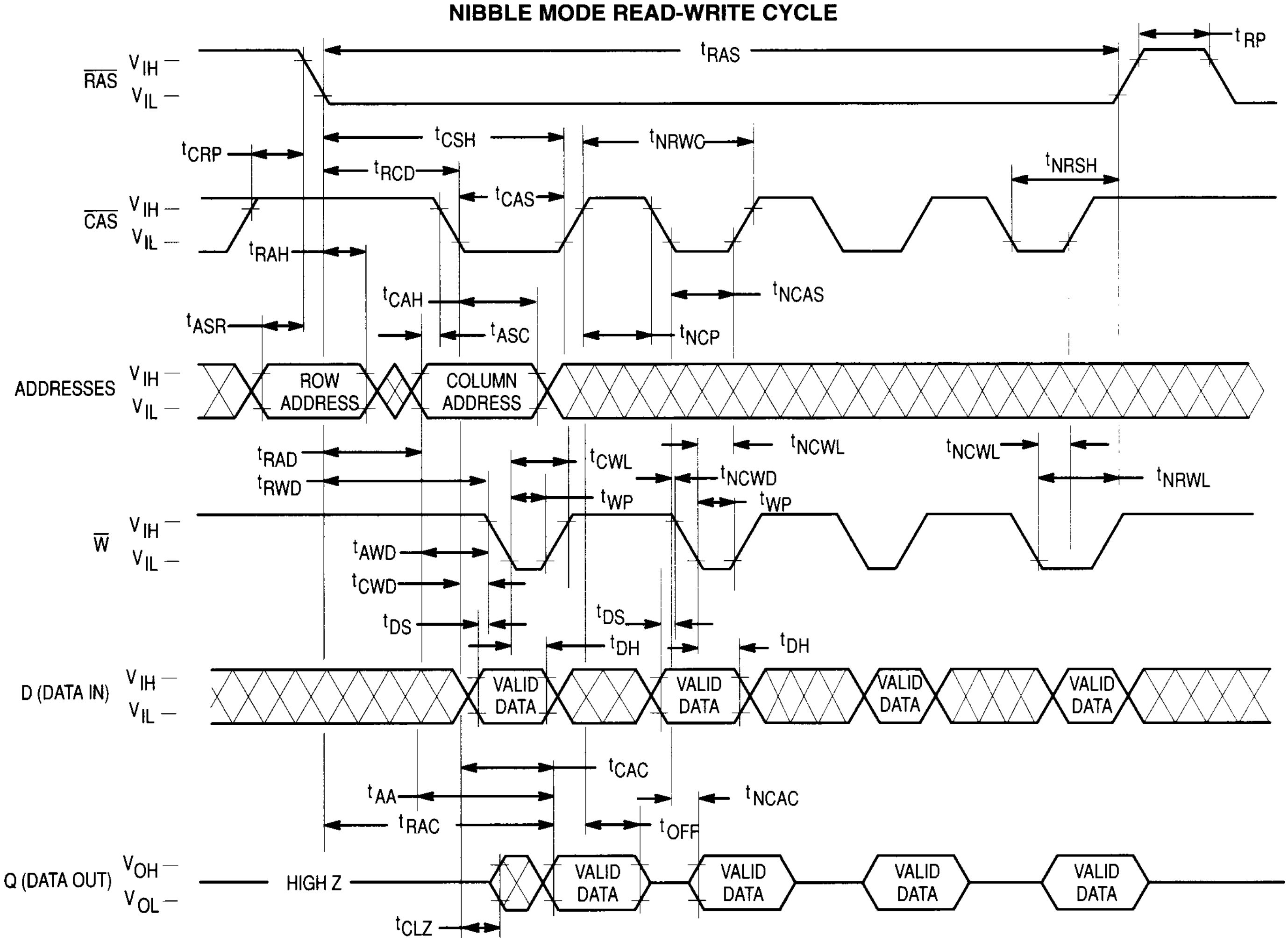
NIBBLE MODE READ CYCLE



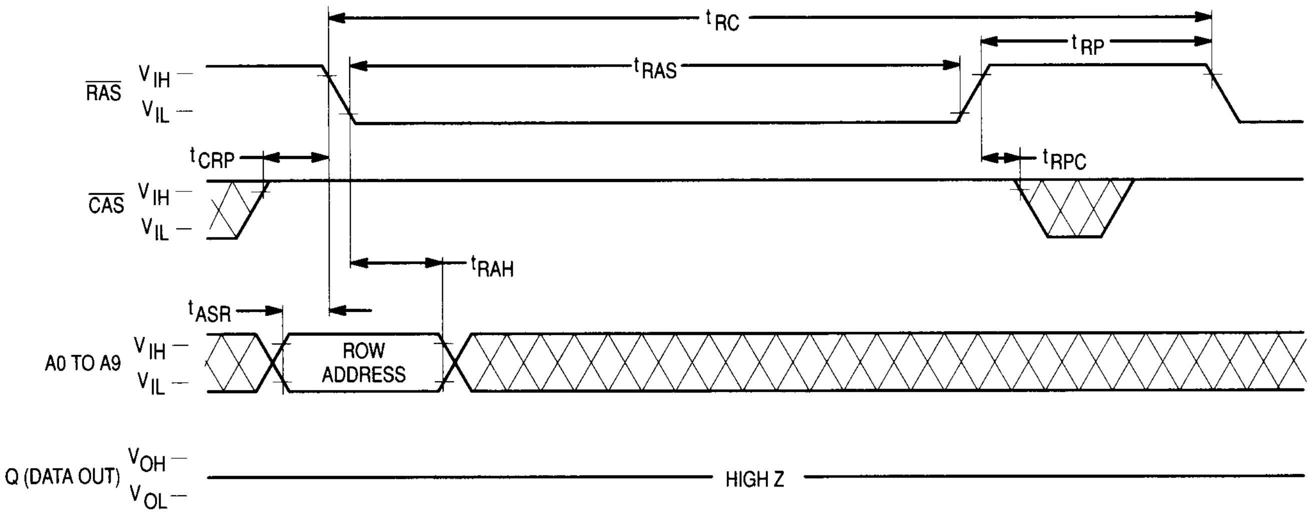
NIBBLE MODE EARLY WRITE CYCLE



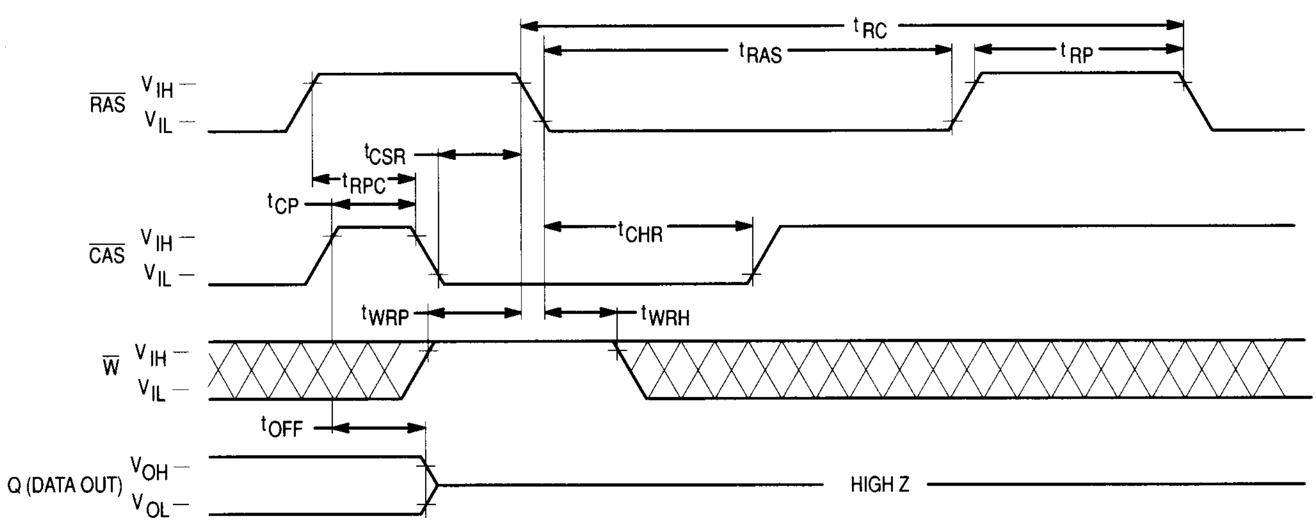
NIBBLE MODE READ-WRITE CYCLE



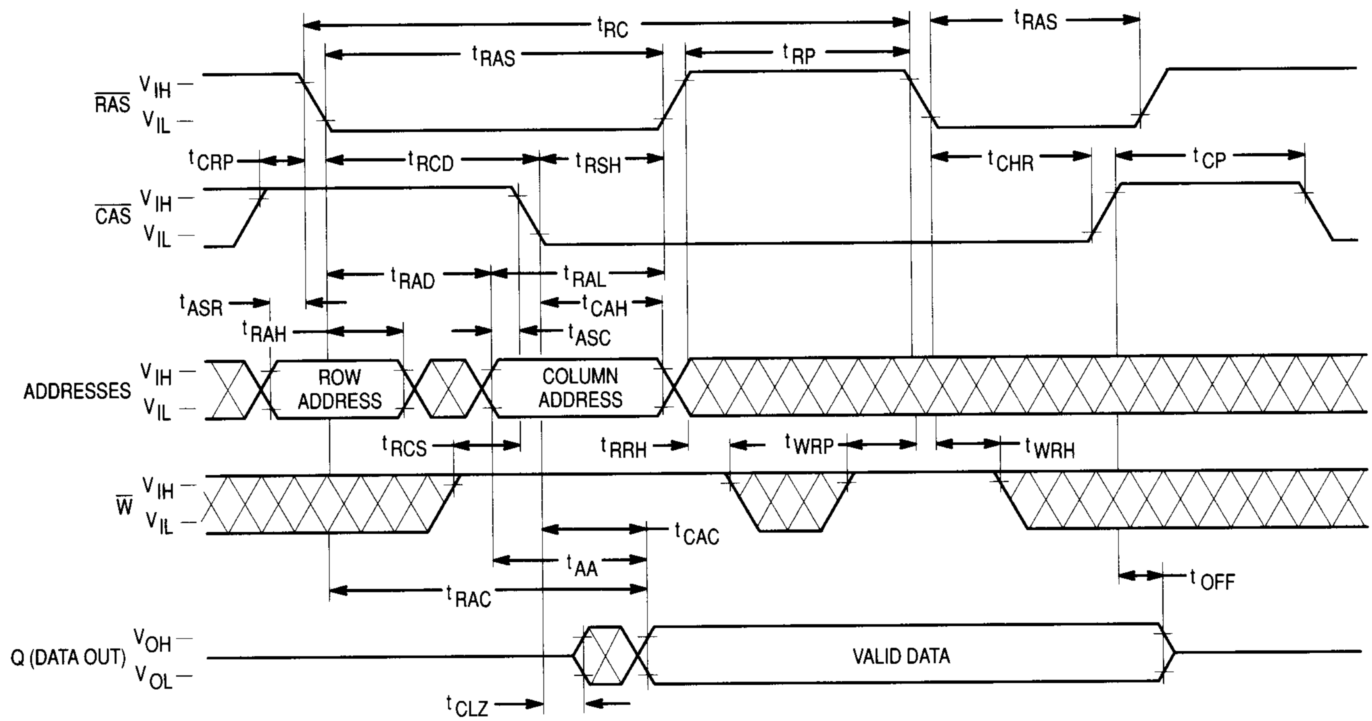
RAS ONLY REFRESH CYCLE
(W and A10 are Don't Care)



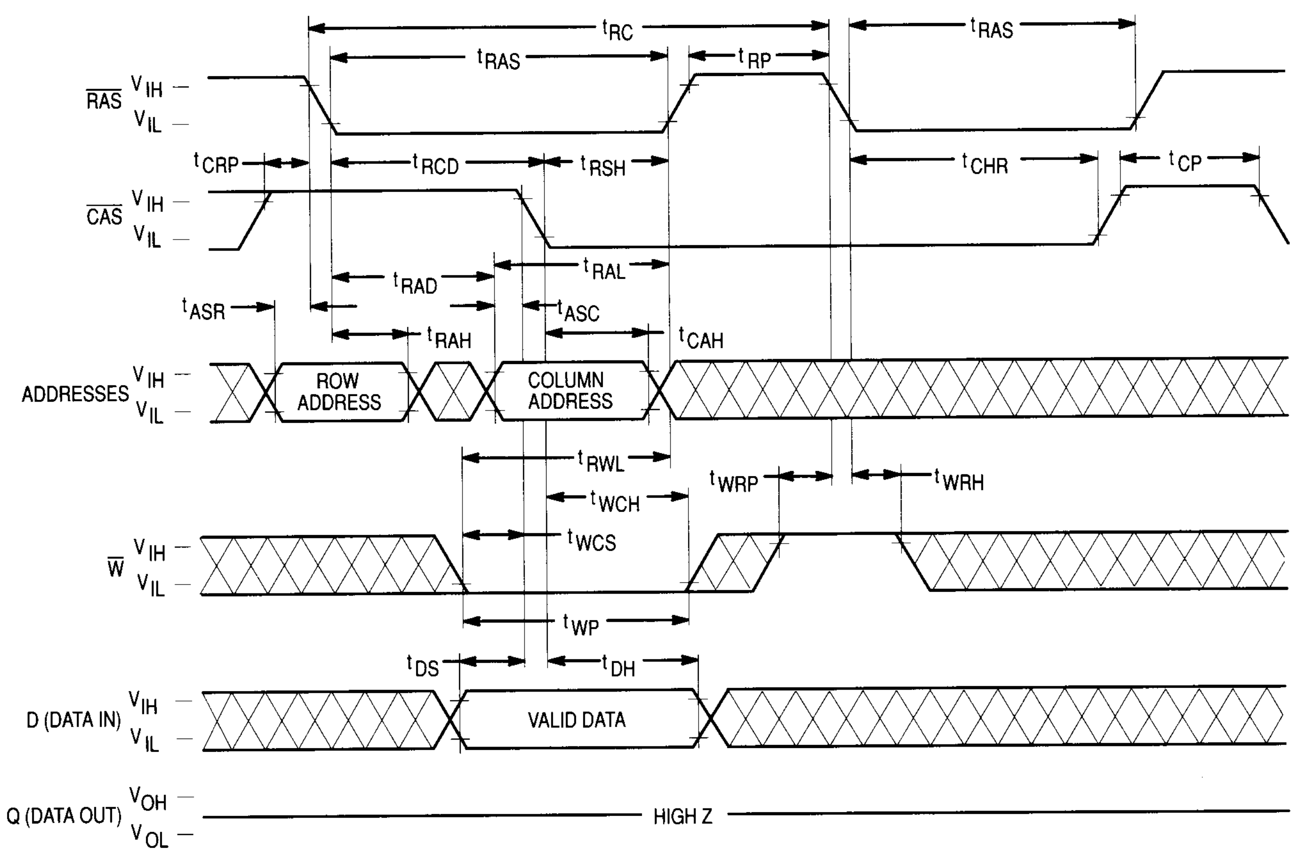
CAS BEFORE RAS REFRESH CYCLE
(A0 to A10 are Don't Care)



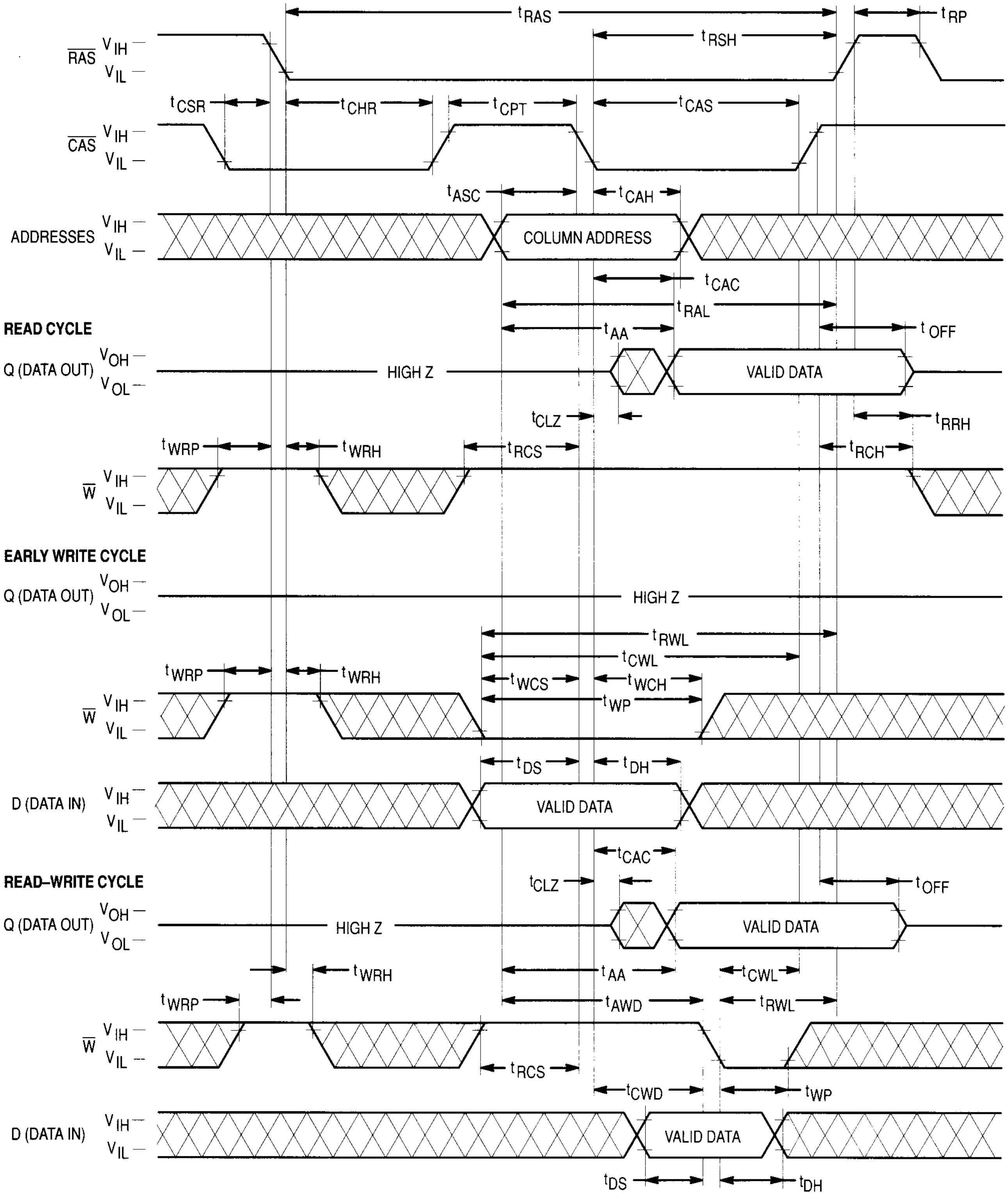
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (EARLY WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DEVICE INITIALIZATION

On power-up an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 16 milliseconds with the device powered up), a wake up sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The eleven address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{RAS}$) and column address strobe ($\overline{CAS}$), into two separate 11-bit address fields. A total of twenty two address bits, eleven rows and eleven columns, will decode one of the 4,194,304 bit locations in the device. $\overline{RAS}$ active transition is followed by $\overline{CAS}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{RAS}$ and $\overline{CAS}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This "gate" feature on the external $\overline{CAS}$ clock enables the internal $\overline{CAS}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

There are three other variations in addressing the 4M RAM: **$\overline{RAS}$ only refresh cycle, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle,** and **nibble mode**. All three are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with four different cycles: "normal" random read cycle, nibble mode read cycle, read-write cycle, and nibble mode read-write cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{RAS}$ and $\overline{CAS}$ active transitions latching the desired bit location. The write ($\overline{W}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{CAS}$ active transition, to enable read mode.

Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window; however, $\overline{CAS}$ must be active before or at t_{RCD} maximum to guarantee valid data out (Q) at t_{RAC} (access time from $\overline{RAS}$ active transition). If the t_{RCD} maximum is exceeded, read access time is determined by the $\overline{CAS}$ clock active transition (t_{CAC}).

The $\overline{RAS}$ and $\overline{CAS}$ clocks must remain active for a minimum time of t_{RAS} and t_{CAS} respectively, to complete the read cycle. $\overline{W}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{RAS}$ or $\overline{CAS}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{RAS}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. Q is valid, but not latched, as long as the $\overline{CAS}$ clock is active. When the $\overline{CAS}$ clock transitions to inactive, the output will switch to High Z (three-state).

WRITE CYCLE

The user can write to the DRAM with any of four cycles: early write, late write, nibble mode early write, and nibble mode read-write. Early and late write modes are discussed here, while nibble mode write operations are covered in another section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{W}$ to active (V_{IL}). Early and late write modes are distinguished by the active transition of $\overline{W}$, with respect to $\overline{CAS}$. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{W}$ active transition at minimum time t_{WCS} before $\overline{CAS}$ active transition. Data in (D) is referenced to $\overline{CAS}$ in an early write cycle. $\overline{RAS}$ and $\overline{CAS}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

Q remains in three-state condition throughout an early write cycle because $\overline{W}$ active transition precedes or coincides with $\overline{CAS}$ active transition, keeping data-out buffers disabled. This feature can be utilized on systems with a common I/O bus, provided all writes are performed with early write cycles, to prevent bus contention.

A late write cycle occurs when $\overline{W}$ active transition is made after $\overline{CAS}$ active transition. $\overline{W}$ active transition could be delayed for almost 10 microseconds after $\overline{CAS}$ active transition, ($t_{RCD} + t_{CWD} + t_{RWL} + 2t_T) \le t_{RAS}$, if other timing minimums (t_{RCD}, t_{RWL}, and t_T) are maintained. D is referenced to $\overline{W}$ active transition in a late write cycle. Output buffers are enabled by $\overline{CAS}$ active transition but Q may be indeterminate—see note 15 of ac operating conditions table. $\overline{RAS}$ and $\overline{CAS}$ must remain active for t_{RWL} and t_{CWL}, respectively, after $\overline{W}$ active transition to complete the write cycle.

READ-WRITE CYCLE

A read-write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except $\overline{W}$ must remain high for t_{CWD} minimum after the $\overline{CAS}$ active transition, to guarantee valid Q before writing the bit.

NIBBLE MODE CYCLES

Nibble mode allows fast successive serial data operations at two, three, or four bits of the 4M dynamic RAM. Read access time in nibble mode (t_{NCAC}) is considerably faster than the regular $\overline{RAS}$ clock access time, t_{RAC}. Nibble mode operation consists of keeping $\overline{RAS}$ active while toggling $\overline{CAS}$ between V_{IH} and V_{IL}. The address of the first nibble bit is latched by $\overline{RAS}$ and $\overline{CAS}$ active transitions. Each subsequent $\overline{CAS}$ active transition increments the row and column addresses internally to access the next bit in binary fashion. After the fourth bit is accessed, the nibble pattern repeats itself (0,0) (0,1) (1,0) (1,1) (0,0) (0,1) (1,0) (1,1). . . . The A10 address determines the starting point of the 4–bit nibble, with row address A10 the least significant of the (column, row) ordered pair. External addresses are ignored after the first nibble bit is selected.

A nibble mode cycle is initiated by a normal read, write, or read-write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, CAS transitions to inactive for minimum of t_{NCP}, while RAS remains low (V_{IL}). The second CAS active transition while RAS is low initiates the first nibble mode cycle (t_{NC} or t_{NRWC}). Either a read, write, or read-write operation can be performed in a nibble mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive nibble mode cycles and performed in any order. The maximum number of consecutive nibble mode cycles is limited by t_{RAS}. Nibble mode operation ends when RAS transitions to inactive, coincident with or following a CAS inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM514101A require refresh every 16 milliseconds.

This is accomplished by cycling through the 1024 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM514101A. Burst refresh, a refresh of all 1024 rows consecutively, must be performed every 16 milliseconds on the MCM514101A.

A normal read, write, or read-write operation to the RAM will refresh all the bits (4096) associated with the particular row decoded. Three other mehtods of refresh, **RAS-only refresh, CAS before RAS refresh,** and **hidden refresh** are available on this device for greater system flexibility.

RAS-Only Refresh

RAS-only refresh consists of RAS transition to active, latching the row address to be refreshed, while CAS remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

CAS Before RAS Refresh

CAS before RAS refresh is enabled by bringing CAS active before RAS. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle.

The output buffer remains at the same state it was in during the previous cycle (hidden refresh). W must be inactive for time t_{WRP} before and time t_{WRH} after RAS active transition to prevent switching the device into a **test mode cycle**.

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding CAS active the end of a read or write cycle, while RAS cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a CAS before RAS refresh from a cycle in progress (see Figure 1). W is subject to the same conditions with respect to RAS active transition (to prevent test mode cycle) as in CAS before RAS refresh.

CAS BEFORE RAS REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **CAS before RAS refresh counter test**. This test is performed with a read-write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 1024 cycles, as indicated by the check data written in each row. See **CAS before RAS refresh counter test cycle** timing diagram.

The test can be performed after a minimum of **8 CAS before RAS** initialization cycles. Test procedure:

1. Write "0"s into all memory cells with normal write mode.
2. Select a column address, read "0" out and write "1" into the cell by performing the **CAS before RAS refresh counter test, read-write cycle**. Repeat this operation 1024 times.
3. Read the "1"s which were written in step 2 in normal read mode.
4. Using the same starting column address as in step 2, read "1" out and write "0" into the cell by performing the **CAS before RAS refresh counter test, read-write cycle**. Repeat this operation 1024 times.
5. Read "0"s which were written in step 4 in normal read mode.
6. Repeat steps 1 to 5 using complement data.

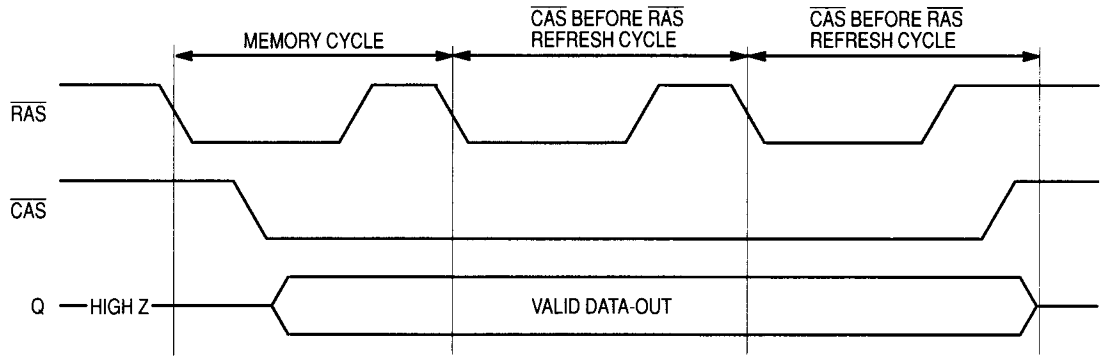


Figure 1. Hidden Refresh Cycle

TEST MODE

The internal organization of this device (512K×8) allows it to be tested as if it were a 512K×1 DRAM. Nineteen of the twenty two addresses are used when operating the device in test mode. Row address A10, and column addresses A0 and A10 are ignored by the device in test mode. A test mode cycle reads and/or writes data to a bit in each of eight 512K blocks (B0–B7) in parallel. External data out is determined by the internal test mode logic of the device. See following truth table and test mode block diagram.

Test mode is enabled by performing a **test mode cycle** (see test mode timing diagram and parameter specifications table). Test mode is disabled by a **$\overline{\text{RAS}}$ only refresh** cycle or **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh** cycle. The test mode performs refresh with the internal refresh counter like a **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh**.

TEST MODE TRUTH TABLE

D	B0	B1	B2	B3	B4	B5	B6	B7	Q
0	0	0	0	0	0	0	0	0	1
1	1	1	1	1	1	1	1	1	1
—	Any Other								0

TEST MODE
AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

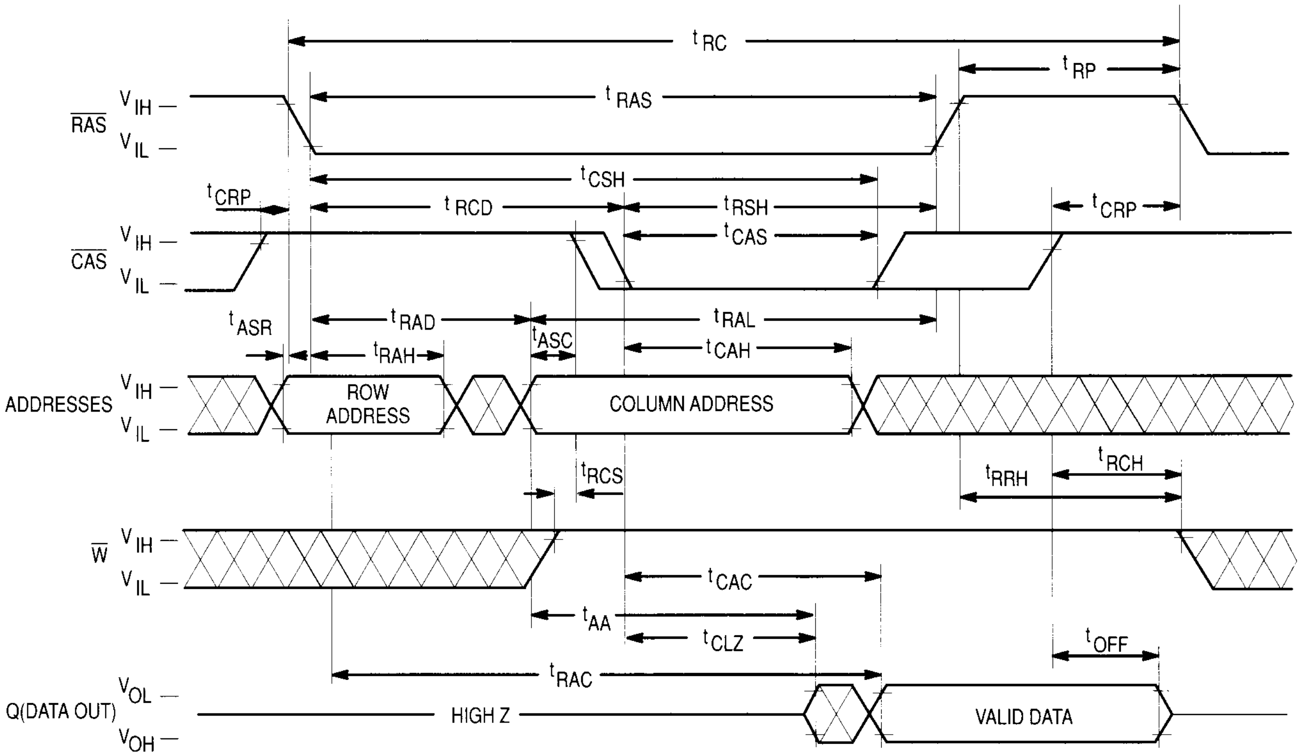
READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		514101A-60		514101A-70		514101A-80		514101A-10		Unit	Notes
	Std.	Alt.	Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	115	—	135	—	155	—	185	—	ns	5
Access Time from $\overline{\text{RAS}}$	t_{RELQV}	t_{RAC}	—	65	—	75	—	85	—	105	ns	6, 7
Access Time from $\overline{\text{CAS}}$	t_{CELQV}	t_{CAC}	—	25	—	25	—	25	—	30	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	35	—	40	—	45	—	55	ns	6, 9
$\overline{\text{RAS}}$ Pulse Width	t_{RELREH}	t_{RAS}	65	10 k	75	10 k	85	10 k	105	10 k	ns	
$\overline{\text{RAS}}$ Hold Time	t_{CELREH}	t_{RSH}	25	—	25	—	25	—	30	—	ns	
$\overline{\text{CAS}}$ Hold Time	t_{RELCEH}	t_{CSH}	65	—	75	—	85	—	105	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t_{CELCEH}	t_{CAS}	25	10 k	25	10 k	25	10 k	30	10 k	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t_{AVREH}	t_{RAL}	35	—	40	—	45	—	55	—	ns	

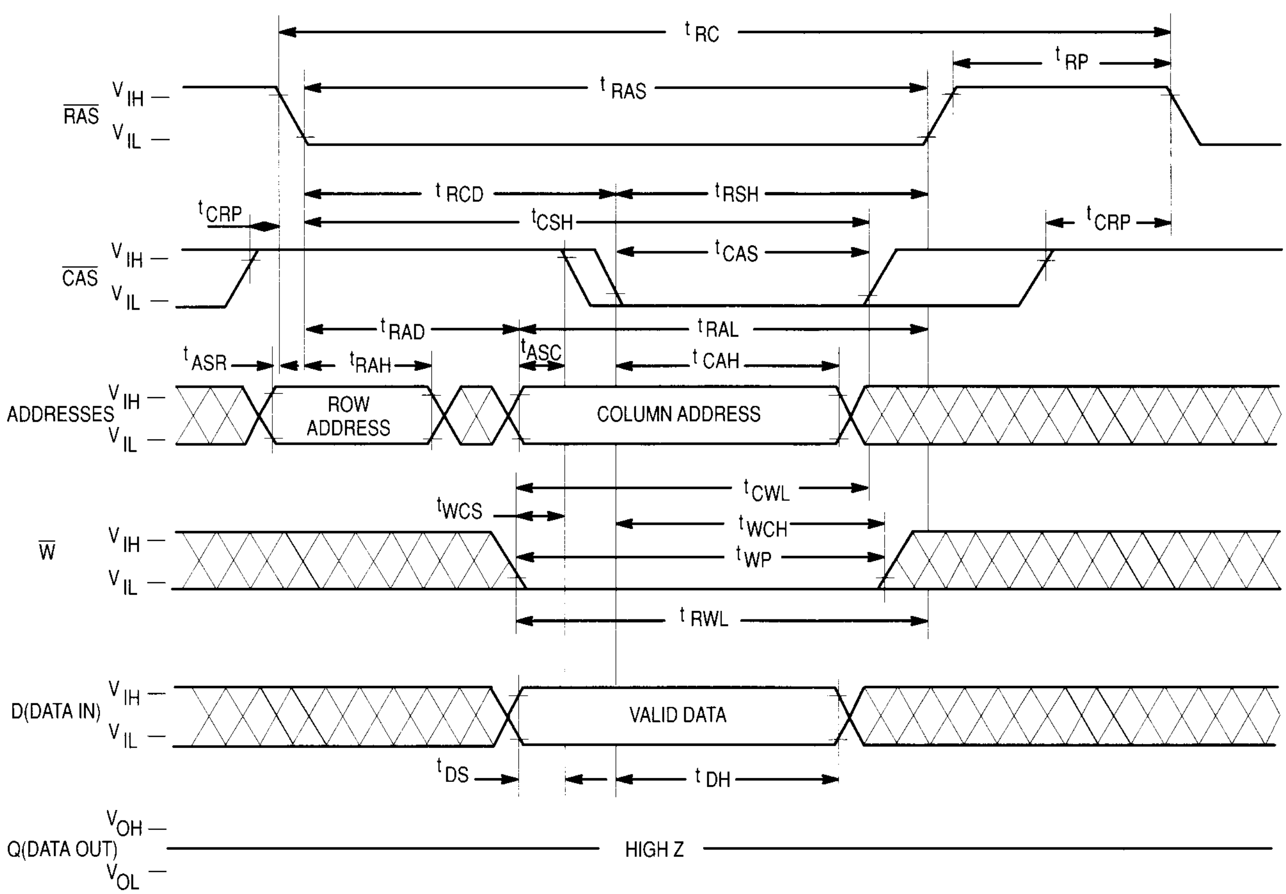
NOTES:

1. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power-up followed by 8 $\overline{\text{RAS}}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is ensured.
6. Measured with a current load equivalent to 2 TTL (–200 μA, +4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \le t_{RCD}$ (max).
8. Assumes that $t_{RCD} \ge t_{RCD}$ (max).
9. Assumes that $t_{RAD} \ge t_{RAD}$ (max).

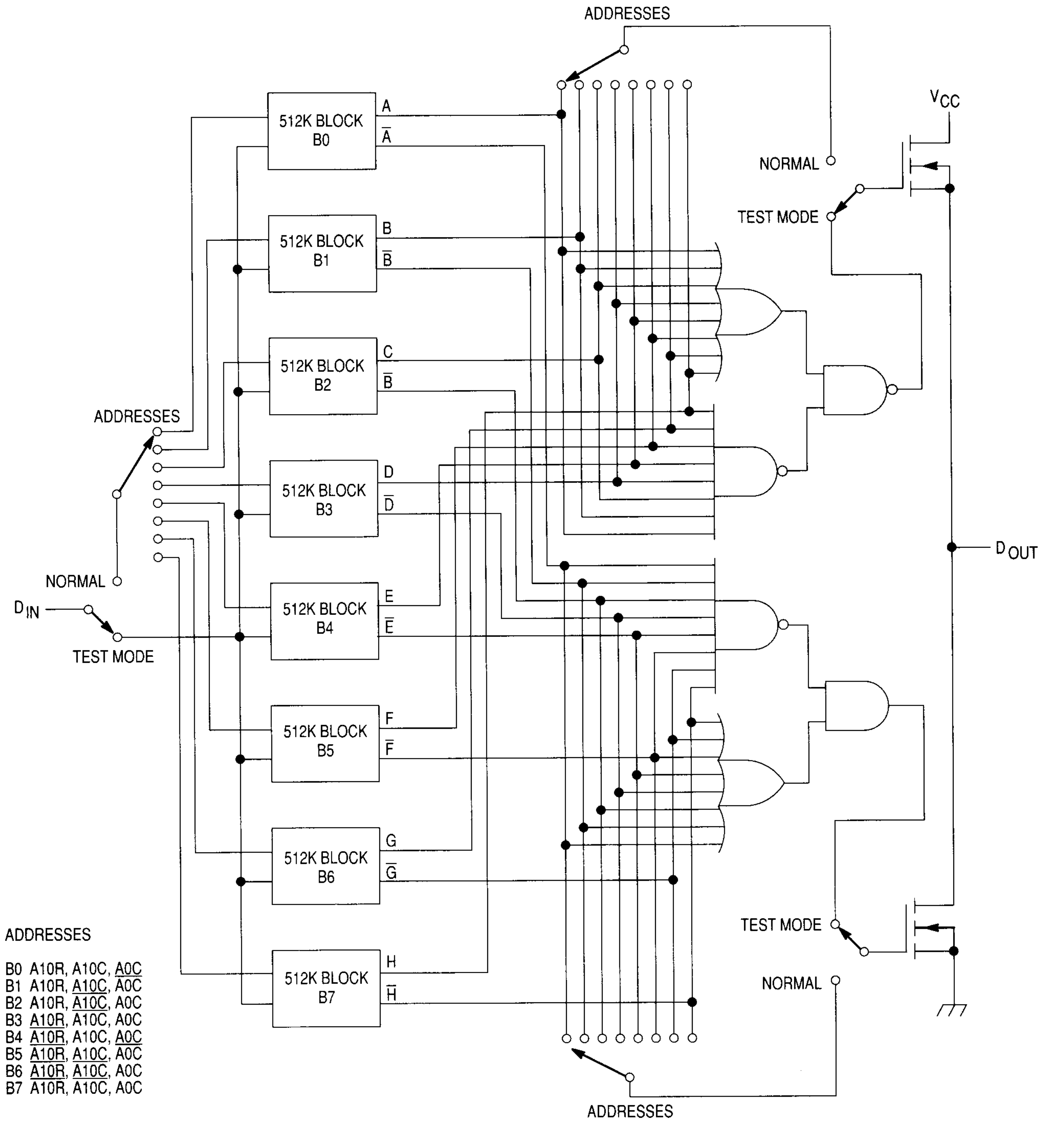
TEST MODE – READ CYCLE



TEST MODE – EARLY WRITE CYCLE



TEST MODE BLOCK DIAGRAM



ORDERING INFORMATION
(Order by Full Part Number)

MCM 514101A X XX XX

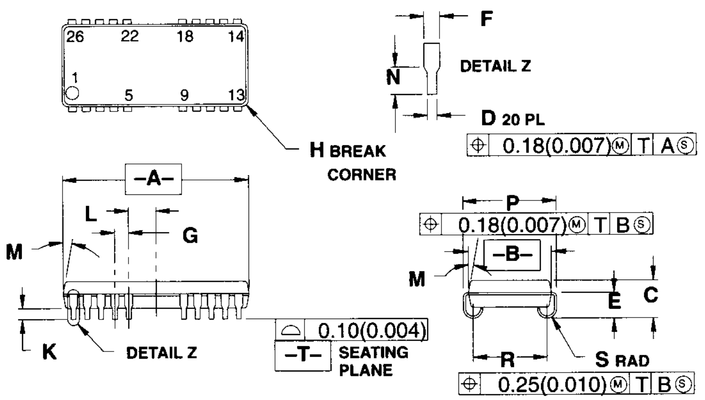
- Motorola Memory Prefix — MCM
- Part Number — 514101A
- Package (NJ = 300 mil SOJ, J = 350 mil SOJ Z = 100 mil Plastic ZIP) — X
- Speed (60 = 60 ns, 70 = 70 ns, 80 = 80 ns, 10 = 100 ns) — XX
- Shipping Method (R2 = Tape & Reel, Blank = Rails) — XX

Full Part Numbers—

MCM514101ANJ60	MCM514101ANJ60R2	MCM514101AZ60
MCM514101ANJ70	MCM514101ANJ70R2	MCM514101AZ70
MCM514101ANJ80	MCM514101ANJ80R2	MCM514101AZ80
MCM514101ANJ10	MCM514101ANJ10R2	MCM514101AZ10
MCM514101AJ60	MCM514101AJ60R2	
MCM514101AJ70	MCM514101AJ70R2	
MCM514101AJ80	MCM514101AJ80R2	
MCM514101AJ10	MCM514101AJ10R2	

PACKAGE DIMENSIONS

NJ PACKAGE
300 MIL SOJ
CASE 822-03

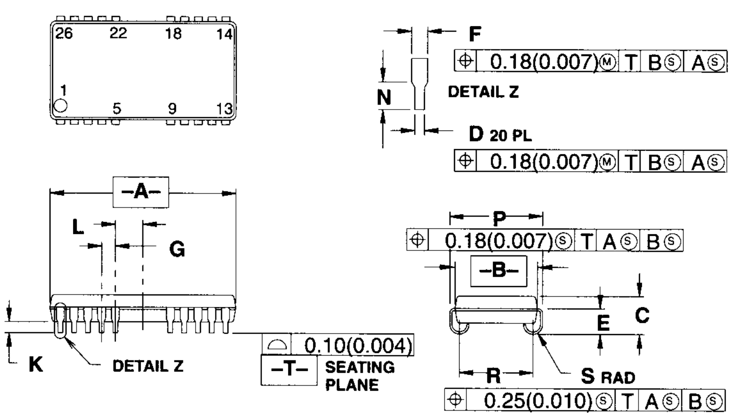


1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION A & B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15(0.006) PER SIDE.
4. DIM R TO BE DETERMINED AT DATUM –T–.
5. FOR LEAD IDENTIFICATION PURPOSES, PIN POSITIONS 6,7,8,19,20, & 21 ARE NOT USED.
6. 822–01 AND –02 OBSOLETE, NEW STANDARD 822–03.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	17.02	17.27	0.670	0.680
B	7.50	7.74	0.295	0.305
C	3.26	3.75	0.128	0.148
D	0.39	0.50	0.015	0.020
E	2.24	2.48	0.088	0.098
F	0.67	0.81	0.026	0.032
G	1.27 BSC		0.050 BSC	
H	—	0.50	—	0.020
K	0.89	1.14	0.035	0.045
L	2.54 BSC		0.100 BSC	
M	0°	10°	0°	10°
N	0.89	1.14	0.035	0.045
P	8.39	8.63	0.330	0.340
R	6.61	6.98	0.260	0.275
S	0.77	1.01	0.030	0.040

PACKAGE DIMENSIONS

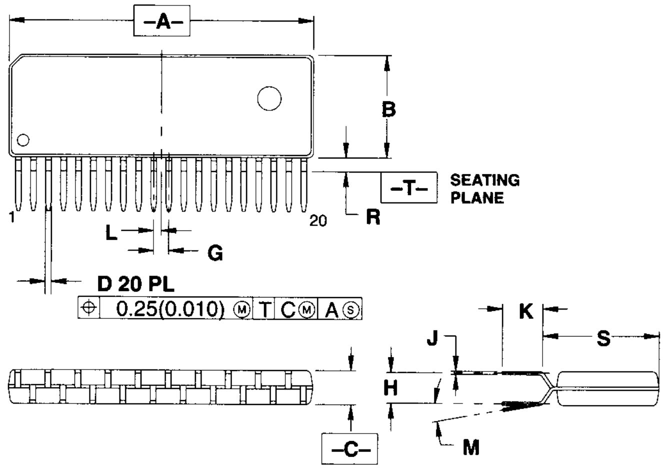
J PACKAGE
350 MIL SOJ
CASE 822A-01



1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION A & B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15(0.006) PER SIDE.
4. DIMENSION A & B INCLUDE MOLD MISMATCH AND ARE DETERMINED AT THE PARTING LINE.
5. DIM R TO BE DETERMINED AT DATUM -T-.
6. FOR LEAD IDENTIFICATION PURPOSES, PIN POSITIONS 6,7,8,19,20, & 21 ARE NOT USED.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	17.02	17.27	0.670	0.680
B	8.77	9.01	0.345	0.355
C	3.26	3.75	0.128	0.148
D	0.41	0.50	0.016	0.020
E	2.24	2.48	0.088	0.098
F	0.67	0.81	0.026	0.032
G	1.27 BSC		0.050 BSC	
K	0.64	—	0.025	—
L	2.54 BSC		0.100 BSC	
N	0.89	1.14	0.035	0.045
P	9.66	9.90	0.380	0.390
R	7.88	8.25	0.310	0.325
S	0.77	1.01	0.030	0.040

Z PACKAGE
ZIG-ZAG IN-LINE
CASE 836-02



1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSIONS A, B, AND S DO NOT INCLUDE MOLD PROTRUSION.
5. MOLD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25(0.010).
6. 836–01 OBSOLETE, NEW STANDARD 836–02.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	25.53	25.90	1.005	1.020
B	8.59	8.89	0.338	0.350
C	2.75	2.94	0.108	0.116
D	0.45	0.55	0.018	0.022
G	1.27 BSC		0.050 BSC	
H	2.44	2.64	0.097	0.103
J	0.23	0.33	0.009	0.013
K	3.18	3.55	0.125	0.140
L	0.64 BSC		0.025 BSC	
M	0°	4°	0°	4°
R	0.89	1.39	0.035	0.055
S	9.66	10.16	0.380	0.400