82506TC
TWISTED PAIR MEDIUM ATTACHMENT UNIT (TP MAU)

- **Complies with IEEE 802.3 10BASE-T Standard for Twisted Pair Interface**
- **Conforms to IEEE 802.3 Standard for Attachment Unit Interface (AUI)**
- **Direct Interface to AUI and Twisted Pair Isolation Transformers**
- **On-Chip Line Drivers and Receivers**
- **LED Drivers for Transmit, Receive, Collision, Jabber and Polarity Status**
- **Generates Internal Predistortion Signal**
- **Selectable Polarity Switching**
- **Resetable Jabber Function**
- **Selectable Link Integrity (LI) Function**
- **Selectable Signal Quality Error (SQE) Function**
- **Low-Power CMOS Technology**
- **Single 5-V Supply**
- **28-Lead Plastic DIP and SOJ Packages**

(See Packaging Spec Order No. 240800-001, Package Type P and PE)

The 82506TC Twisted Pair Medium Attachment Unit (TP MAU) is intended for local area network (LAN) designs that interface the IEEE 802.3-1988 AUI cable to the twisted pair wire (10BASE-T). It offers LAN designers a cost-effective, integrated solution to the problem of upgrading existing standard Ethernet* networks to twisted pair. The 82506TC complies with IEEE 802.3 AUI specifications and IEEE 802.3 10BASE-T specifications. The device incorporates the interface circuitry and both the AUI and twisted pair line drivers and receivers in a low-power CMOS package. The 82506TC TP MAU internally generates predistortion signals to eliminate line overcharge and improve jitter performance. It provides selectable 10BASE-T features for simplified network management, including selectable signal quality error (SQE) test, link integrity test, jabber protection and selectable polarity switching. In addition, the 82506TC TP MAU supports LED status indicators for transmit, receive, jabber, collision and receive polarity. It is fabricated using CMOS-process technology and is available in 28-lead plastic DIP and 28-lead SOJ packages.

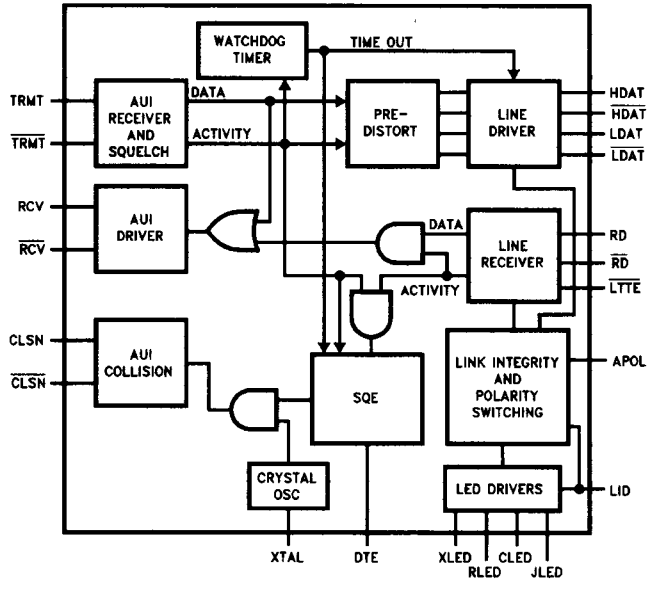


Figure 1. 82506TC TP MAU Block Diagram

Manufactured and tested for Intel by AT&T in accordance with AT&T internal standards.

*Ethernet is a registered trademark of Xerox Corporation.

November 1992
Order Number: 290260-004

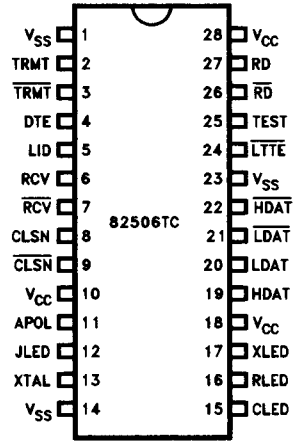


Figure 2. 82506TC Pinout

TABLE 1. 82506TC Pinout Description

Symbol	Pin No.	Type	Name and Function
V_{SS}	1	—	**Analog Ground.**
TRMT, $\overline{TRMT}$	2, 3	I	**Transmit Data.** A differentially driven input tied to the D0 pair of the transceiver cable. The transmit pair of the transceiver cable supplies 10-Mb/s Manchester encoded data. These pins must be isolated with a pulse transformer. End of Packet (EOP) is detected when a positive transition has not occurred for 200 ns.
DTE	4	I	**Data Terminal Equipment.** When this pin is tied high (V_{CC}) a SQE-test signal is generated at the end of each packet (as required for DTE applications). When DTE is tied low (V_{SS}) the SQE test is disabled, but the collision circuit remains enabled for use in repeater applications. When the DTE is floated, an internal pull-up biases the signal high.
LID	5	I	**Link Integrity Disable.** When this pin is tied high (V_{CC}), the link integrity function of the TPMAU is disabled. When link integrity is enabled, the receive traffic indicator remains on when the receive twisted pair link is present.
RCV, $\overline{RCV}$	6, 7	O	**Receive Data Pair.** A differential output pair that drives the DI pair of the AUI cable with 10-Mb/s Manchester encoded data. These pins must be isolated from the AUI transceiver cable with a pulse transformer.
CLSN, $\overline{CLSN}$	8, 9	O	**Collision Presence Pair.** A differential output pair that drives the CI pair of the AUI cable with a 10-MHz (± 15%) signal when simultaneous activity exists on the TRMT and RD pairs. These pins must be isolated from the AUI-transceiver cable with a pulse transformer.
V_{CC}	10	—	**Power.** Digital, 5 V.

TABLE 1. 82506TC Pinout Description (Continued)

Symbol	Pin No.	Type	Name and Function
APOL	11	I/O	**Automatic Polarity Switching Enable.** This is a dual-function pin which determines if the automatic polarity switching function should be enabled. The function is enabled if the pin is HIGH and is disabled if the pin is LOW, thus backwards compatible with the 82506TB. The pin is also capable of driving an LED if the function is enabled.
JLED	12	O	**Jabber Indicator.** Indicates that the watchdog timer has timed out and the twisted pair drivers have been disabled.
XTAL	13	I	**Crystal In.** A 20-MHz clock input. This signal can be driven by a 20-MHz, parallel-resonant crystal or a MOS level clock with a 60/40 duty cycle.
V_{SS}	14	I	**Ground.** For XTAL (Pin 13) and indicator output drivers.
CLED	15	O	**Collision Indicator.** Indicates that a collision has been detected by the TP medium attachment unit.
RLED	16	O	**Receive Indicator.** Indicates that a reception from the network is in progress.
XLED	17	O	**Transmit Indicator.** Indicates that a transmission onto the network is in progress.
V_{CC}	18	—	**Power.** 5 V.
HDAT, $\overline{\text{HDAT}}$ LDAT, $\overline{\text{LDAT}}$	19, 22 20, 21	O	**TP Transmit Pair Drivers.** These four outputs constitute the twisted-pair drivers, which have predistortion capabilities. The HDAT/$\overline{\text{HDAT}}$ outputs generate the 10-Mb/s Manchester encoded data. The LDAT/$\overline{\text{LDAT}}$ outputs mirror the HDAT/$\overline{\text{HDAT}}$ outputs except for "fat" bit occurrences. During the second half of a "fat" bit (either high or low), the LDAT/$\overline{\text{LDAT}}$ outputs are inverted with respect to HDAT/$\overline{\text{HDAT}}$ outputs. This signal behavior reduces the amount of jitter by preventing overcharge on the twisted-pair medium.
$\overline{\text{LTTE}}$	24	I	**Lower TP Threshold Enable (Active Low).** For 10BASE-T compatible operation this pin must be tied high. But, if this pin is grounded, the TP receiver threshold is lowered by approximately 4.5 db from the nominal 10BASE-T required specification. By using this lower-threshold option and by selecting different compensation resistor values for wave-construction circuits, a customized interface is possible for non-10BASE-T applications. However, once this lower threshold is invoked, the wiring used must not be a bundled system (e.g., 25 pair) where other services reside (e.g., voice, other 10BASE-T users, etc.).
TEST	25	I	**Test.** This pin is used for testing; it should be connected to V_{SS} during normal operation.
$\overline{\text{RD}}$, RD	26, 27	I	**TP Receive Pair.** The differential twisted pair receiver. The receive pair is connected to the twisted pair medium and is driven with 10-Mb/s Manchester encoded data.
V_{CC}	28	—	**Analog Power.** 5 V.

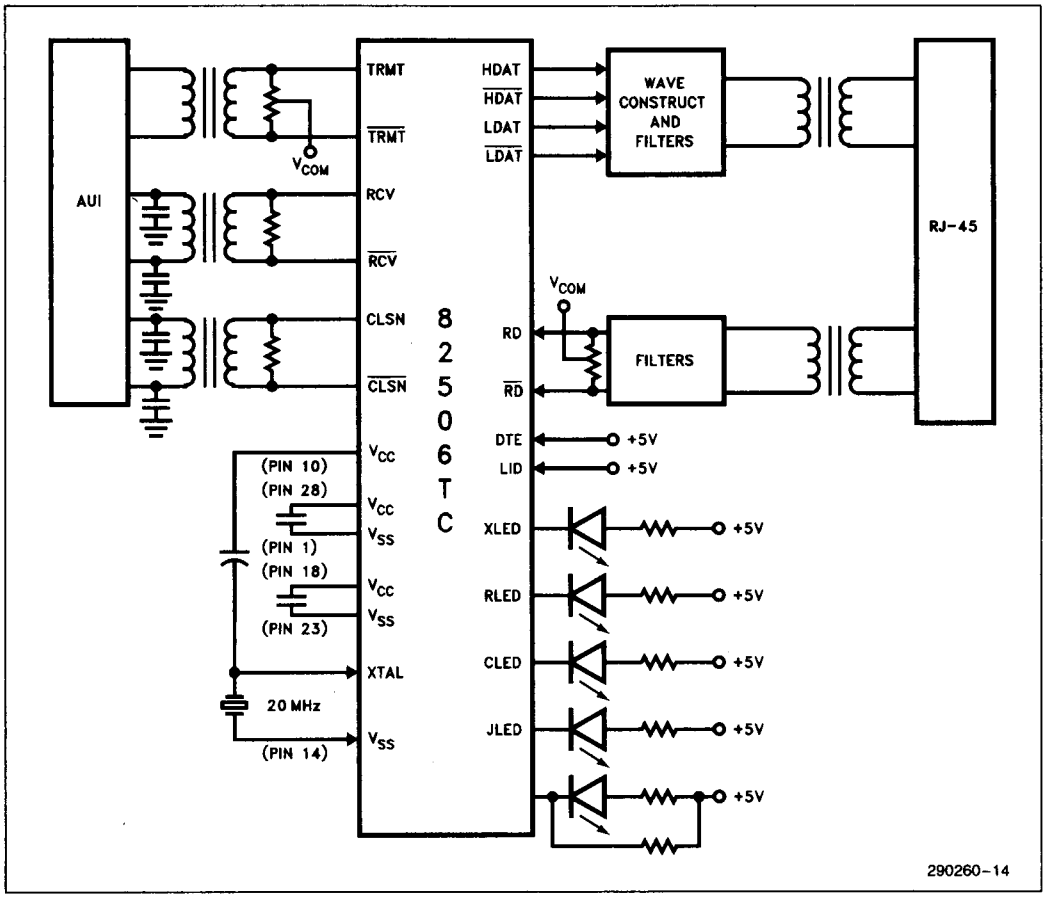
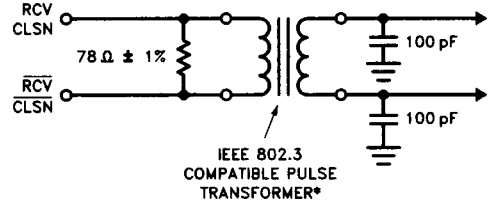


Figure 3. Typical System Configuration



*Required transformers are the Pulse Engineering Inc. (PE64503), TDK Corp. (TLA-100-3E), Coilcraft (LAXET304 or LO323-A), or equivalents.

Figure 4. Typical Load Output on the Outputs of RCV/$\overline{\text{RCV}}$ and CLSN/$\overline{\text{CLSN}}$

FUNCTIONAL DESCRIPTION

Overview

The 82506TC provides the transmit, receive, and collision detection functions specified by the IEEE 802.3 10BASE-T specification for a 10-Mb/s, CSMA/CD, twisted-pair Ethernet. The 82506TC is used as the interface between the attachment unit interface (AUI) signals and the twisted pair. Three strapping options are available.

- **Link Integrity Disable (LID).** When the LID strapping option is enabled (driven high), the link integrity function is disabled. When driven low, link pulses are transmitted on the twisted pair medium in the absence of data transmissions. In addition, the receiver expects to see link pulses in the absence of receive data. If no receive data or link pulses are received within 100 ms ± 50 ms the 82506TC will enter a link fail state. When LID is floated an internal pull-up biases the signal high.
- **Data Terminal Equipment (DTE).** When the DTE strapping option is enabled (driven high) the SQE test sequence is transmitted to the DTE after every successful transmission on the twisted pair network.
- **Automatic Polarity Switching Enable (APOL).** When the APOL strapping option is enabled (driven HIGH), the polarity of the receive twisted pair wire will be corrected if it has been accidentally reversed. When this function is enabled, it is also capable of driving an LED to indicate the status of the polarity of the receive twisted pair.

The 82506TC simplifies network management and troubleshooting by providing five status indicator LED drivers that monitor traffic on a node and report transmit, receive, collision, jabber conditions, and receive polarity status.

Figure 3 is an example of a typical system configuration.

Transmit Path (AUI to TP)

The transmit portion of this component transfers data from the AUI to the twisted-pair analog filters. It also loops back the data to the RCV pair.

- **AUI Receiver.** The TP MAU receives transmit data from the data terminal equipment on the transmit pins(TRMT/$\overline{\text{TRMT}}$) of the AUI-DO circuit (as defined by the IEEE802.3-1988 specification). The 82506TC then transmits the data onto the twisted-pair cable via the twisted-pair drivers. The AUI transmit inputs must be transformer coupled to the TRMT/$\overline{\text{TRMT}}$ pins. For best operation, the AUI signal should be dc biased to a common mode voltage of $V_{CC}/2$.

  The squelch circuit rejects (filters) all signals with an amplitude less than 160 mV or a pulse width less than 20 ns. A signal with an amplitude greater than 300 mV and a pulse width greater than 75 ns is accepted and turns off the squelch filter.

The squelch filter remains off until an IDL pulse is detected or until the input does not exceed the detection threshold for 500 ±100 ns.

- **AUI Receive Signal Levels.** The receiver (TRMT/$\overline{\text{TRMT}}$) is able to recognize differential signals as small as 300-mV peak. Internal circuitry samples the common mode voltage to provide full differential signal detection.
- **TP Driver Characteristics.** The drivers (HDAT/$\overline{\text{HDAT}}$ and LDAT/$\overline{\text{LDAT}}$) output CMOS logic levels with a source resistance less than 10 Ω and maximum current rating of 25 mA dc. All TP output driver pins are driven low as a result of any of the following.
  - Reception of an IDL signal.
  - A jabber condition is detected.
  - Activation of a link failure.
  - TRMT pair input fails to cross the detection threshold for 500 ± 100 ns.

When the driver detects the end of an IDL pulse on the TRMT pair, a timer of not more than 5 bit times (BT) is started. Activity on the TRMT pair is ignored until this timer expires.

Receive Path (TP to AUI)

When a RD signal is present, the receive circuit of the 82506TC transfers data from the RD pair input to the RCV pair output.

- **AUI Driver Characteristics.** This driver differentially drives a current onto the load connected between the RCV and $\overline{\text{RCV}}$ pins. The current through the load results in an output voltage between ±0.6 V and ±1.2 V measured differentially between the two pins. An external resistor (78 Ω) and capacitor (100 pF) must be connected for proper termination, as shown in Figure 4. This output is in accordance with the IEEE Spec 802.3 Sec.7.4.1 for MAUs. When the driver detects that it has finished sending an IDL pulse to the AUI it starts a timer of not more than 5 BT. Activity on the RD pair is ignored when this timer is functioning.
- **TP Receiver Threshold.** The TP receiver is connected to the output of a band limiting filter. The filter's input is transformer coupled to the twisted pair. The receiver is able to recognize differential signals as small as 350 mV peak. An external biasing circuit must provide a common mode volt-

age of $V_{CC}/2$. The differential input impedance of the RD pair is 20 kΩ ± 20%. Internal circuitry generates a dual-level bias voltage to determine proper signal level thresholds and prevent reception of spurious signals from the network (this is similar to a squelch function).

When the signal level at the RD input falls below −500 mV, with respect to the common mode voltage ± 10%, the data path is activated and the received signal is passed to the AUI cable. At the beginning of a reception the bias level at the RD input is reduced to −350 mV with respect to the common mode voltage ± 10%

Collision

The collision detection portion of the 82506TC senses the simultaneous presence of data on the TRMT and RD pins. It reacts by transmitting a 10-MHz square wave on the CLSN pair of the AUI cable. This signal is a periodic waveform of 10 MHz ± 15%, with a duty cycle no worse than 40/60 or 60/40. It is transmitted within 9 bit times after the component detects a collision (as specified by the 10BASE-T Standard, Sec.14.2.1.3). If the receive pair becomes active while the transmit pair is active, the loopback data on the RCV pair switches from transmit data to receive data within 13 ± 3 BT from the assertion of the CLSN pair. If the RD pair goes active while the TRMT pair is active a collision condition will be detected and the SQE will continue for 7 ± 2 BT. If a collision condition exists where the TRMT pair has gone idle while the RD pair is still active, SQE can continue for up to 9 BT.

The collision AUI driver differentially drives a signal onto the load connected between the CLSN pair.

This driver differentially drives a current onto the load connected between the CLSN and $\overline{\text{CLSN}}$ pins. The current through the load results in an output voltage between ±0.6 V and ±1.2 V measured differentially between the two pins. An external resistor (78 Ω) and capacitor (100 pF) must be connected for proper termination, as shown in Figure 4. The output is in accordance with IEEE 802.3-1988 Sec. 7.4.1 for the AUI.

Jabber (Watchdog Timer)

The 82506TC supports a self-interrupt function that protects the network from a jabbering node (i.e., continuous transmission). The component provides a nominal window of 50 ms during the time a normal data link frame can be transmitted. If the frame length exceeds this duration, the component immediately inhibits all further transmission of that frame and activates the CLSN pair (as specified by IEEE 802.3-1988 Sec. 8.2.1.5). When activity on the TRMT pair has ceased, the component continues to present the CSO signal to the CLSN pair for 0.5 s ± 50%. The component then resets itself and returns to the idle state (as specified by the 10BASE-T Standard, Sec. 14.2.1.5). The transmission of link integrity pulses from the TP drivers is not inhibited when the TP MAU jabber is activated and link integrity is enabled.

SQE Test (Heartbeat)

The SQE test begins within 11 ± 5 bit times after the TRMT pair detects the IDL signal. The SQE test duration is 10 ± 5 bit times. When the AUI-DO circuit has gone idle after a successful transmission (without a collision), and the DTE input is high, the 82506TC activates the CLSN pair to simulate a collision.

Link Integrity

The link integrity function determines if the receive twisted-pair link is faulty. Enabling the function (LID tied to V_{SS}) causes the RLED receive traffic indicator to display the status of the receive twisted-pair link. The link integrity function permits the active disabling of the transmit and loopback paths within the TP MAU component in response to a link integrity fault. The link integrity function monitors the RD pair for either data or link test pulses by providing a 100 ms ± 50 ms window during which data or a link test pulse is expected. If this timer expires and the LID is off, the RLED indicator is turned off and the component's transmit and loopback capabilities are disabled. The 82506TC remains in a link fail state until after a data packet is received, or until after a sequence of consecutive link test pulses are received. The sequence length is between two and ten pulses. If a pulse or receive traffic is detected within this window, the timer is reset and the RLED indicator remains on.

The TP MAU also transmits link test pulses onto the transmit twisted pair link when link integrity is enabled. In the absence of transmit traffic, a link test pulse is transmitted at a nominal rate of one pulse each 16 ms ± 8 ms. If the link integrity is disabled, the RLED indicator remains on in the absence of receive traffic, (data and link pulses). Received link test pulses are also ignored at the RD pair input.

Automatic Polarity Switching

The most common fault in twisted pair wiring is reversed polarity. The 82506TC detects polarity faults and internally corrects the polarity when it senses a polarity fault on the twisted pair wire. This au-

tomatic polarity switching function is defeatable by connecting the APOL pin to ground. When enabled, the APOL pin is capable of driving an LED to indicate the status of the polarity. If the receive polarity is correct, the pin is allowed to float HIGH to keep the LED off. If the function is enabled and the receive polarity is incorrect, the pin is driven LOW to light up the LED. Figure 5 shows the connection of APOL pin to the LED.

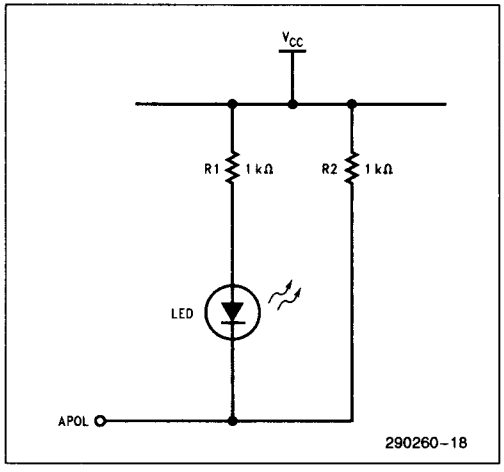


Figure 5. Connection of LED to APOL Pin

LED Status

Five light-emitting diodes (LEDs) give the user a visual indication of the MAU's status. The 82506TC provides the logic signals needed to drive the LEDs.

- **XLED.** The following LED values (on or off) are used to indicate transmission (AUI) status.
  - The LED is normally on, which indicates no transmission is in progress.
  - The LED is off when a valid packet is transmitted. The duration of the off period is 100 ms ±10 ms. The minimum duration of the on period is 4 ms while waiting for next valid packet transmission.
- **RLED**—With LID Disabled. The following LED values (on or off) are used to indicate reception (TP) status.
  - The LED is normally on, which indicates there is no receive traffic.
  - The LED is off when a valid packet is received. The duration of the off period is 100 ms ±10 ms. The minimum duration of the on period is 4 ms while waiting for next valid packet receive.
- **RLED**—With LID Enabled. The following LED values (on or off) are used to indicate reception (TP) status.
  - The LED is normally on, which indicates no receive traffic and successful reception of the link test pulse.
  - The LED turns off if no receive traffic or link integrity signals have been received for more than 0.5 s. This visually indicates a failure of a link segment. The LED remains off until a link test pulse, or receive traffic, is successfully detected, after which the LED is turned on with a minimum on time of 0.5 s.
  - If the link is working, the LED will be turned off when a valid data packet is received from the twisted pair. When a packet is received, the LED is turned off for a duration of 100 ms ±10 ms, then the LED is turned back on.
  - The LED remains on for a minimum of 4 ms; it is turned off when the next packet is received.
- **CLED.** The following LED values indicate collision status.
  - The LED is normally off, which indicates no collision.
  - The LED is turned on when a collision is detected. It remains on for a nominal time of 15 ms ±5 ms, after which it is turned off.
  - The LED may be turned back on immediately upon detection of another collision. There is no minimum off time.
  - If a collision occurs while the LED is on, the LED remains on for the nominal time following the last detected collision.
- **JLED.** The following LED values indicate the jabber status.
  - The LED is normally off, which indicates a no jabber condition.
  - The LED is turned on when the watchdog timer times out, and the TP drivers are disabled. It remains on until the jabber condition is corrected.
  - The LED is turned off after the watchdog timer counts out the 0.5 s ±0.25 s reset time.
- **APOL.** When enabled, the APOL pin is capable of driving an LED to indicate the following polarity status:
  - The LED is off to indicate the receive polarity is correct.
  - The LED is turned on to indicate the receive polarity is incorrect.

LED Drivers

The typical LED circuit consists of an external resistor in series with the LED and connected the V_{CC}. The LED driver pulls the pin low to turn the LED on. Each LED driver can sink up to 15 mA of current, with an output impedance of less than 50 Ω.

Clock Generation

A 20-MHz, parallel-resonant crystal is used to control the clock generation oscillator of the TP MAU. We recommend that the crystal meet the following specifications.

- Quartz crystal
- 20 MHz ± 0.01%
- Parallel resonant with a 20-pF load fundamental mode with a maximum series resistance of 25 Ω.

The crystal shunt and external capacitance should be less than 10 pF. The crystal should be connected adjacent to the 82506TC to the XTAL and V_{SS} pins. The crystal shunt capacitance (CO) should not exceed 5 pF. Two crystals from two different manufacturers are included. Refer to Table 1 and 2 for more information.

An external MOS-level clock can be applied to the crystal oscillator input. A resistor should be added in series with the clock source to limit the amplitude of the voltage swing seen by the pin. A 500-Ω resistor works well in most cases. If users are concerned about the duty-cycle variation caused by driving the TPMAU with a clock source, the following test can be done on the bench to empirically determine the best resistor value for the user's application.

- Place the part in dc test mode, as described in the Test Mode section of this document.
- Attach an oscilloscope to the JLED pin. This pin outputs the internal clock source.
- Alter the resistor value to obtain an optimal duty-cycle ratio. Experiments have shown that a 500-Ω resistor works well for LS TTL logic levels; CMOS logic levels need a 1-kΩ resistor.

Under no circumstances should the clock be driven straight into the TPMAU. Also, under no circumstances should the clock stop, not even briefly, once power is applied to the TPMAU. If the clock to the TPMAU is stopped, power to the TPMAU must be removed to ensure proper behavior of the TPMAU.

Strapping Options

All strapping options are connected to internal pull-up resistors, (nominally 100 kΩ). A resistor tying a strapping option low must be able to sink 70 μA.

Test Mode

The 82506TC enters the ac or dc test mode when the test pin (TEST) is held high. The ac test mode is activated by also holding the DTE pin high; the internal clock speeds are increased by three to reduce the ac test time. The dc test is activated by holding the DTE pin low while TEST is held high. During the dc test the oscillator frequency and duty cycle can be tested on the JLED pin and the three internal clocks (ACK, BCK, and CCK) can be tested on the XLED, RLED,and CLED pins respectively. The AUI driver current can be measured with a 39-Ω resistor between the receive pair pins.

Table 1. Components Information

Vendor	P/N	Description	Pkg	Verified
Valor Electronics	ST3984	TPE Filter/Transformer	SM	Yes
Valor Electronics	PT3877	TPE Filter/Transformer	TH	Yes
Valor Electronics	ST3934	TPE Common Mode Choke	SM	Yes
Valor Electronics	PT3868	TPE Common Mode Choke	TH	Yes
Fil-Mag	78Z1100D	TPE Filter	SM	Yes
Fil-Mag	78Z1100B	TPE Filter	TH	Yes
Fil-Mag	23Z114SM	TPE Transformer	SM	Yes
Fil-Mag	23Z114	TPE Transformer	TH	Yes
Fil-Mag	23Z81SM	TPE Common Mode Choke	SM	Yes
Fil-Mag	23Z81	TPE Common Mode Choke	TH	Yes
Valor Electronics	ST6031	AUI Transformer	SM	No
Valor Electronics	LT1500	AUI Transformer	TH	Yes
Pulse Engineering	PE65723	AUI Transformer	SM	No
Pulse Engineering	PE64102	AUI Transformer	TH	Yes
Crystek Corp.	013212	20 MHz Crystal	HC49	Yes
M-Tron Industries	463-000	20 MHz Crystal	HC49	Yes

NOTE:
TH = Through Hole
SM = Surface Mount

Table 2. Vendor Information

Company	Telephone	Fax
Valor Electronics, 6275 Nancy Ridge Dr., San Diego, CA 92121	(619) 458-1471	(619) 458-0875
Fil-Mag, 4787 Cardin St., San Diego, CA 92111	(619) 569-6577	(619) 569-6073
Pulse Engineering, P.O. Box 12235, San Diego, CA 92112	(619) 268-2400	(619) 268-2515
CoilCraft, 1102 Silver Lake Rd., Cary, IL 60013	(708) 639-2361	(708) 639-1469
Crystek Corporation, 100 Crystal Dr., Ft. Myers, FL 33907	(813) 936-2109	(813) 939-4226
M-Tron Industries, Inc., P.O. Box 630, Yankton, SD 57078	(605) 665-9321	(605) 665-1709

Power Considerations

There are seven power connections to the TP MAU—three pairs of V_{CC} and V_{SS} connections and a fourth V_{SS} pin for the XTAL oscillator. Table 3 describes which internal circuits are powered by each V_{CC}/V_{SS} pair.

Table 3. Internal Circuit

Pin No.	Internal Circuits
1, 28	**Analog Supplies.** Analog signal receivers, energy detection circuits, delay lock loop, and band gap reference.
10, 14	**AUI Output Drivers.** Digital polycells, XTAL oscillator and LED drivers.
18, 23	TP CMOS output drivers only.

ELECTRICAL CHARACTERISTICS

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

Absolute Maximum Ratings

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

Ambient Operating Temperature (TA)	0 to +70°C
Storage Temperature	−40 to +125°C
All Output and Supply Voltages	−0.5 V to V_{CC} +0.5V
All Input Voltages	−0.5 V to V_{CC} +0.5V

1

DC Characteristics T_A = 0 to 70°C, V_{CC} = 5V ±5%

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{AID}	Input Differential Voltage (AUI)	0.300	1.3	V	
V_{TID}	Input Differential Voltage (TP)	0.350	2.0	V	
V_{XTL}	XTAL Input Low Voltage		0.4	V	
V_{XCH}	XTAL Input High Voltage	3.9		V	
V_{IL}	Input Low Voltage		0.4	V	
V_{IH}	Input High Voltage	2.4		V	
V_{AOD}	Output Differential Voltae (AUI)	0.600	1.2	V	
V_{TOL}	Output Voltage Low (TP)		0.1	V	V_{CC} = 5.0 V, R_L = 500 Ω
V_{TOH}	Output Voltage High (TP)	4.9		V	V_{CC} = 5.0 V, R_L = 500 Ω
V_{OL}	Output Voltage Low		0.13	V	V_{CC} = 5.0 V, R_L = 2000 Ω
V_{OH}	Output Voltage High	4.87		V	V_{CC} = 5.0 V, R_L = 2000 Ω
R_S	TP Driver Series Impedance		10	Ω	V_{CC} = 4.5 V, I = 25 mA (max)
I_{CC}	Power Supply Current with a Traffic Load		145	mA	V_{CC} = 5.00 V
PD	Power Dissipation with a Traffic Load		0.72	W	V_{CC} = 5.0 V

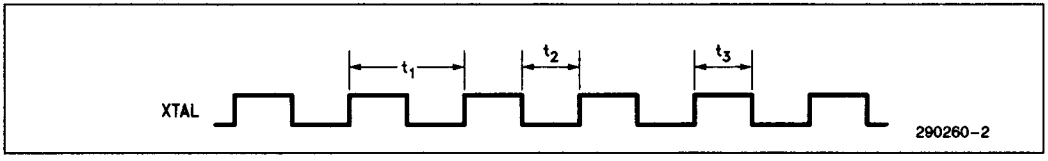
AC Timing Conditions

1. T_A = 0 to 70°C, V_{CC} = 5 V ± 5%.
2. Timing measurement points are 50% points unless otherwise noted.

Clock Timing

Symbol	Parameter	Min	Max	Units
t_1	XTAL (or Oscillator) Frequency	18	22	MHz
t_2	XTAL High and Low Times	22.5	27.5	ns

Clock Timing

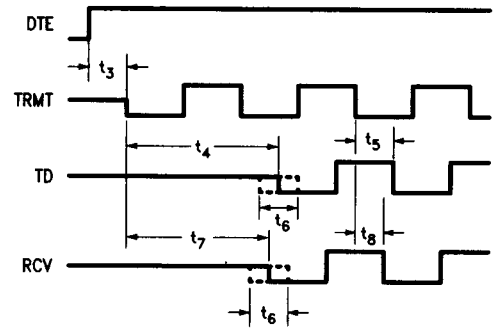


Transmit Timing

Symbol	Parameter	Min	Max	Units
t_3	DTE Setup and Hold Time to TRMT Pair Active	10	—	μs
t_4	Transmit Start-up Delay	0	2	bits
t_5	Transmit Steady State Delay	0	2	bits
t_6	Transmit Start-up Delay Variability	0	2	bits
t_7	Loopback Start-up Delay	0	5	bits
t_8	Loopback Steady State Delay	0	1	bits
t_9	TD* Held High at End of Packet	250	350	ns
t_{10}	Incremental Transmit Jitter	0	3.5	ns
t_{11}	TRMT Pair Return to Idle to SQE Test	600	1600	ns
t_{12}	SQE Test Duration	500	1500	ns

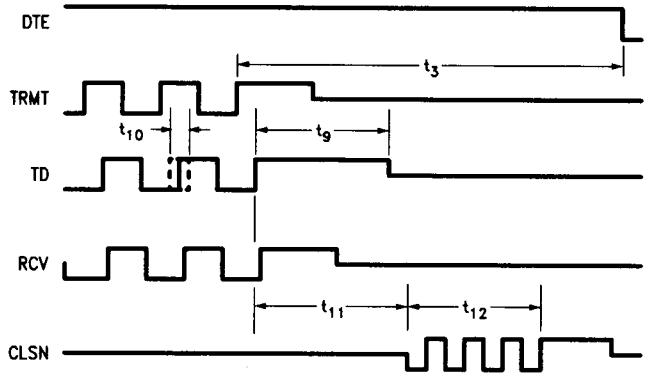
*TD represents the differential voltage between the signals HDAT and $\overline{\text{HDAT}}$

Transmit Timing: Start of Packet



290260-3

Transmit Timing: End of Packet

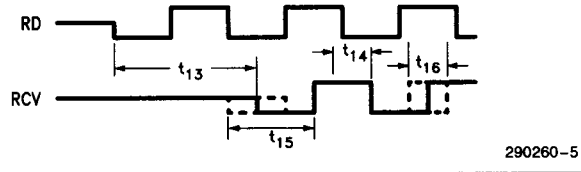


290260-4

Receive Timing

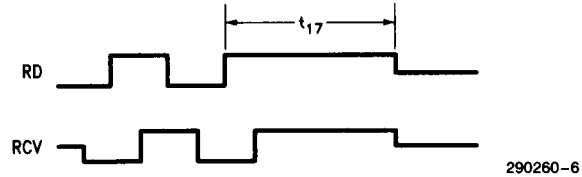
Symbol	Parameter	Min	Max	Units
t_{13}	Receive Start-up Delay	0	5	bits
t_{14}	Receive Steady State Delay	0	2	bits
t_{15}	Receive Start-up Delay Variability	0	2	bits
t_{16}	Incremental Receive Jitter	0	1.5	ns
t_{17}	RD Pair Held High at End of Packet	0	300	ns

Receive Timing: Start of Packet



290260-5

Receive Timing: End of Packet

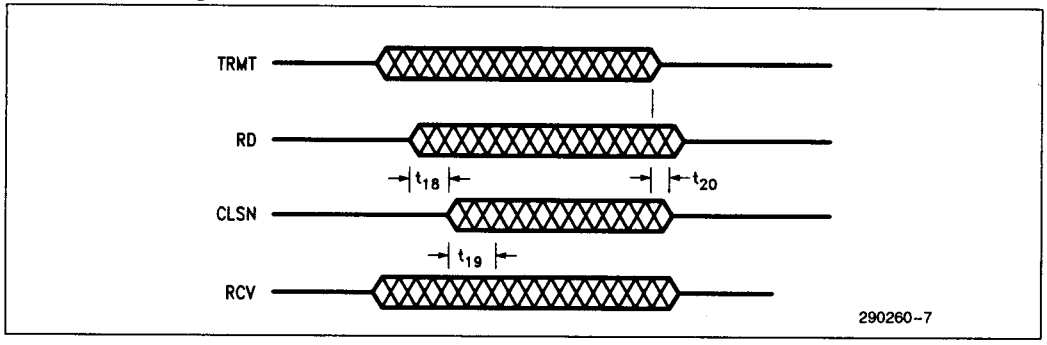


290260-6

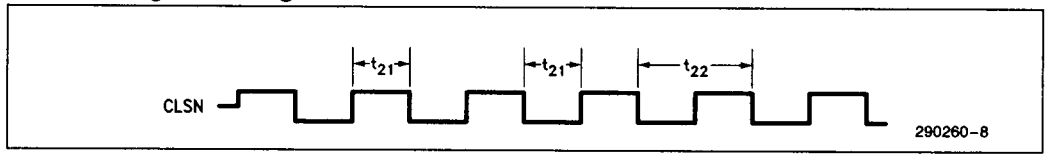
Collision Timing

Symbol	Parameter	Min	Max	Units
t_{18}	Onset of Collision to CLSN Pair Assertion	0	900	ns
t_{19}	RCV Pair Source to RD after CLSN Assert	0	900	ns
t_{20}	End of Collision to CLSN Pair Return to Idle	0	900	ns
t_{21}	CLSN Pair High/Low Time	40	60	ns
t_{22}	CLSN Pair Frequency	8.5	11.5	MHz

Collision Timing



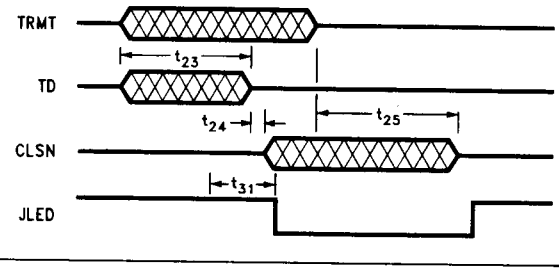
Collision Signal Timing



Jabber Protection Timing

Symbol	Parameter	Min	Max	Units
t_{23}	Assertion of TRMT Pair to Jabber Inhibit	45	55	ms
t_{24}	Jabber Inhibit to CLSN Assert	0	900	ns
t_{25}	TRMT Idle to Jabber Inhibit Removed	250	750	ms

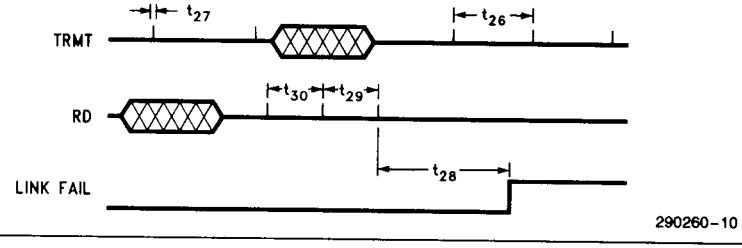
Jabber Protection Timing



Link Integrity Timing

Symbol	Parameter	Min	Max	Units
t_{26}	Last TRMT Pair Activity to Link Test Pulse	8	24	ms
t_{27}	Link Test Pulse Width	80	120	ns
t_{28}	Last RD Activity to Link Integrity Fault Assert	50	150	ms
t_{29}	Minimum Idle Time Between Consecutive Leakbeat Reception	6	8	ms
t_{30}	Maximum Idle Time Between Consecutive Leakbeat Reception	24	150	ms
t_{31}	JLED Turn-on Time	—	10	μs

Link Integrity Timing

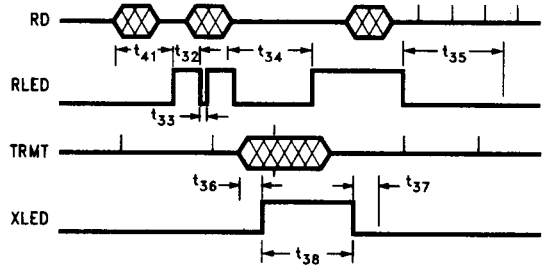


LED Timing

Symbol	Parameter	Min	Max	Units
t_{32}	RLED Fixed Off Time	90	110	ms
t_{33}	RLED Minimum on Time	4	8	ms
t_{34}	Last RD Activity to RLED Off (Link Integrity Fault)	50	150	ms
t_{35}	RLED Minimum On Time After Link Integrity Fault Correction	500	1500	ms
t_{36}	XLED Turnoff Time	—	10	μs
t_{37}	XLED Fixed Off Time	90	110	ms
t_{38}	XLED Minimum On Time	4	8	ms
t_{39}	CLED Turnoff Time	—	10	μs
t_{40}	CLED Nominal On Time	10	20	ms
t_{41}	RLED Turnoff Time	—	10	μs

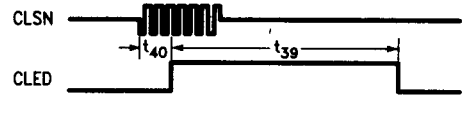
1

LED Timing: Transmit and Receive



290260-11

LED Timing: Collision

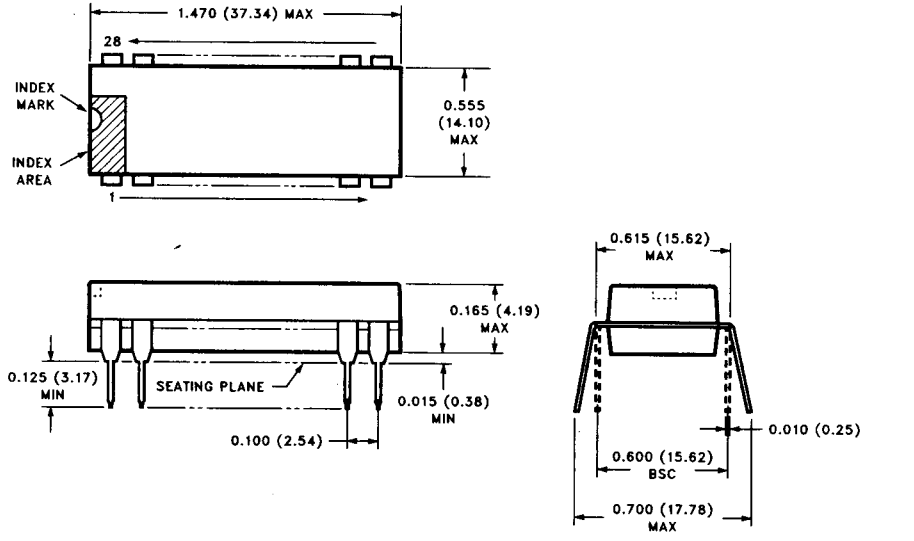


290260-12

Outline Diagrams

Dimensions are in inches and (millimeters).

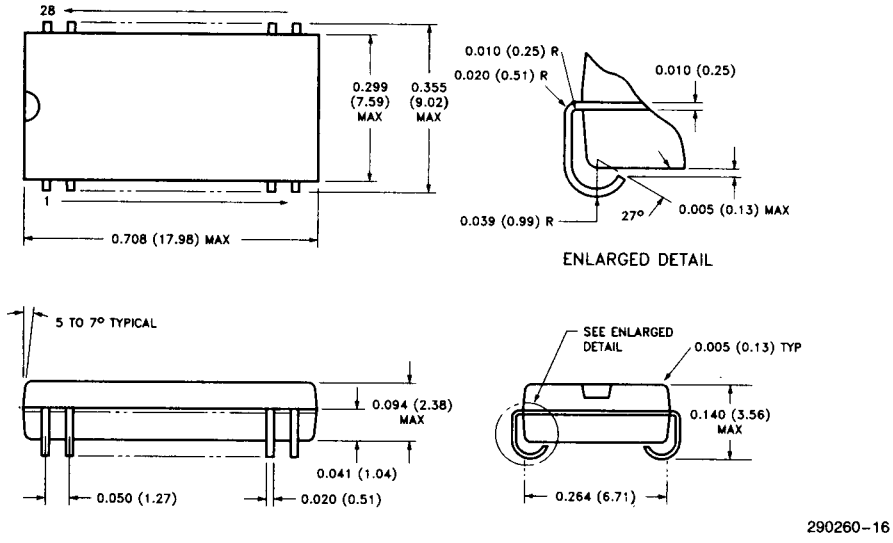
28-Pin, Plastic DIP



290260-15

NOTES:
Meets JEDEC standards.
Index mark may be a semicircular notch or circular dimple located in the index area.

28-Pin, Plastic SOJ
Dimensions are in inches and (millimeters)



NOTE:
Index mark may be a notch, dimple, or bevel.

REVISION SUMMARY

The following list are changes of the 82506TB to 82506TC.

- Polarity switching function added.
- LED driver (also an APOL pin) to indicate status of receive polarity.