SIEMENS

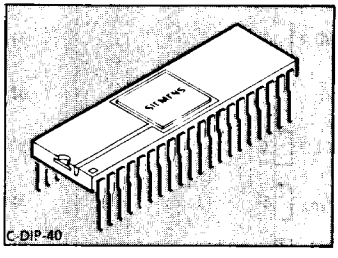
6-Bit A/D Converter, 300 MHz

SDA 8200

Features

Bipolar IC

- 300 MHz strobe frequency
- 5.4 effective bits (f_{analog} = 100 MHz)
- ± 0.25 LSB max. linearity error
- ± 1 V input voltage range
- 12 pF input capacitance
- Optionally 2:1 demultiplexed output data
- No pipelining in "Transparent Mode"
- Data ready clock output
- Overflow output



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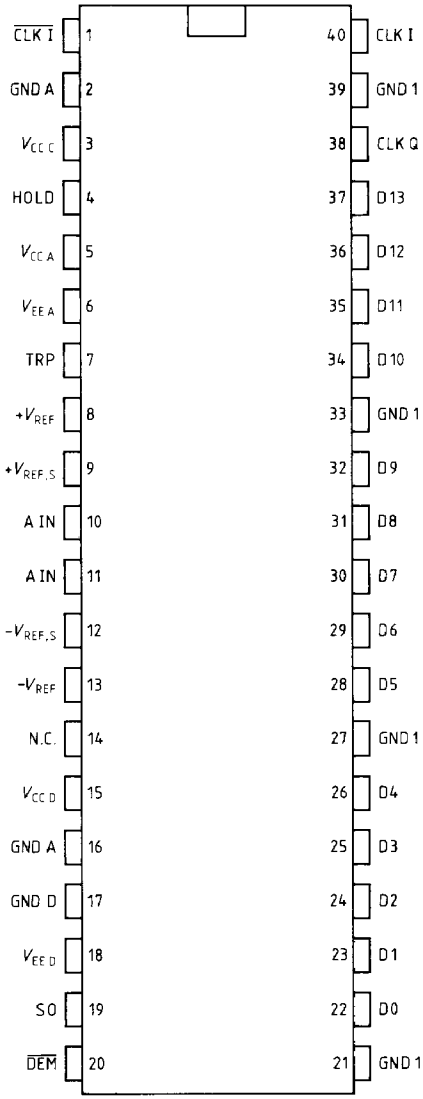
Type	Ordering Code	Package
SDA 8200	Q67000-A8164	C-DIP-40

The SDA 8200 is an ultrafast A/D converter operating according to the parallel principle with a resolution of 6 bits, a guaranteed clock frequency of 300 MHz and high performance up to 150 MHz full-scale input.

Figure 1
Pin Configuration
(top view)



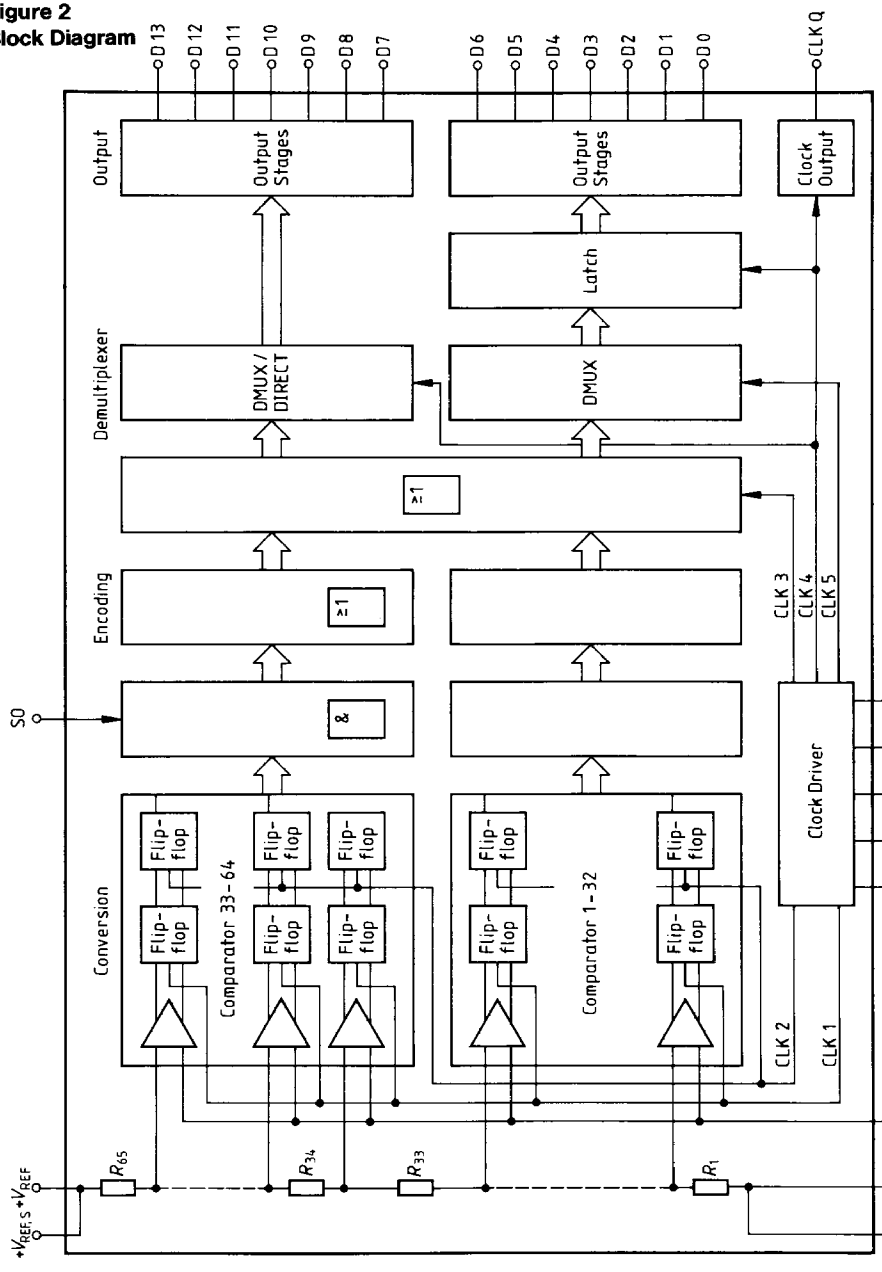
Pin Definitions and Functions

Pin	Name	Symbol	Function
10, 11	Analog input	A IN	Input for the signal to be digitalized. To lower parasitic inductance two pins are used for this input.
13, 12 8, 9	Reference inputs	$-V_{REF}$ $-V_{REF,S}$ $+V_{REF}$ $+V_{REF,S}$	Bottom and top of the reference-resistor string. The inputs may either be used as sense and force for a Kelvin connection or connected in parallel to minimize parasitic resistance.
40, 1	Conversion clock	CLK I, $\overline{\text{CLK I}}$	Every rising edge of a signal applied to CLK I initiates sampling of the analog signal. Either ECL (differential or single-ended) or sinewave clock inputs may be used.
38	Clock output	CLK Q	Provides an ECL signal which can be used to control the transfer of the digital outputs into subsequent circuits (not available in the transparent mode). In the demultiplexing mode the frequency of CLK Q is half the sampling frequency (see "Modes of Operation").
22, 23 24, 25 26, 28 29	Output word 1	D0...D6	ECL outputs including overflow bit (D6) valid only in the demultiplexing mode. In this mode every first digital word of a pair of subsequent samples is delivered with a clock rate of half the sampling frequency. In the direct modes these outputs are undefined.
30, 31 32, 34 35, 36 37	Output word 2	D7...D13	ECL outputs (D13 overflow) delivering the second word of a pair in the demultiplexing mode. In the direct modes the digital data at these outputs appear with a clock rate equal to the sampling rate.

Pin Definitions and Functions (cont'd)

Pin	Name	Symbol	Function
19	Set Overflow	SO	A logic H at this ECL input or strapping the pin to GND D causes the overflow bit to be H and the data bits to be L when the analog signal exceeds the uppermost comparator threshold. If the pin is not connected or L is applied the data bits remain H in case of overflow.
20	Demultiplexing	$\overline{DEM}$	Setting this pin to H or strapping it to GND D sets the device in the direct mode.
7	Set transparent	TRP	A logic H (or GND D) at this input sets the device in the transparent mode (no pipelining). In this mode both DEM and HOLD inputs become ineffective. Besides, no clock output is provided.
4	Hold	HOLD	H active ECL input that immediately stops data transfer to the outputs (D0...D13) and inhibits the clock output. The last data word remains at the output and CLK Q is forced Low. In the direct mode the first valid output data together with the output clock appear one clock cycle after HOLD is released. In the demultiplexing mode clock and valid data appear after two conversion clock cycles with the first data word (corresponding to the first sampled value after HOLD is set to L) always present on D0...D6. HOLD is inactive in the transparent mode.
5, 6, 2, 16,	Analog supply	$V_{CC\,A}$, $V_{EE\,A}$, GND A	Supply voltages
15, 18, 17,	Digital supply	$V_{CC\,D}$, $V_{EE\,D}$, GND D	
3	Clock supply	$V_{CC\,C}$	
21, 27 33, 39	Output ground	GND 1	Return path for the emitter-follower current in the ECL output stages.

Figure 2
Block Diagram



Circuit Description

The A/D conversion is carried out in an array of 64 comparators connected in parallel to the analog input A IN. The signal is compared simultaneously with 64 equally spaced reference voltages provided by the resistor string $R_1 \ldots R_{65}$. With the rising edge of the conversion clock CLK I the result of the comparison is stored in the first comparator latch and afterwards passed to the second latch in a pipelining operation. Then the digital result of the comparison is pending at the comparators' output in a so-called thermometer code. Three subsequent encoding stages form the binary representation of the sampled value and a demultiplexer optionally divides the 300-MHz output data stream into two 150-MHz channels which are converted to ECL levels by two parallel output driver blocks. All clock signals for the pipelining and demultiplexing stages are formed internally by a clock driver circuit connected to the external conversion clock via CLK I. A clock signal for transferring the output data into subsequent circuitry is provided at CLK Q. If, however, the pipelined operation is disadvantageous (e.g. in subranging converter applications), all internal latches following the comparators may be set transparent via the programming input TRP. So any encode command directly causes the appearance of the respective output data after a short delay.

Clock Input (CLK I)

The clock inputs are designed to be driven differentially with ECL levels **(figure 3a).** Since CLK I is internally biased to −1.32 V, it is also possible to use CLK I single-ended. With this configuration a bypass capacitor from CLK I to GND A is recommended.

In this case the clock has to be stable with regard to the internal reference voltage to ensure the specified timing ($t_{WH,\ CLK\ I}$, $t_{WL,\ CLK\ I}$) over the operating range. For a continuously applied input clock the configuration shown in **figure 3b** is recommended. A capacitively coupled sinewave clock input (300 m V_{pp} typ.) can then be employed without degradation in performance **(figure 3c)**.

Analog and Reference Inputs

The input voltage range is determined by the voltages applied to the top ($+V_{REF}$) and bottom ($-V_{REF}$) of the resistor string. Two pins for each voltage allow a Kelvin connection (sense, force) if very high precision is required. Otherwise the parallel connection of these pins ensures low parasitic resistances. The analog input can be driven from a customary 50 Ω source since the input capacitance is a very low 12 pF, independent of input voltage, and the input voltage range may be set symmetric to ground.

Supply System

The supply system breaks down into three parts. The analog supply $V_{CC\ A}$, $V_{EE\ A}$ is connected to the first comparator stages, the digital supply $V_{CC\ D}$, $V_{EE\ D}$ serves for encoding, demultiplexer and output stages, and a special clock supply $V_{CC\ C}$ is provided to separate the high and noisy driver currents from the other supply systems. Additionally, a separate return path for the currents of the output emitter followers is established via GND 1.

Modes of Operation

The analog signal is sampled with every rising edge of the clock signal CLK I. By programming the TRP and DEM inputs three different output modes can be chosen:

a) Direct modes (figure 4):

The output data appear at the outputs D7...D13 with a word rate equal to the sampling rate. The logic state of the outputs D0...D6 is not defined.

One of two submodes can be chosen:

(I) Normal Mode (TRP low, DEM high)
Due to internal pipelining the output data appear one clock cycle after the rising edge of CLK I (sampling moment). CLK Q delivers a clock signal with the same frequency as CLK I.

(II) Transparent Mode (TRP high)
After a sampling command the associated output data appear directly with a delay of less than 7 ns. No output clock is available.

b) Demultiplexing mode (TRP low, DEM low; figure 5)

The output words corresponding to two subsequent samples appear simultaneously at the outputs D0...D6 and D7...D13, respectively, with half the clock rate of the conversion clock CLK I. After a HOLD pulse the word belonging to the first sample is always shown at D0...D6 and the delay between the first sample and output is two cycles of the conversion clock CLK I. At CLK Q a clock signal with half the frequency of the conversion clock, synchronous to the output data, is provided.

In all modes the output format in the overflow status can be programmed via the SO input. Setting SO to H causes the overflow bits (D6 and D13, respectively) to remain H and the data bits (D0...D5 and D7...D12, respectively) to go to L when the analog signal exceeds the threshold of comparator 64. If SO is set to L or not connected all data and overflow bits remain H in case of overflow **(figure 6).**

The HOLD input allows the output digital data stream to be stopped and restarted with defined output conditions. It is disabled in the transparent mode.

Absolute Maximum Ratings

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit
Pos. supply voltages	$V_{CC\,A}$ $V_{CC\,D}$ $V_{CC\,C}$	−0.3	6.0	V
Neg. supply voltages	$V_{EE\,A}$ $V_{EE\,D}$	−6.0	0.3	V
Analog input voltages	$+V_{REF}$ $-V_{REF}$ V_{AIN}	−2.5[1]	1.5	V
Digital input voltages	V_{CLKI} $V_{\overline{CKLI}}$ V_{DEM} V_{SO} V_{TRP}	−3.0	0.3	V
Output current	$I_{D0} \dots I_{D13}$		20	mA
Junction temperature	T_j		150	°C
Ambient temperature (without heat sink)	T_A	−25	50	°C
Storage temperature	T_{stg}	−40	125	°C
Thermal resistance Junction – ambient (without heat sink)	$R_{th\,JA}$		45	K/W

[1]) $+V_{REF}$ has to be more positive than $-V_{REF}$.

Characteristics

$V_{CC\,A}$, $V_{CC\,D}$, $V_{CC\,C}$ = 5 V ± 5%, $V_{EE\,A}$, $V_{EE\,D}$ = −4.5 V ± 5%,
T_j = 25 °C to 125 °C

Parameter	Symbol	Limit Values min.	Limit Values typ.	Limit Values max.	Unit
Supply					
Pos. supply currents	$I_{VCC\,A}$		50		mA
	$I_{VCC\,D}$		65		mA
	$I_{VCC\,C}$		35		mA
Total pos. supply current	I_{CC}			170	mA
Neg. supply currents	$I_{VEE\,A}$		45		mA
	$I_{VEE\,D}$		125		mA
Total neg. supply current	I_{EE}			180	mA
Power dissipation	P_D		1.5	1.8	W
Permissible supply voltage difference	$\Delta V_{CC}, \Delta V_{EE}$			100	mV

Characteristics

$V_{CC\,A}$, $V_{CC,\,D}$, $V_{CC\,C} = 5\ V \pm 5\%$, $V_{EE\,A}$, $V_{EE\,D} = -4.5\ V \pm 5\%$,
$T_j = 25\,°C$ to $125\,°C$

Parameter	Symbol	Limit Values min.	typ.	max.	Unit
Analog Section					
Signal input					
Voltage range	V_{AIN}	−2		1	V
Max. input current $V_{AIN} = +V_{REF}$	I_{AIN}		500	700	µA
Input capacitance	C_I		12		pF
Reference Inputs					
Reference voltages[4])	$+V_{REF}$, $-V_{REF}$	−2		1	V
Reference resistance	R_{REF}		200		Ω
Temperature coefficient of reference resistor	TC		1.7		10^{-3}/K
Digital Section					
Logic Levels					
H-input voltage[1])	V_{IH}	−1.165			V
L-input voltage[1])	V_{IL}			−1.475	V
H-output voltage[2]) $R_L = 100\ \Omega$	V_{QH}	−1.025		−0.88	V
L-output voltage[2]) $R_L = 100\ \Omega$	V_{QL}	−1.810		−1.620	V
Clock Inputs[3])					
Input current	I_{CLKI}			20	µA
Max. clock frequency	$f_{c,\,max}$	300	350		MHz
Aperture delay	t_A		1		ns
Hold time	$t_{WH,\,CLKI}$	1.2			ns
Strobe time	$t_{WL,\,CLKI}$	1.2			ns
Programming Inputs[3])					
H-input current	I_{IH}		80		µA
L-input current	I_{IL}		60		µA
Hold Input					
Setup time	$t_{S,\,HOLD}$	0.5			ns
Release time	$t_{R,\,HOLD}$	2			ns
High pulse width	$t_{W,\,HOLD}$	1			ns

[1]) applies to DEM, SO, HOLD, TRP
[2]) applies to DEM, SO, HOLD, TRP
[3]) applies to CLKQ, D0...D13
[4]) see "Circuit Description"

Characteristics

$V_{CC\,A}$, $V_{CC\,D}$, $V_{CC\,C}$ = 5 V ± 5%, $V_{EE\,D}$ = −4.5 V ± 5%, 25 °C < T_j < 125 °C

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Conditions
Data Outputs[1])						
Data valid range						
normal mode	$t_{V,N}$	3	3.5		ns	f_c = 250 MHz
transparent mode	$t_{V,T}$	2.5			ns	f_c = 250 MHz
demultiplexing mode	$t_{V,D}$	5	5.8		ns	f_c = 300 MHz
Output timing						
normal mode	$t_{d,N}$	0.5[2])			ns	f_c = 250 MHz
transparent mode	$t_{d,T}$			9	ns	
demultiplexing mode	$t_{d,D}$	0[2])			ns	f_c = 300 MHz
Clock Output						
Max. frequency[3])	$f_{Q\,max}$		250		MHz	
Clock delay LH	t_{dLH}		6		ns	
Clock delay HL	t_{dHL}		5.5		ns	
Static Nonlinearity						
Integral nonlinearity	*INL*			0.25	LSB	
Differential nonlinearity	*DNL*			0.25	LSB	
Dynamic Performance[4])						
Large signal bandwidth	f_{3dB}		250		MHz	
Effective resolution[5])						
f_c = 300 MHz, V_{AIN} = 2 V_{pp}						
f_{AIN} = 10 MHz			5.9		bit	
f_{AIN} = 50 MHz		5.6	5.8		bit	
f_{AIN} = 100 MHz		5.3	5.4		bit	
f_{AIN} = 150 MHz			5.0		bit	
Signal-to-noise ratio[6])	*SNR*					
f_c = 300 MHz, V_{AIN} = 2 V_{pp}						
f_{AIN} = 50 MHz		36	37.5		dB	
f_{AIN} = 100 MHz		35	36.5		dB	
f_c = 300 MHz, V_{AIN} = 1 V_{pp}						
f_{AIN} = 50 MHz			37		dB	
f_{AIN} = 100 MHz			36		dB	
Total harmonic distortion	*THD*					
f_{AIN} = 50 MHz, V_{AIN} = 2 V_{pp}			−44		dB	
f_{AIN} = 100 MHz, V_{AIN} = 2 V_{pp}			−39		dB	

1) Values refer to sinewave clock inputs (duty cycle 50%)
2) Increases with sampling period
3) Has been chosen lower than the max. sampling frequency because at very high input clock rates the device should preferably be operated in the demultiplexing mode.
4) Measured in a 50 Ω analog system at 300 MHz sampling rate (300 mV_{pp} sinewave clock)
5) Includes both noise and harmonic distortions
6) Without the effect of harmonics: thus b_{eff}, *SNR* [dB] and *THD* [dB] are related by $b_{eff} = ¦-10 \log -(10^{-SNR/10} + 10^{THD/10}) - 1.8¦/6$

Clock input
Figure 3a

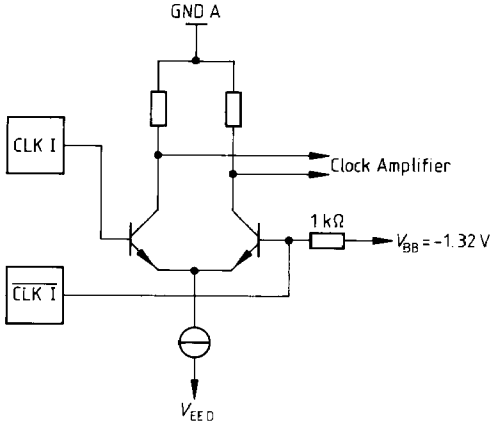


Figure 3b

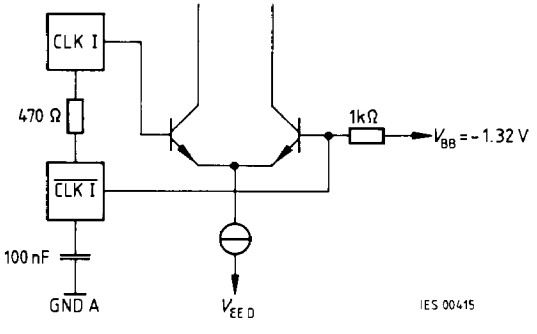


Figure 3c

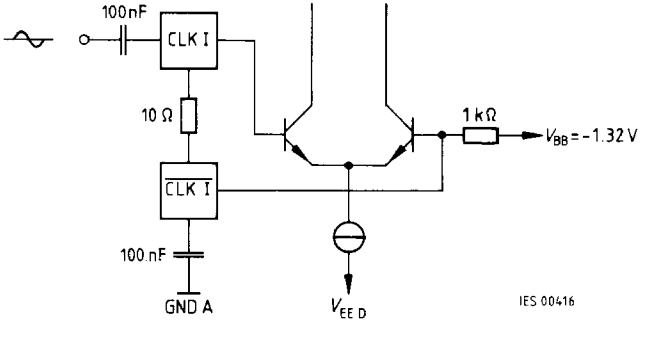


Figure 4
Timing Diagram
Direct Modes

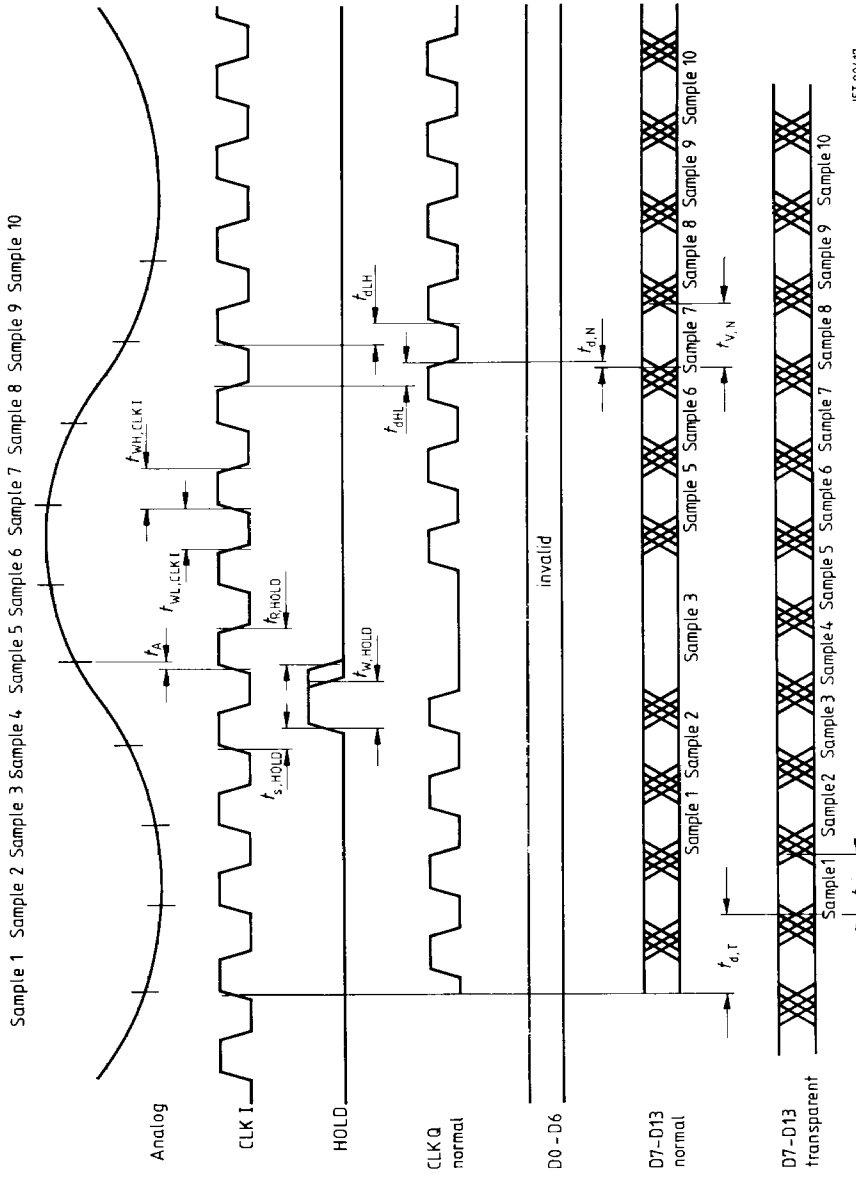


Figure 5
Demultiplexing Mode

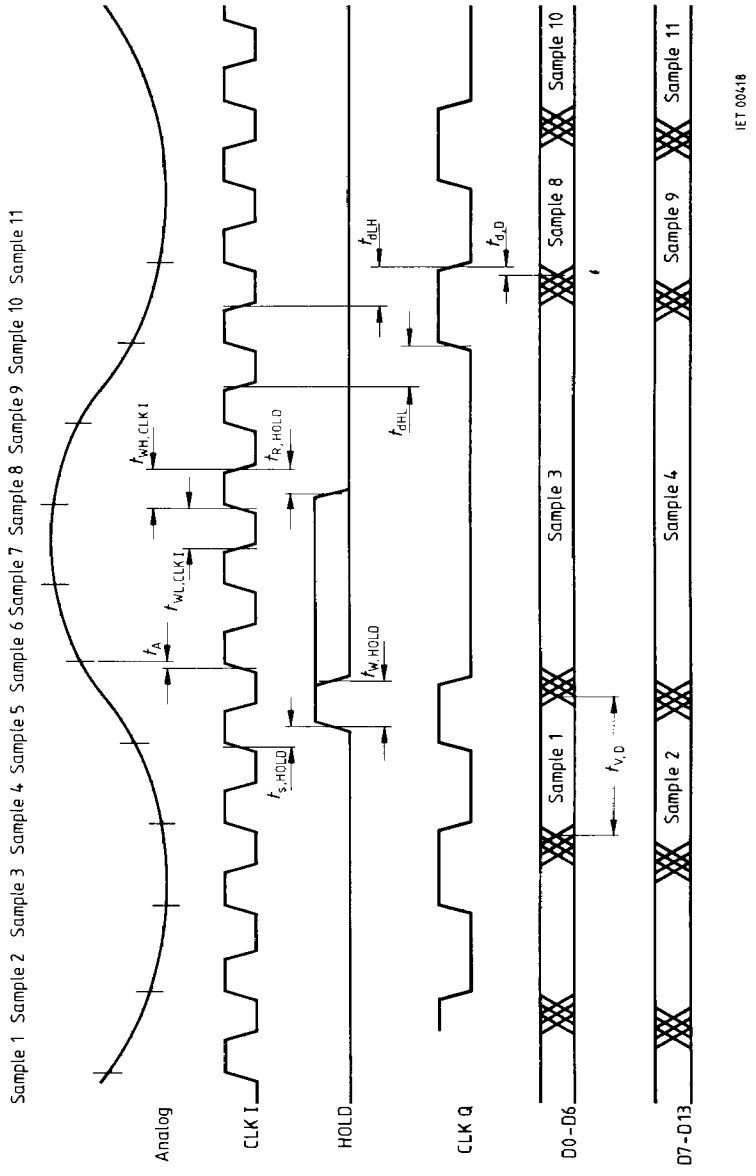
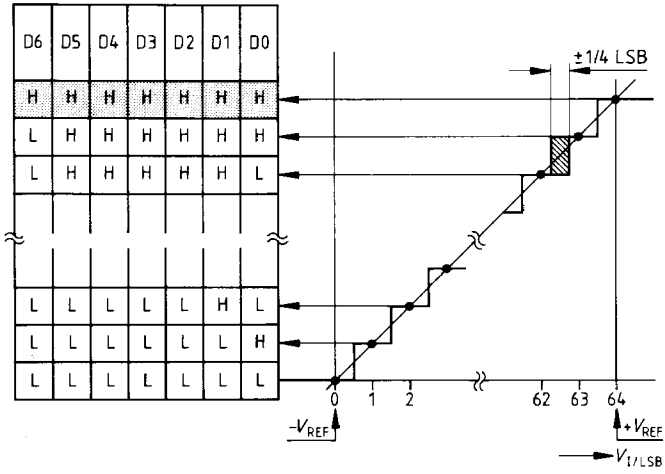
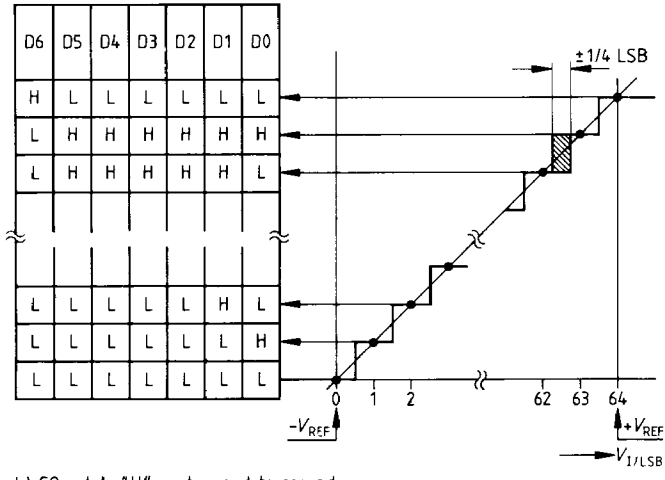


Figure 6
Transfer Characteristic and Truth Table

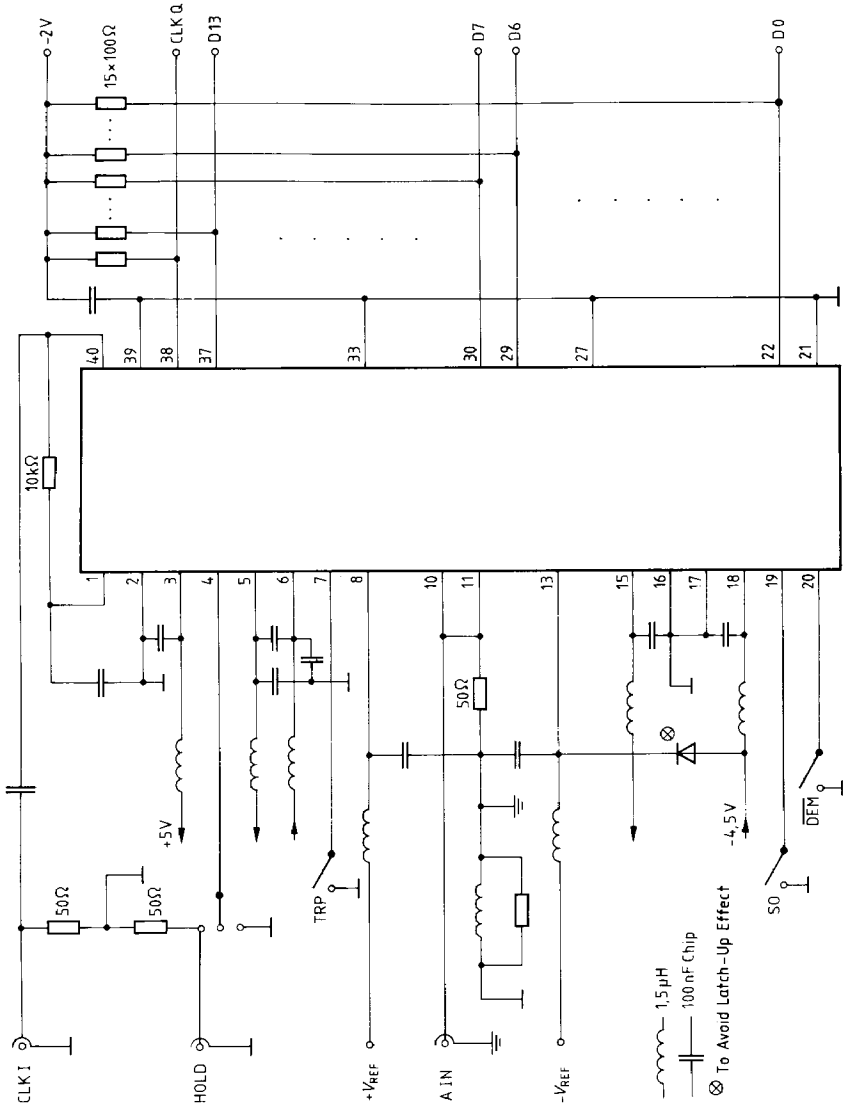


a) SO set to "L" or not connected

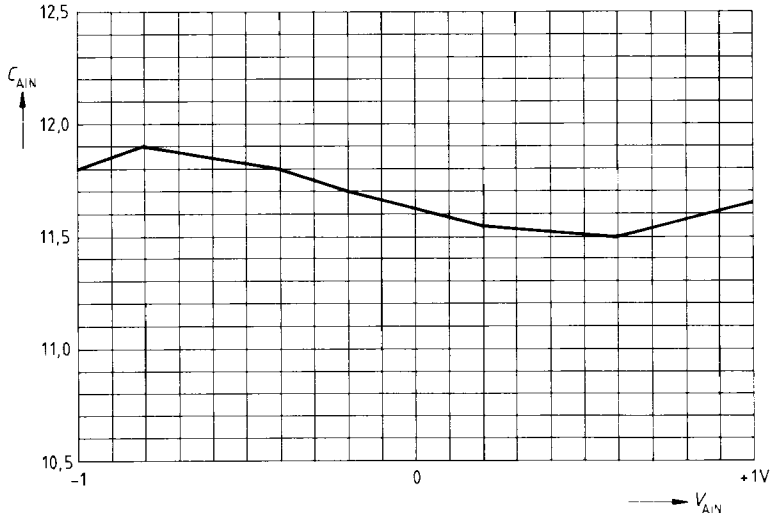


b) SO set to "H" or strapped to ground

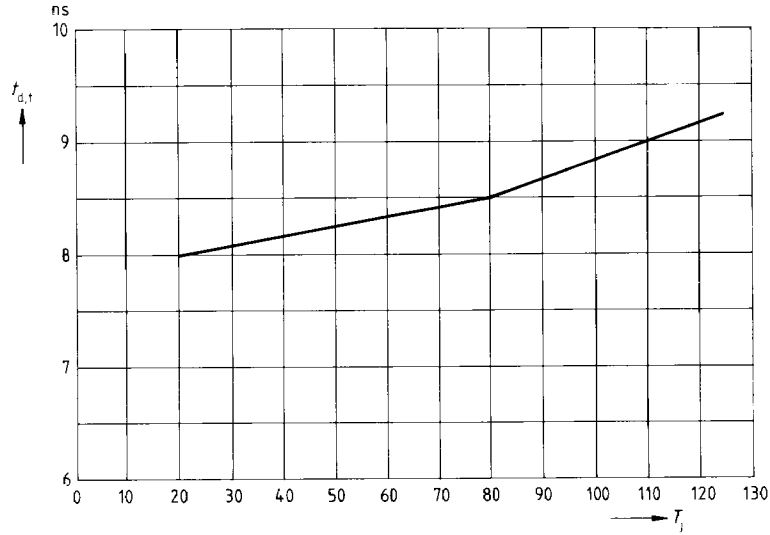
Figure 7
Test Circuit



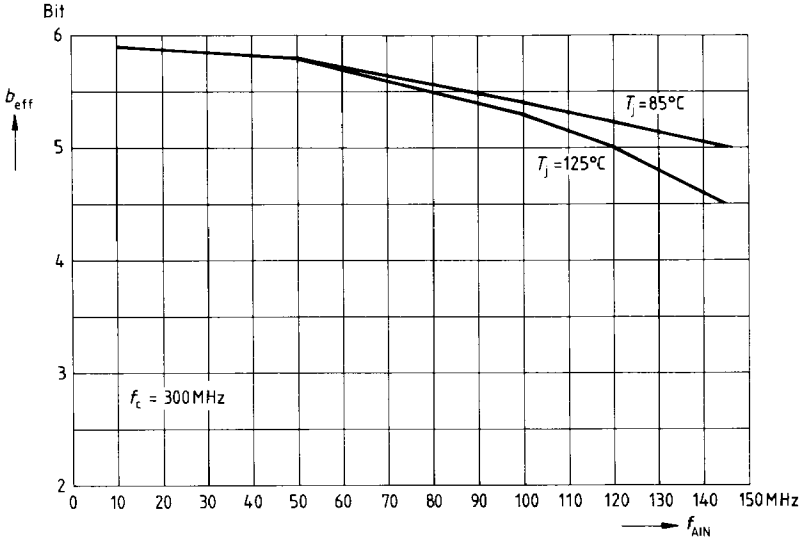
Analog Input Capacitance C_{AIN} versus Input Bias Voltage



Output Delay (Transparent Mode) $t_{d,T}$ versus Junction Temperature



Effective Resolution b_{eff} versus Analog Frequency



Signal-to-Noise-Ratio *SNR* and Total Harmonic Distortion *THD* versus Analog Frequency