

**9-BIT SERIAL-INPUT, LATCHED DRIVER**

**DESCRIPTION**

The M54970P is a semiconductor integrated circuit of  $I^2L$  structure containing a serial input to serial/parallel output 9-bit shift register and latch as well as a bipolar 9-bit parallel-output driver.

**FEATURES**

- Serial input to serial/parallel output
- Cascade connections possible through serial output
- Enable input for output control
- Power-cut input
- Driver : Withstand voltage .....  $BV_{CEO} \geq 20V$   
Large drive current .....  $(I_{O(max)}) = 300mA$
- Wide operating temperature range .....  $T_a = -20 \sim +75^\circ C$

**APPLICATION**

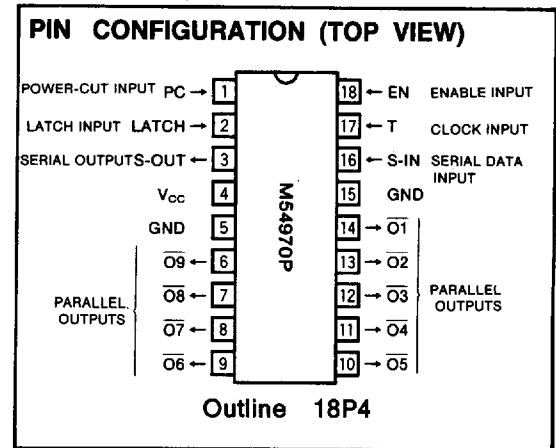
Thermal printer head dot driver, Serial-to-parallel conversion, Relay and Solenoid driver

**FUNCTION**

The M54970P consists of a 9bit D-type flip-flop, the output of which is connected to 9 latches.

When data is applied to the serial data input (S-IN) and a clock pulse is applied to clock input (T), an "L" to "H" change of the clock will cause the data input signals to enter the internal shift registers and the data in the shift registers will be shifted in order.

Using a number of M54970P units for bit expansion in

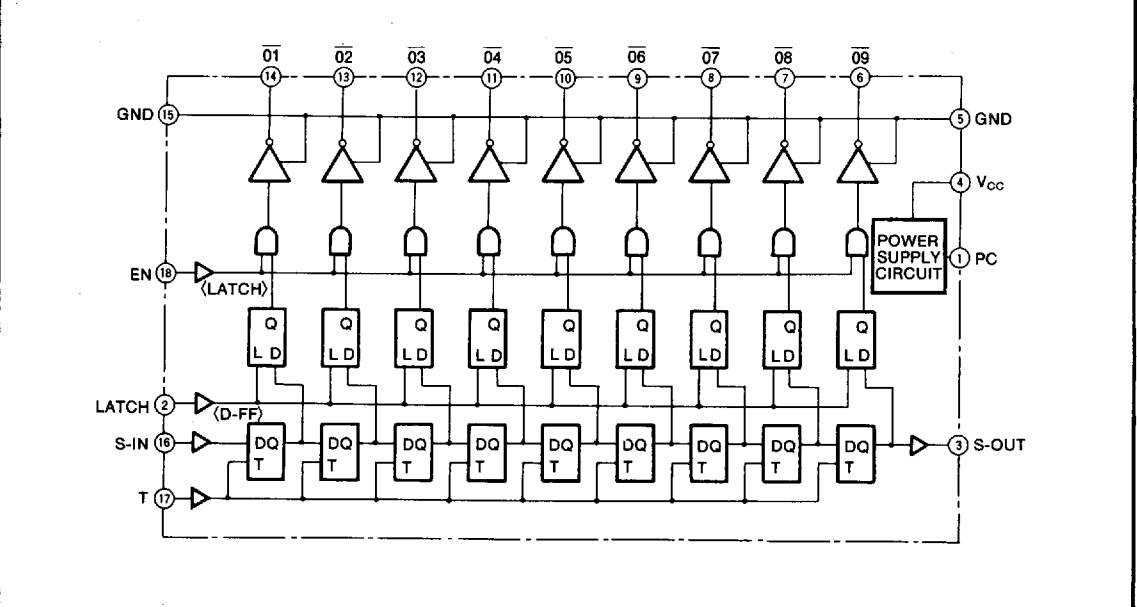


series will entail connecting serial output (S-OUT) to S-IN of the next-stage M54970P.

In parallel output, when the power-cut input and latch input are set to "H" and the output-control input (enable input EN) is "H", a clock pulse changing from "L" to "H" will cause the serial data input signal to appear at output  $01$ , and the data will be shifted in order at outputs  $02 \sim 09$ .

The parallel output will yield a signal that is inverted with respect to the serial data input.

**BLOCK DIAGRAM**



**9-BIT SERIAL-INPUT, LATCHED DRIVER**

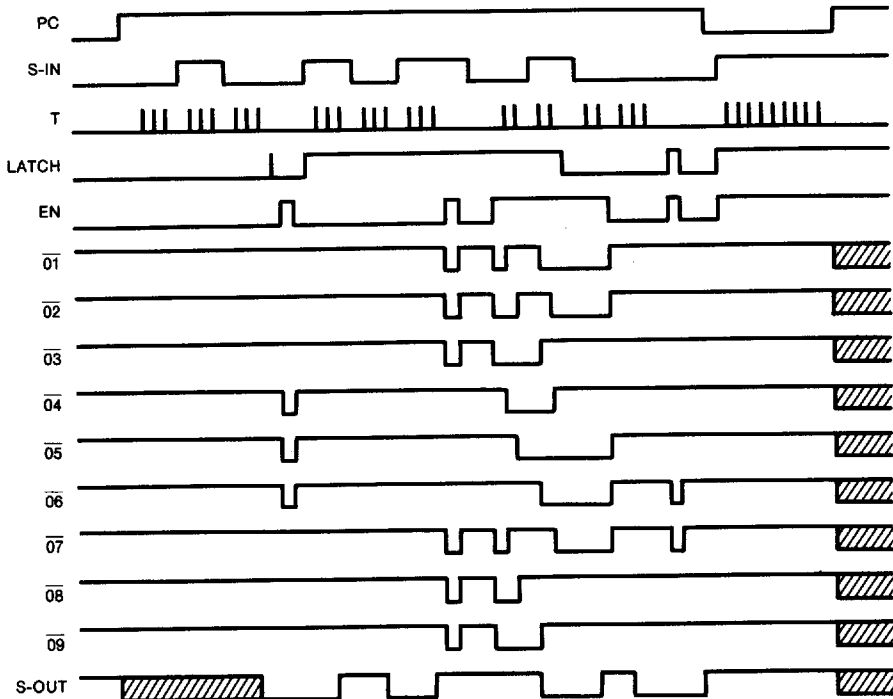
Setting the LATCH input to "L" will prevent data from entering the latch.

When the EN input is set to "L", all outputs ( $\overline{01} \sim \overline{09}$ ) will be set to OFF. Since the internal logic state of the IC is uncertain at power-on time, set the EN input to "L" (and outputs  $\overline{01} \sim \overline{09}$  will be set to OFF) until the input data is set and

the internal logic state has been determined.

The power will be cut when the power-cut input is set to "L", and since the data of the shift registers and latches are not maintained in this state, it will be necessary to input data again in order to set the output following a change of PC input from "L" to "H".

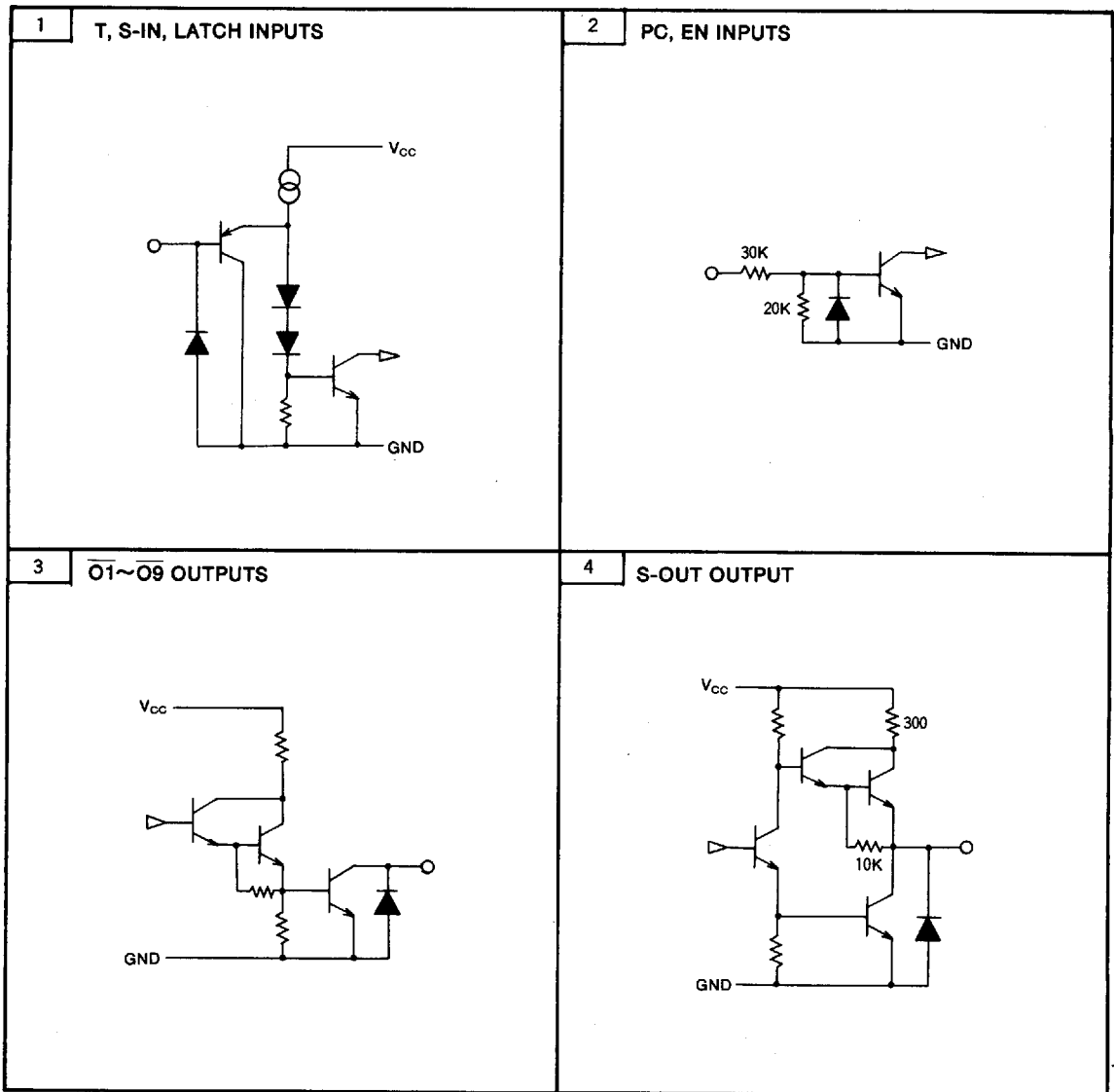
**TIMING CHART**



\*The state of the shaded areas is uncertain.

## 9-BIT SERIAL-INPUT, LATCHED DRIVER

## INPUT/OUTPUT EQUIVALENT CIRCUIT SCHEMATICS



## 9-BIT SERIAL-INPUT,LATCHED DRIVER

ABSOLUTE MAXIMUM RATINGS ( $T_a = -20^\circ\text{C} \sim +75^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
$V_{CC}$	Supply voltage		-0.5~+8	V
$V_I$	Input voltage		-0.5~+10	V
$V_O$	Output voltage	Output is OFF	-0.5~+20	V
$I_O$	Output current		350	mA
$P_D$	Power dissipation	$T_a = 25^\circ\text{C}$	1.25	W
$T_{opr}$	Operating temperature		-20~+75	$^\circ\text{C}$
$T_{stg}$	Storage temperature		-55~+125	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS ( $T_a = -20 \sim +75^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
$V_{CC}$	Supply voltage		4.5	5.0	5.5	V
$V_O$	Applied output voltage	When output is OFF			20	V
$I_O$	Output current (per circuit)	All outputs ON simultaneously Duty cycle less than 30%			300	mA

ELECTRICAL CHARACTERISTICS ( $T_a = +25^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameter	Test pin	Test conditions	Limits			Unit
				Min	Typ*	Max	
$V_{IH}$	High-level input voltage	2, 16, 17	$T_a = -20 \sim +75^\circ\text{C}$	2.2		$V_{CC}$	V
$V_{IL}$	Low-level input voltage			0		0.8	V
$V_{IH}$	High-level input voltage	1, 18	$T_a = -20 \sim +75^\circ\text{C}$	2.2		$V_{CC}$	V
$V_{IL}$	Low-level input voltage			0		0.8	V
$I_{IH}$	High-level input current	2, 16, 17	$V_{CC} = 5.5\text{V}$ , $V_{IH} = 2.4\text{V}$			10	$\mu\text{A}$
$I_{IL}$	Low-level input current		$V_{CC} = 5.5\text{V}$ , $V_{IL} = 0.4\text{V}$			-50	$\mu\text{A}$
$I_{IH}$	High-level input current	1, 18	$V_{CC} = 5.5\text{V}$ , $V_{IH} = 5.5\text{V}$			250	$\mu\text{A}$
$I_{IL}$	Low-level input current		$V_{CC} = 5.5\text{V}$ , $V_{IL} = 0\text{V}$			100	$\mu\text{A}$
$I_{IH}$	High-level input current		$V_{CC} = 5.5\text{V}$ , $V_{IH} = 2.4\text{V}$			-10	$\mu\text{A}$
$I_{IL}$	Low-level input current		$V_{CC} = 5.5\text{V}$ , $V_{IL} = 0\text{V}$			-10	$\mu\text{A}$
$V_{OH}$	High-level output voltage	3	$V_{CC} = 4.5\text{V}$ , $I_{OH} = -400\mu\text{A}$	2.4			V
$V_{OL}$	Low-level output voltage		$V_{CC} = 4.5\text{V}$ , $I_{OL} = 8\text{mA}$			0.4	V
$V_{OL}$	Low-level output voltage	6~14	$V_{CC} = 4.5\text{V}$ , $I_{OL} = 300\text{mA}$			0.6	V
$I_{CC1}$	Supply current	4	$V_{CC} = 5.5\text{V}$ , power-cut is ON			10	$\mu\text{A}$
$I_{CC2}$			$V_{CC} = 5.5\text{V}$ , EN is "L"		10	15	mA
$I_{CC3}$			$V_{CC} = 5.5\text{V}$ , all outputs are ON		90	130	mA
$I_{O(leak)}$	Output leakage current	6~14	$V_{CC} = 5.5\text{V}$ , $V_{OH} = 20\text{V}$			100	$\mu\text{A}$

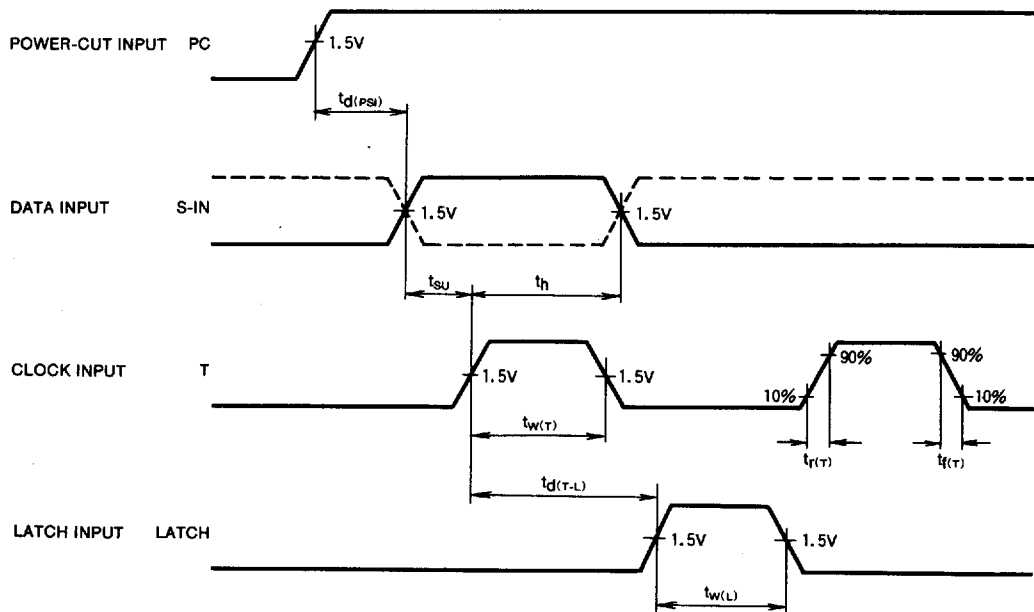
\* : Typical values are at  $T_a = 25^\circ\text{C}$ .

## 9-BIT SERIAL-INPUT, LATCHED DRIVER

REQUIRED TIMING CONDITIONS ( $T_a = -20 \sim +75^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
$f_{(T)}$	Clock frequency	Input duty cycle 40~60%			1	MHz
$t_{w(T)}$	Clock pulse width		0.4			$\mu\text{S}$
$t_{w(L)}$	Latch pulse width		0.4			$\mu\text{S}$
$t_{su}$	Data setup time		0.2			$\mu\text{S}$
$t_h$	Data hold time		0.3			$\mu\text{S}$
$t_{d(T-L)}$	Clock-latch time		1			$\mu\text{S}$
$t_{r(T)}$	Clock pulse rise time				0.5	$\mu\text{S}$
$t_{f(T)}$	Clock pulse fall time				0.5	$\mu\text{S}$
$t_{d(P-S)}$	Power-cut input $\rightarrow$ data input setting time	Hold EN input at "L" when PC input is changed from "L" to "H"	2			$\mu\text{S}$

## TIMING DIAGRAM

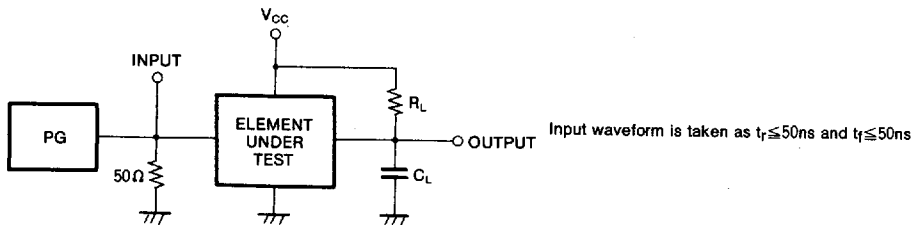


**9-BIT SERIAL-INPUT, LATCHED DRIVER**

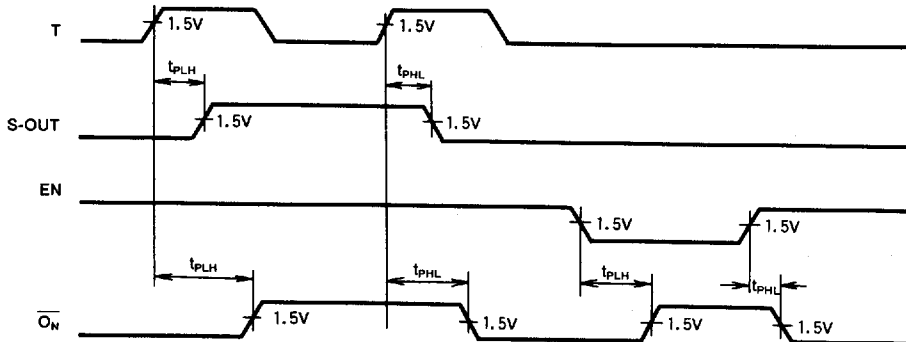
**SWITCHING CHARACTERISTICS** ( $T_a=25^\circ\text{C}$ ,  $V_{CC}=5\text{V}$ )

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
$t_{PLH}$	Low to high-level output propagation time (Input T to output S-OUT)	$V_{IH}=3\text{V}$ $V_{IL}=0\text{V}$ $R_L: S\text{-OUT}=2\text{K}\Omega$ $R_L: \overline{O_N}=100\Omega$ (N=1~9) $C_L=15\text{pF}$ (Note 1)			0.7	$\mu\text{S}$
$t_{PHL}$	High to low-level output propagation time (Input T to output S-OUT)				0.8	$\mu\text{S}$
$t_{PLH}$	Low to high-level output propagation time (Input T to output $\overline{O_N}$ )				5	$\mu\text{S}$
$t_{PHL}$	High to low-level output propagation time (Input T to output $\overline{O_N}$ )				1	$\mu\text{S}$
$t_{PLH}$	Low to high-level output propagation time (Input EN to output $\overline{O_N}$ )				10	$\mu\text{S}$
$t_{PHL}$	High to low-level output propagation time (Input EN to output $\overline{O_N}$ )				1	$\mu\text{S}$

(Note 1) TEST CIRCUIT



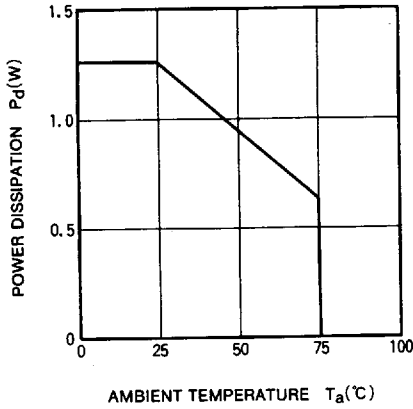
**TIMING DIAGRAM**



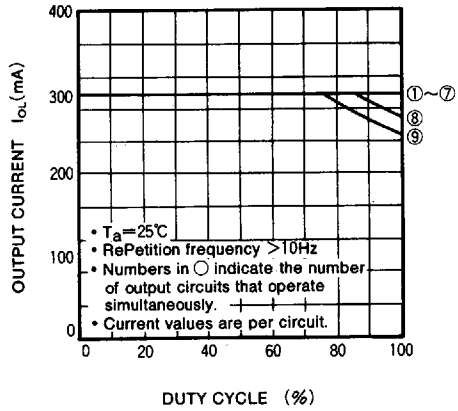
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TYPICAL CHARACTERISTICS

THERMAL DERATING



DUTY CYCLE VS PERMISSIBLE OUTPUT CURRENT



DUTY CYCLE VS PERMISSIBLE OUTPUT CURRENT

